Integrated Device Technology, Inc.

# 64K x 32 CMOS STATIC RAM MODULE

**IDT7M4017**

## FEATURES:

- High-density 2 megabit CMOS static RAM module
- Fast access time
  - — Military: 40ns (max.)
  - — Commercial: 30ns (max.)
- Individual byte selects
- Upper and lower word write enables
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7M4017 is a (64K x 32) high-speed CMOS static RAM module constructed on a co-fired ceramic substrate using eight 32K x 8 static RAMs in leadless chip carriers. On-board decoders use $A_{15}$ to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

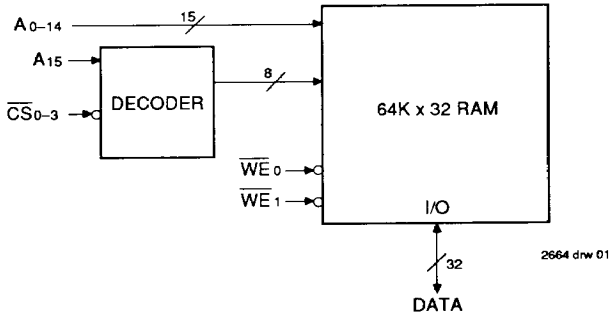
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

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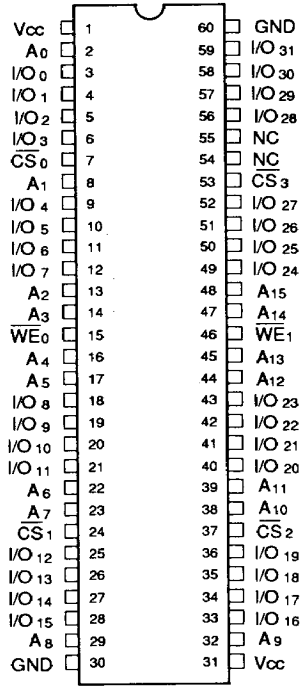
## PIN CONFIGURATION[1]




2664 drw 02

**DIP**
**TOP VIEW**

**NOTE:**
1. For module dimensions, please refer to module drawing M16 in the packaging section.

## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{15}$ | Addresses |
| $I/O_{0-31}$ | Data Inputs/Outputs |
| $\overline{CS}_0$ | Chip Select for $I/O_{0-7}$ |
| $\overline{CS}_1$ | Chip Select for $I/O_{8-15}$ |
| $\overline{CS}_2$ | Chip Select for $I/O_{16-23}$ |
| $\overline{CS}_3$ | Chip Select for $I/O_{24-31}$ |
| $\overline{WE}_0$ | Write Enable for $I/O_{0-15}$ |
| $\overline{WE}_1$ | Write Enable for $I/O_{16-31}$ |
| GND | Ground |
| Vcc | Power |

2664 tbl 01

## TRUTH TABLE

| Mode | $\overline{CS}_X$ | $\overline{WE}_X$ | Output | Power |
|---|---|---|---|---|
| Standby | L | X | X | Standby |
| Read | L | H | $D_{OUT}$ | Active |
| Write | L | L | $D_{IN}$ | Active |

2664 tbl 09

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to + 7.0 | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | -55 to +125 | ° C |
| $T_{BIAS}$ | Temperature Under Bias | -10 to +85 | -65 to +135 | ° C |
| $T_{STG}$ | Storage Temperature | -55 to + 125 | -65 to +150 | ° C |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

2664 tbl 02

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = + 25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN(D)}$ | Input Capacitance (Data) | $V_{IN}$ = 0V | 30 | pF |
| $C_{IN(A)}$ | Input Capacitance (Address and Control) | $V_{IN}$ = 0V | 100 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 12 | pF |

2664 tbl 10

**NOTE:**
1. This parameter is guaranteed by design, but not tested.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | - | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | - | 0.8 | V |

2664 tbl 03

**NOTE:**
1. $V_{IL}$ (min.) = –3.0V for pulse width less than 20ns.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55° C to + 125° C | 0V | 5.0V ± 10% |
| Commercial | 0° C to + 70° C | 0V | 5.0V ± 10% |

2664 tbl 04

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5V ± 10%, $T_A$ = 0°C to +70°C and -55°C to +125°C)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage (Address & Control) | $V_{CC}$ = Max. $V_{IN}$ = GND to $V_{CC}$ | — | 20 | µA |
| $\|I_{LI}\|$ | Input Leakage (Data) | $V_{CC}$ = Max. $V_{IN}$ = GND to $V_{CC}$ | — | 10 | µA |
| $\|I_{LO}\|$ | Output Leakage | $V_{CC}$ = Max. $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8mA | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ = Min., $I_{OH}$ = -4mA | 2.4 | — | V |

2664 tbl 05

| Symbol | Parameter | Test Conditions | Commercial Max. | Military Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$(1) | Dynamic Operating Current | $V_{CC}$ = Max; $\overline{CS}$ ≤ $V_{IL}$; f = $f_{MAX}$ Output Open | 750 | 790 | mA |
| $I_{SB}$ | Standby Supply Current (TTL Level) | $\overline{CS}$ ≥ $V_{IH}$, $V_{CC}$ = Max., Outputs Open | 180 | 180 | mA |
| $I_{SB1}$ | Full Standby Supply Current (CMOS Levels) | $\overline{CS}$ ≥ $V_{CC}$ – 0.2V $V_{IN}$ ≥ $V_{CC}$ – 0.2V or ≤ 0.2V | 135 | 175 | mA |

2664 tbl 06

**NOTE:**
1. For tAA = 30, 35ns versions, ICC = 900 mA.

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## AC TEST CONDITIONS

| | |
|---|---|
| In Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 10ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

2664 tbl 07

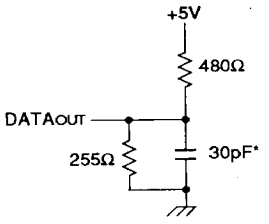
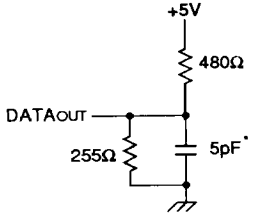



Figure 1. Output Load




2664 drw 03

Figure 2. Output Load (for tCLZ, tCHZ, tOW, tWHZ)

* Including scope and jig.

## AC ELECTRICAL CHARACTERISTICS

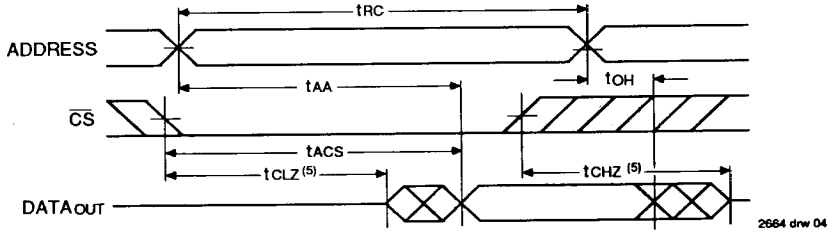
($V_{CC}$ = 5V ± 10%, $T_A$ = 0°C to +70°C and -55°C to +125°C)

| Symbol | Parameter | 7M4017S30 | | 7M4017S35 | | 7M4017S40 | | 7M4017S45 | | 7M4017S50 | | 7M4017S60 | | 7M4017S70 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | | | | | | | | | |
| tRC | Read Cycle Time | 30 | — | 35 | — | 40 | — | 45 | — | 50 | | 60 | — | 70 | — | ns |
| tAA | Address Access Time | — | 30 | — | 35 | — | 40 | — | 45 | — | 50 | — | 60 | — | 70 | ns |
| tACS | Chip Select Access Time | — | 30 | — | 35 | — | 40 | — | 45 | — | 50 | — | 60 | — | 70 | ns |
| tCLZ(1) | Chip Select to Output in Low Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| tCHZ(1) | Chip Deselect to Output in High Z | — | 15 | — | 17 | — | 20 | — | 20 | — | 20 | — | 25 | — | 25 | ns |
| tOH | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| tPU(1) | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tPD(1) | Chip Deselect to Power Down Time | — | 30 | — | 35 | — | 40 | — | 45 | — | 50 | — | 60 | — | 70 | ns |
| **Write Cycle** | | | | | | | | | | | | | | | | |
| tWC | Write Cycle Time | 30 | — | 35 | — | 40 | — | 45 | — | 50 | — | 60 | — | 70 | — | ns |
| tCW | Chip Select to End of Write | 25 | — | 30 | — | 35 | — | 40 | — | 45 | — | 55 | — | 60 | — | ns |
| tAW | Address Valid to End of Write | 27 | — | 30 | — | 35 | — | 40 | — | 45 | — | 55 | — | 60 | — | ns |
| tAS | Address Set-up Time | 2 | — | 5 | — | 5 | — | 5 | — | 10 | — | 10 | — | 10 | — | ns |
| tWP | Write Pulse Width | 20 | — | 25 | — | 30 | — | 35 | — | 35 | — | 45 | — | 50 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWHZ(1) | Write Enable to Output in High Z | — | 12 | — | 13 | — | 15 | — | 20 | — | 20 | — | 25 | — | 30 | ns |
| tDW | Data to Write Time Overlap | 13 | — | 14 | — | 15 | — | 20 | — | 20 | — | 25 | — | 30 | — | ns |
| tDH | Data Hold from Write Time | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| tOW(1) | Output Active from End of Write | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |

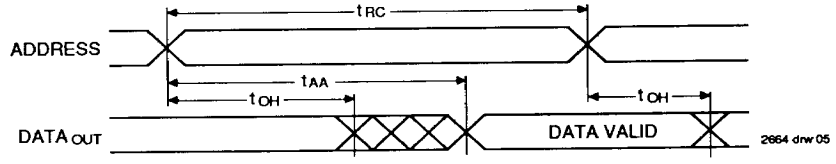
2664 tbl 08

**NOTE:**
1. This parameter is guaranteed by design, but not tested.

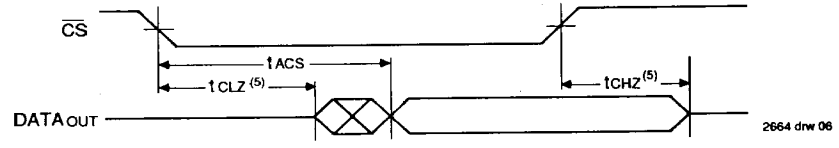
## TIMING WAVEFORM OF READ CYCLE NO. 1(1)




## TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)




## TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)




**NOTES:**
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is guaranteed by design, but not tested.

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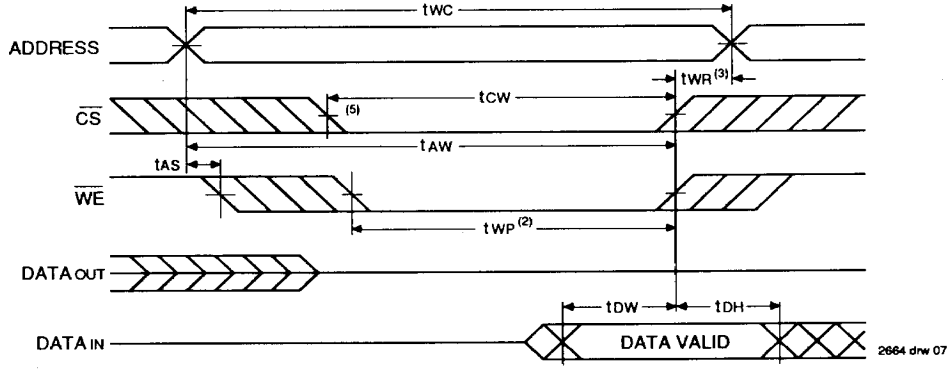
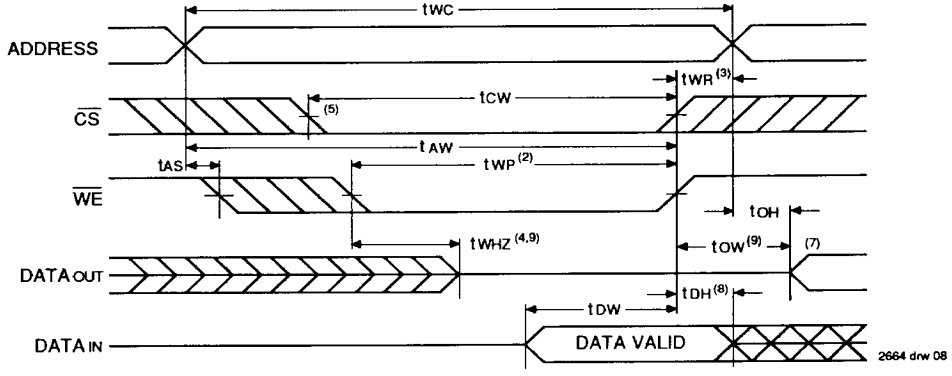
## TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]

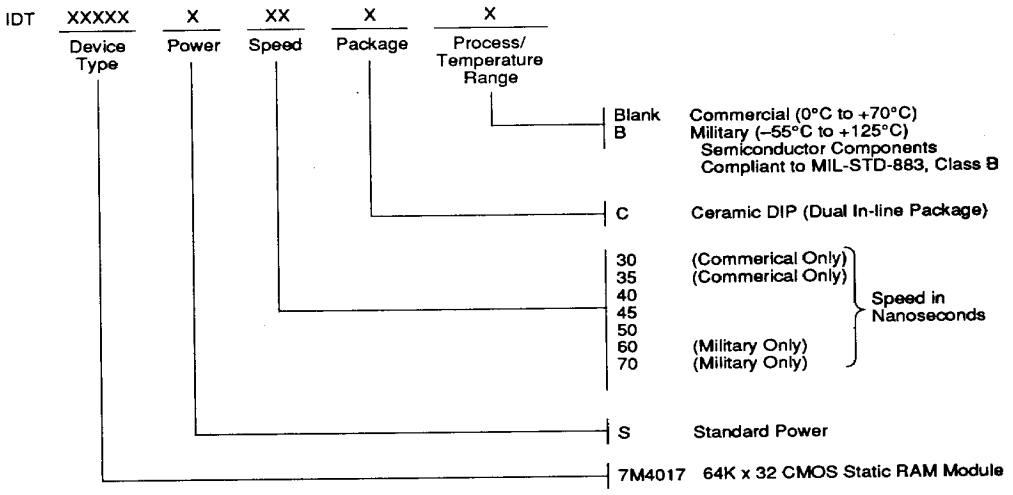



## TIMING WAVEFORM OF WRITE CYCLE NO. 2[1, 6]




**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CS low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is guaranteed by design, but not tested.

## ORDERING INFORMATION

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