SPP3413

DESCRIPTION

The SPP3413 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

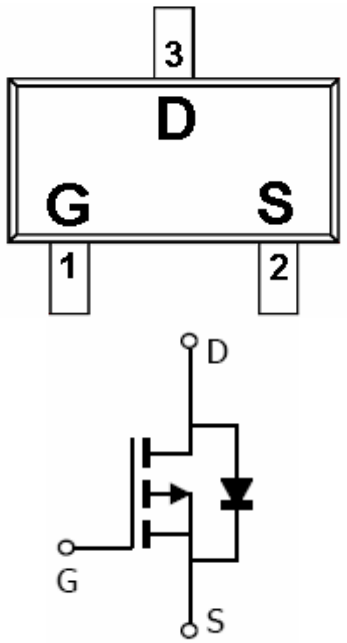
FEATURES

- -20V/-3.4A,$R_{DS(ON)}$= 95mΩ@V_{GS}=-4.5V
- -20V/-2.4A,$R_{DS(ON)}$=120mΩ@V_{GS}=-2.5V
- -20V/-1.7A,$R_{DS(ON)}$=145mΩ@V_{GS}=-1.8V
- -20V/-1.0A,$R_{DS(ON)}$=210mΩ@V_{GS}=-1.25V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

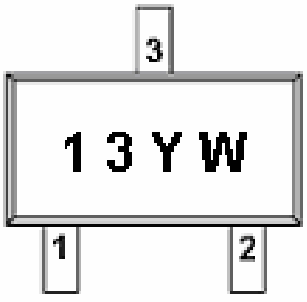
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23-3L)



PART MARKING



Y : Year Code
W : Week Code

SPP3413

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3413S23RG	SOT-23-3L	13YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP3413S23RG : Tape Reel ; Pb – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-3.5	A
	T_A=70℃		-2.8	
Pulsed Drain Current		I_{DM}	-15	A
Continuous Source Current(Diode Conduction)		I_S	-1.4	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

SPP3413

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.35		-0.8	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V			-1	uA
		V_{DS}=-20V,V_{GS}=0V T_J=55℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-4.5V	-6			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-3.4A		0.076	0.095	Ω
		V_{GS}=-2.5V,I_D=-2.4A		0.097	0.120	
		V_{GS}=-1.8V,I_D=-1.7A		0.123	0.145	
		V_{GS}=-1.25V,I_D=-1.0A		0.185	0.210	
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-2.8A		6		S
Diode Forward Voltage	V_{SD}	I_S=-1.5A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-6V,V_{GS}=-4.5V I_D≡-2.8A		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	V_{DS}=-6V,V_{GS}=0V f=1MHz		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	V_{DD}=-6V,R_L=6Ω I_D≡-1.0A,V_{GEN}=-4.5V R_G=6Ω		10	16	ns
	t_r			13	23	
Turn-Off Time	$t_{d(off)}$			18	25	
	t_f			15	20	