Low Dropout 300mA Linear Regulator With Power-Ok Indicator

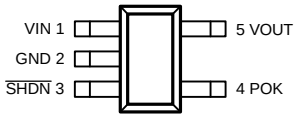
Features

- **Wide Operating Voltage: 2.8~6V**
- **Fixed Output Voltage in the range of 0.8V~5.5V**
- **Low Dropout Voltage:**
  170mV(typical) @ 300mA
- **Guaranteed 300mA Output Current**
- **Power-Ok Indicator**
- **Current Limit Protection with Foldback Current**
- **Internal Soft-Start**
- **Over Temperature Protection**
- **Stable with Low ESR Ceriamic Capacitors**
- **SOT-23-5 Package**
- **Lead Free and Green Devices Available**
  (RoHS Compliant)

General Description

The APL5316 is a low dropout linear regulator which needs only a single input voltage supply from 2.8 to 6V, and it can deliver output current up to 300mA. It can work with low ESR ceramic capacitors and ideally use in the battery-powered applications, such as notebook computers and cellular phones. Its typical dropout voltage is only 170mV at 300mA loading. A power-ok detection indicates the output status at POK pin. The current limit protection (with foldback current) and thermal shutdown functions protect the device against current overloads and over temperature. The APL5316 is available in a SOT-23-5 package.

Pin Configuration



APL5316
SOT-23-5

Applications

- **Cellular Phones**
- **Portable and Battery-powered Equipment**
- **Notebook and Personal Computers**

Ordering and Marking Information

APL5316 □□□□ – □□ □

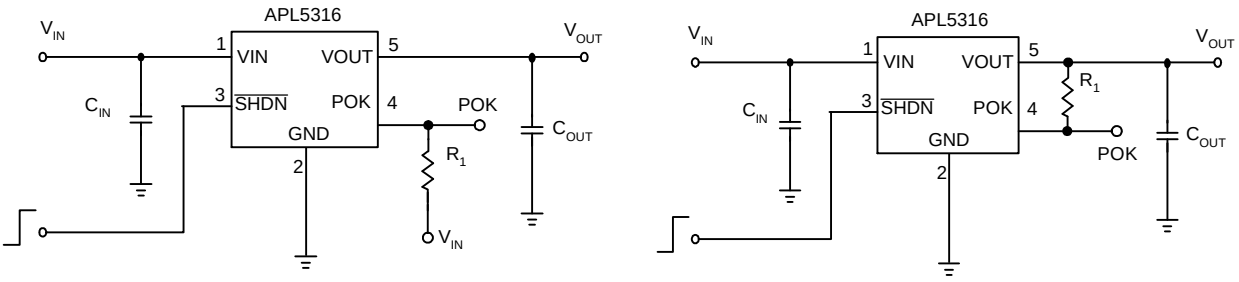
- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- Voltage Code

Package Code
B : SOT-23-5
Operating Junction Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Voltage Code
12 : 1.2V 33 : 3.3V
Assembly Material
L : Lead Free Device G: Halogen and Lead Free Device

APL5316 -12 B:	365X	APL5316 -33 B:	36RX	X - Date code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Simplified Application Circuits



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6.5	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Voltage ($\overline{SHDN}$ to GND)	-0.3 ~ 6.5	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	-40 ~ 150	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	℃

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note 1)	240	°C/W
θ_{JC}	Thermal Resistance- Junction to Case	130	°C/W

Note 1 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	2.8 ~ 6	V
V_{OUT}	Output Voltage	Fixed Voltage	V
I_{OUT}	VOUT Output Current	0 ~ 300	mA
C_{OUT}	Output Capacitor	1.5 ~ 22	µF
T_J	Junction Temperature	-40 ~ 125	°C

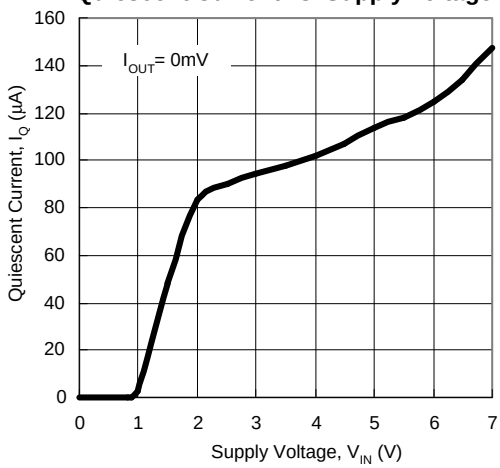
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN} = V_{OUT}+1V (min V_{IN}=2.8V), I_{OUT}=0~300mA, C_{IN} = 1µF, C_{OUT} = 2.2µF, T_A = -40 to 85°C. Typical values are at T_A = 25°C.

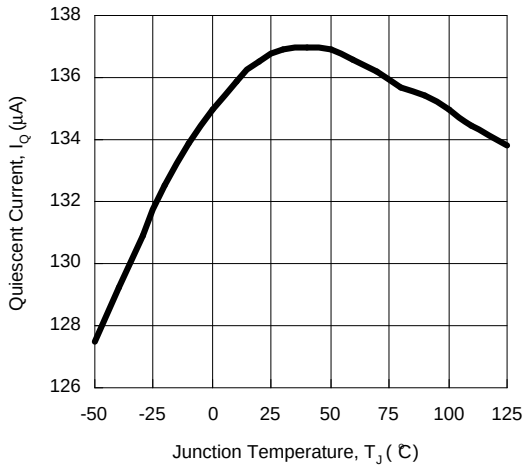
Symbol	Parameter	Test Conditions	APL5316			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.8	-	6	V
I_Q	Quiescent Current	I_{OUT} =10mA ~300mA	-	135	160	µA
	Output Voltage Accuracy	I_{OUT}=10mA	-2	-	+2	%
REG_{LINE}	Line Regulation	ΔV_{OUT}%/ΔV_{IN}, I_{OUT}=10mA	-0.06	-	+0.06	%/V
REG_{LOAD}	Load Regulation	ΔV_{OUT}%/ΔI_{OUT}	-0.2	-	+0.2	%/A
V_{DROP}	Dropout Voltage	V_{OUT} = 3.3V, I_{OUT} = 300mA	-	170	300	mV
PSRR	Power Supply Ripple Rejection Ratio	f = 10kHz, I_{OUT} = 300mA	-	45	-	dB
I_{LIMIT}	Current Limit		450	600	-	mA
I_{SHORT}	Foldback Current	V_{OUT} = 0V	-	80	-	mA
	$\overline{SHDN}$ Input Voltage High		1.6	-	-	V
	$\overline{SHDN}$ Input Voltage Low		-	-	0.4	
	Shutdown VIN Supply Current	$\overline{SHDN}$ = Low, V_{IN} = 6V	-	0.1	1	µA
	$\overline{SHDN}$ Pull Low Resistance		-	3	-	MΩ
	V_{OUT} Discharge MOSFET $R_{DS(ON)}$	$\overline{SHDN}$ = Low	-	60	-	Ω
	Over Temperature Threshold		-	160	-	℃
	Over Temperature Hysteresis		-	40	-	℃
T_{SS}	Soft-Start Interval		-	60	-	µs
V_{POK}	POK threshold Voltage for Power Ok	V_{OUT} Rising	89	92	95	%V_{OUT}
V_{PNOK}	POK threshold Voltage for Power Not Ok	V_{OUT} falling	78	81	84	%V_{OUT}
	POK Low Voltage	POK sinks 5mA	-	0.25	0.4	V

Typical Operating Characteristics

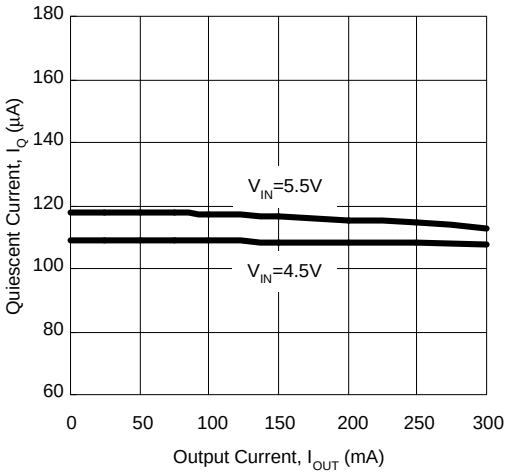
Quiescent Current vs. Supply Voltage



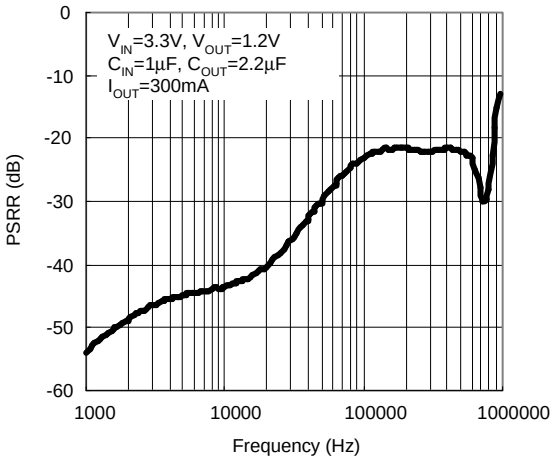
Quiescent Current vs. Junction Temperature



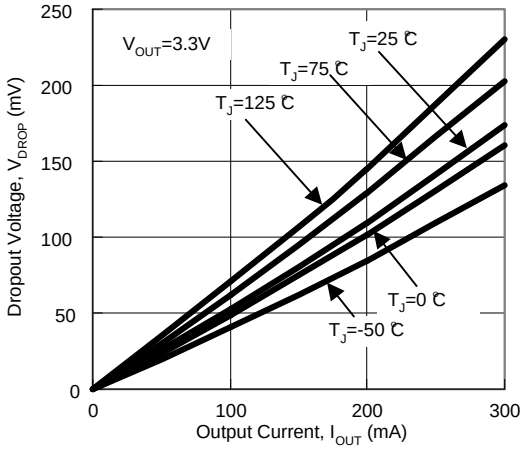
Quiescent Current vs. Output Current



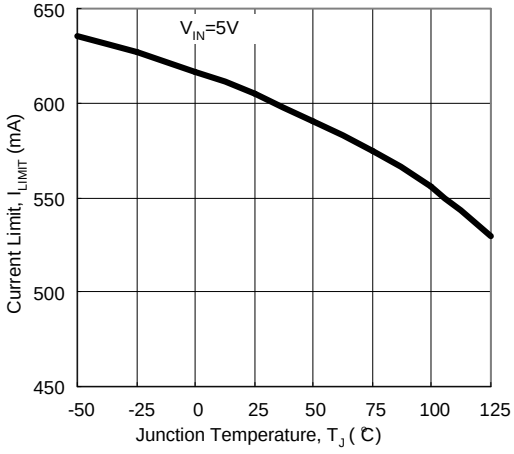
PSRR vs. Frequency



Dropout Voltage vs. Output Current

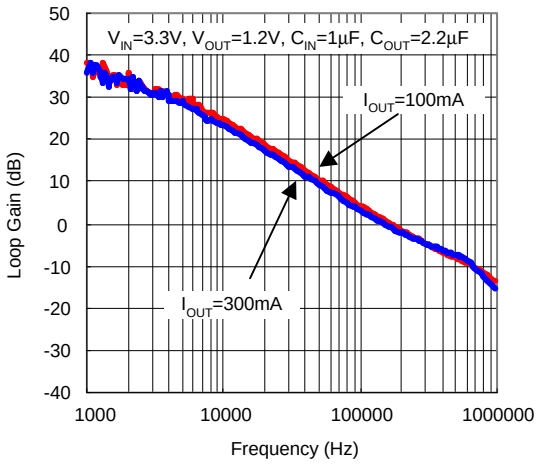


Current Limit vs. Junction Temperature

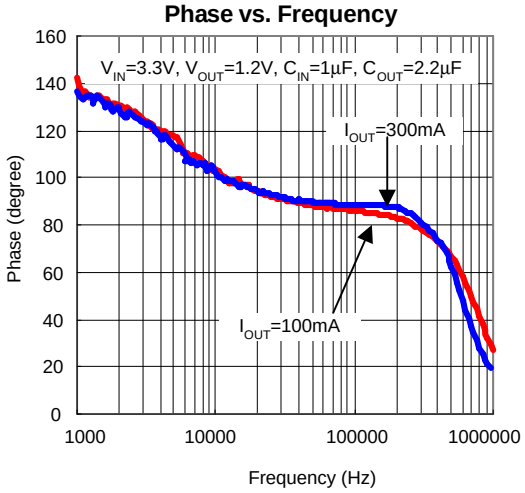


Typical Operating Characteristics (Cont.)

Loop Gain vs. Frequency

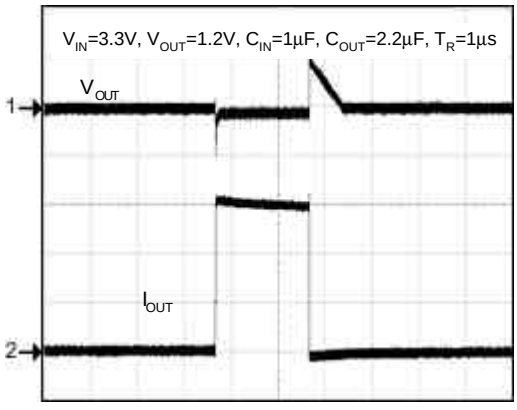


Phase vs. Frequency



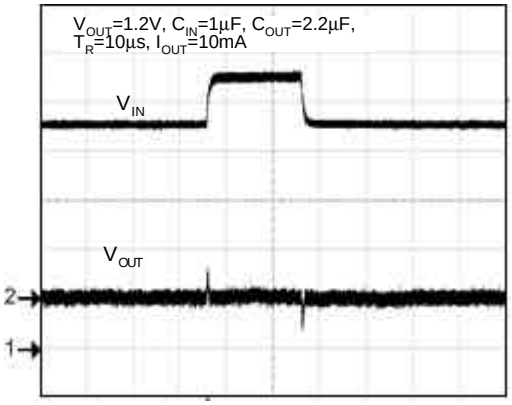
Operating Waveforms

Load Transient



CH1 : V_{OUT}, 50mV/div, AC
CH2 : I_{OUT}, 100mA/div, DC
Time : 100µs/div

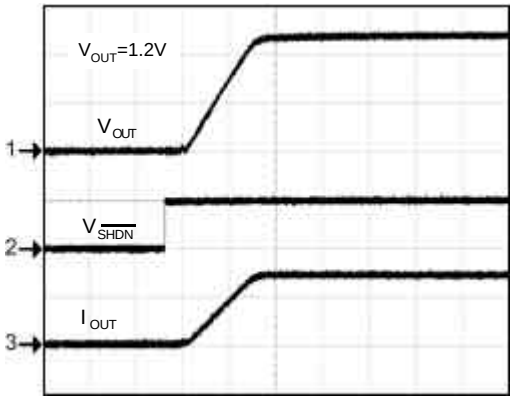
Line Transient



CH1 : V_{IN}, 1V/div, DC
CH2 : V_{OUT}, 20mV/div, AC
Time : 100µs/div

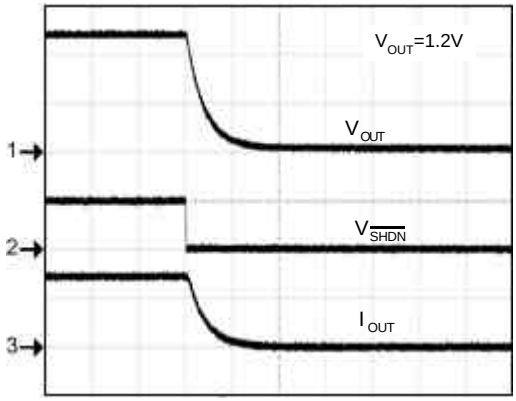
Operating Waveforms (Cont.)

Enable



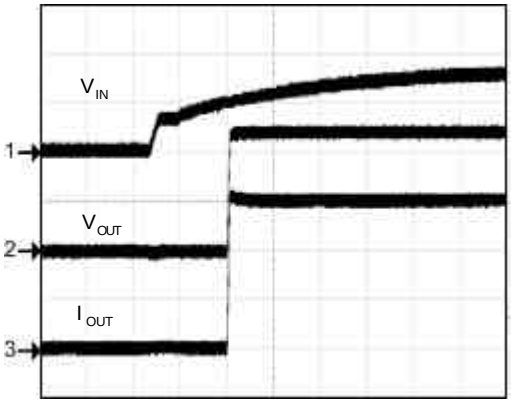
CH1 : V_{OUT}, 500mV/div
CH2 : $V_{\overline{SHDN}}$, 5V/div
CH3 : I_{OUT}, 200mA/div
Time : 50µs/div

Shutdown



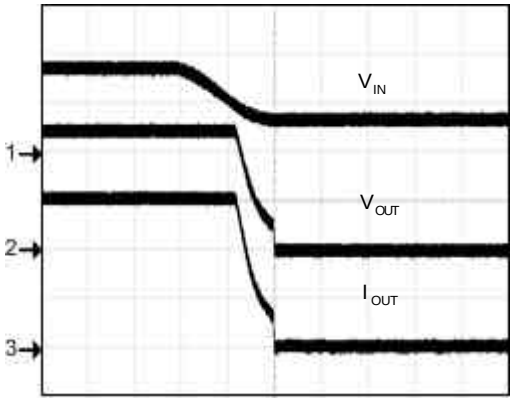
CH1 : V_{OUT}, 500mV/div
CH2 : $V_{\overline{SHDN}}$, 5V/div
CH3 : I_{OUT}, 200mA/div DC
Time : 10µs/div

Power on



CH1 : V_{IN}, 2V/div
CH2 : V_{OUT}, 500mV/div
CH3 : I_{OUT}, 100mA/div
Time : 200µs/div

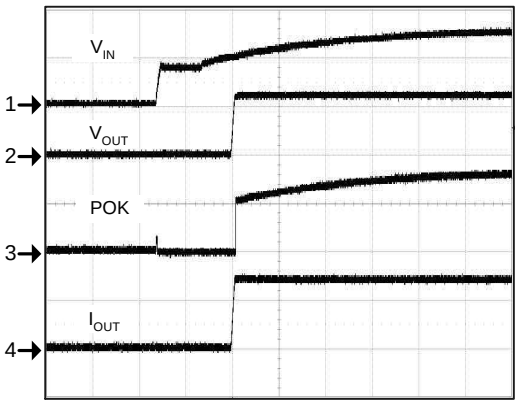
Power off



CH1 : V_{IN}, 2V/div
CH2 : V_{OUT}, 500mV/div,
CH3 : I_{OUT}, 100mA/div
Time : 50ms/div

Operating Waveforms (Cont.)

POK

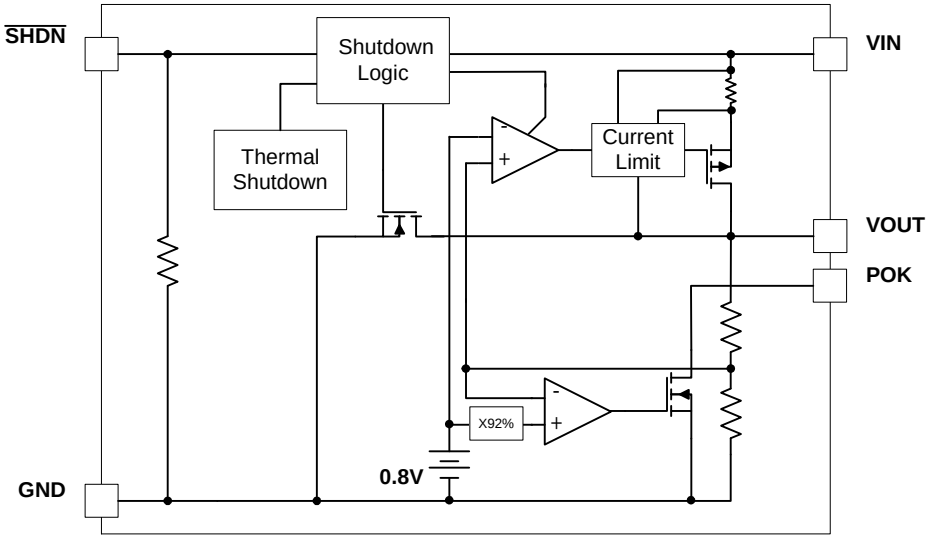


CH1 : V_{IN}, 2V/div
CH2 : V_{OUT}, 1V/div,
CH3 : P_{OK}, 2V/div
CH4 : I_{OUT}, 200mA/div
Time : 1ms/div

Pin Description

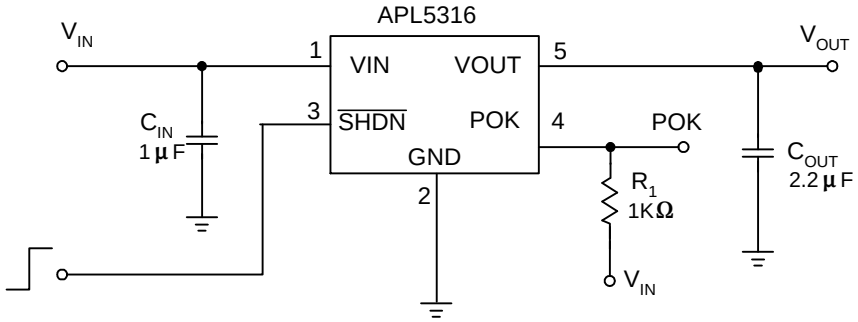
PIN		FUNCTION
No	NAME	
1	VIN	Voltage supply input pin
2	GND	Ground pin
3	$\overline{SHDN}$	Shutdown control pin, logic high: enable; logic low: shutdown
4	POK	Power-ok signal output pin
5	VOUT	Regulator output pin

Block Diagram



Typical Application Circuit

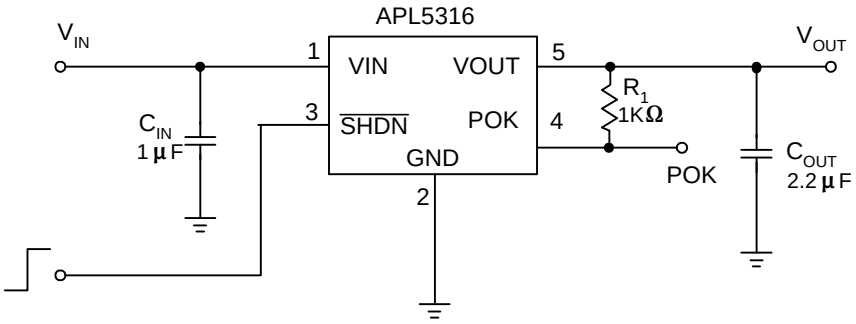
1



2.2µF/GRM155R60J225M Murata

Typical Application Circuit (Cont.)

2.



Function Description

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up. The typical soft-start interval is about 60μs.

Power-ok (POK)

The APL5316 indicates the status of the output voltage. As the V_{OUT} rises and reaches the Power-ok threshold (V_{POK}), the IC turns off the internal NMOS of the POK to indicate the output is ok. As the V_{OUT} falls and reaches the falling Power-ok threshold (V_{PNOK}), the IC immediately turns on the NMOS of the POK to indicate the output is not ok. The resistance of the resistor R1 connected from V_{OUT} to POK or V_{IN} to POK should be in the range from 1K to 50K.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5316. When the junction temperature exceeds +160°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C. The thermal shutdown is designed with a 40°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, the device power dissipation should be externally limited by the design to keep the junction temperature below 125°C.

Shutdown Control

The APL5316 has an active-low shutdown function. Forcing $\overline{SHDN}$ high (>1.6V) enables the V_{OUT}; forcing $\overline{SHDN}$ low (<0.4V) disables the V_{OUT}. $\overline{SHDN}$ is internally pulled low by a resistor (3MΩ typical). If shutdown control is not necessary, please connect $\overline{SHDN}$ pin to VIN for normal operation.

Application Information

Input Capacitor

The APL5316 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, it is recommeded to place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1µF and a minimum ceramic capacitor of 1µF is necessary.

Output Capacitor

The APL5316 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 2.2µF. With X5R and X7R dielectrics, 2.2µF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, however, it also affects power on issue. Equation (1) shows the relationship between the maximum C_{OUT} value and V_{OUT}.

$$C_{OUT(max)} = 31 - \frac{6}{V_{OUT}} \quad \text{.....(1)}$$

Where the unit of C_{OUT} is µF and V_{OUT} is V. Figure 1 shows the curve of maximum output capacitor over the output voltage. The output voltage range is from 0.8 to 5.5V and the output capacitor value should be under the line. Output capacitors must be placed at the load and ground pin as close as possible and the impedance of the layout must be minimized.

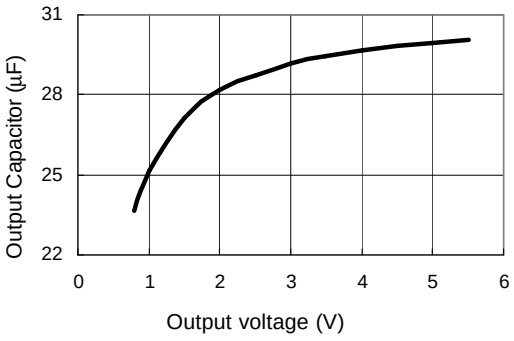


Figure 1

Operation Region and Power dissipation

The APL5316 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(160-25)/240$$
$$= 0.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125 °C. The calculated power dissipation should be less than:

$$P_D=(125-25)/240$$
$$= 0.41(W)$$

The GND provides an electrical connection to ground and channels heat away. Connect the GND to ground by using a large pad or ground plane.

Layout Consideration

Figure 2 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5316 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.

Application Information (Cont.)

PCB Layout Consideration (Cont.)

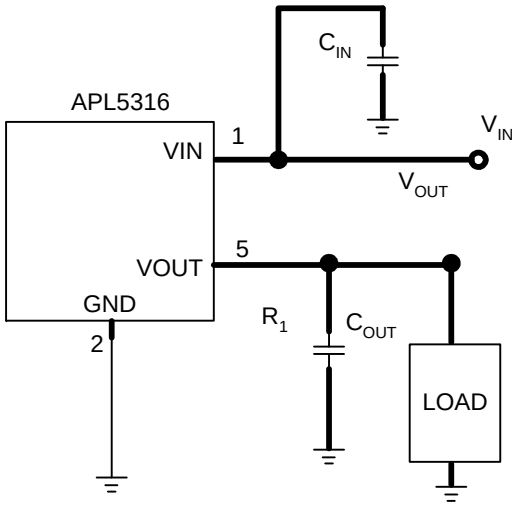
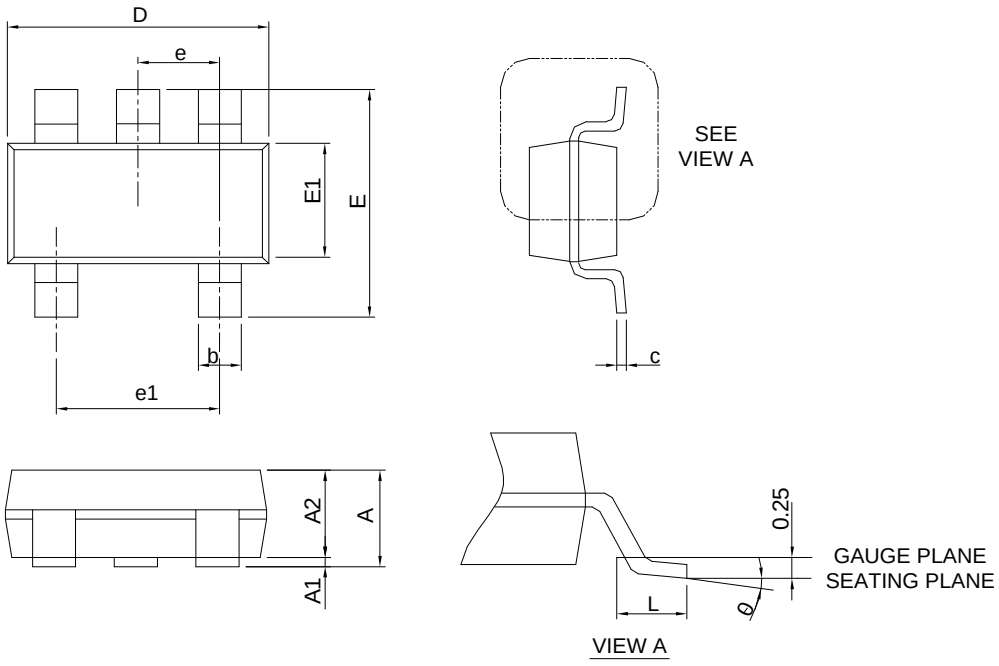


Figure 2

Package Information

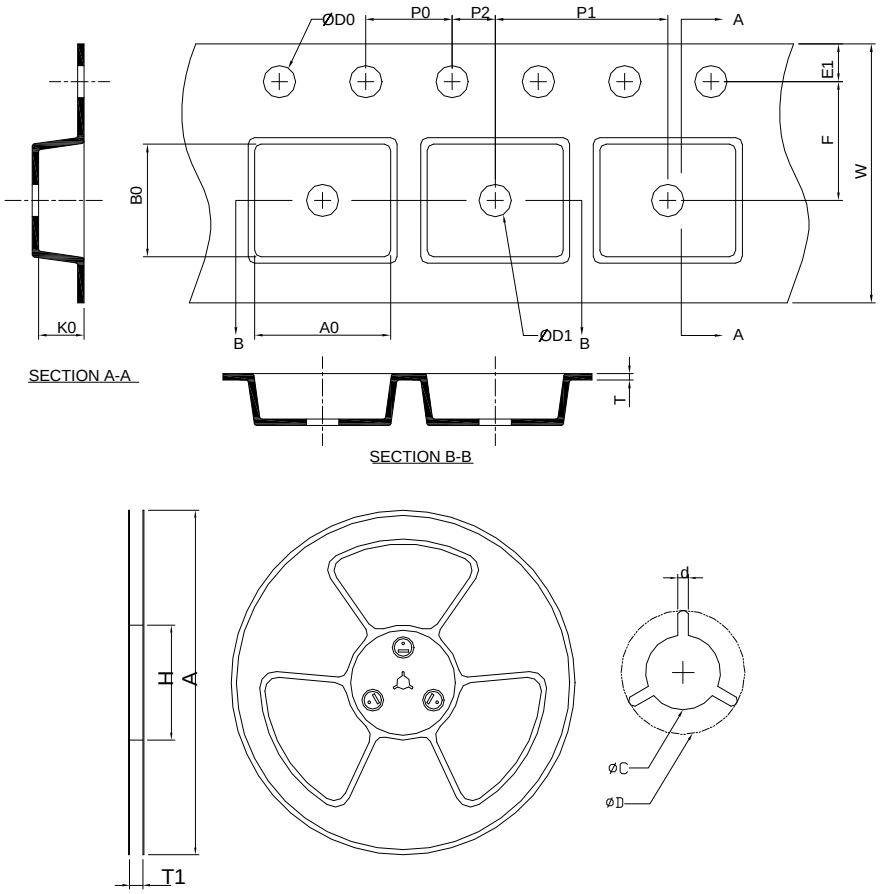
SOT-23-5



SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

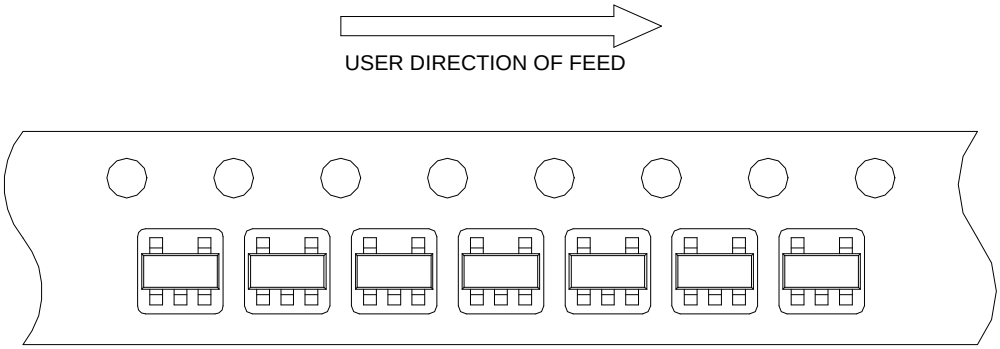
(mm)

Devices Per Reel

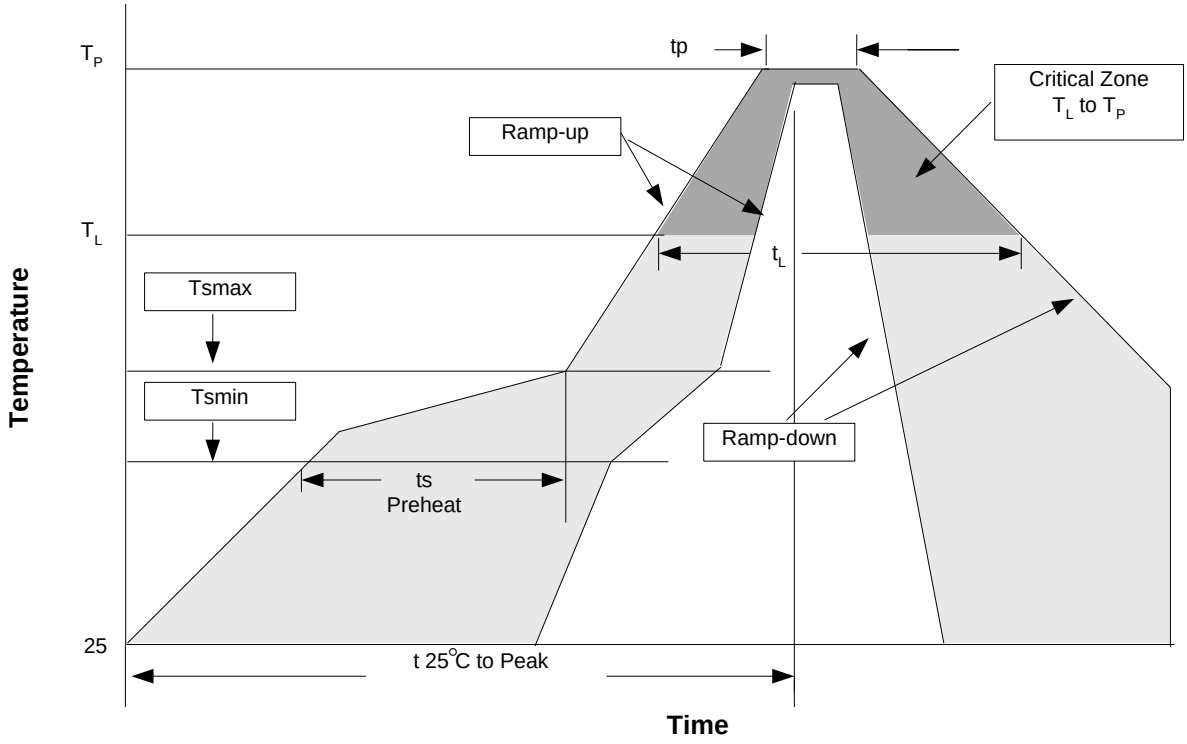
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000

Taping Direction Information

SOT-23-5



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

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