# IBM

**Preliminary**

**128K x 36 & 256K x 18 SRAM**

## Features

- 128K x 36 or 256K x 18 Organizations

- CMOS Technology

- Synchronous Pipeline Mode Of Operation with Self-Timed Late Write

- Single Differential HSTL Clock

- +3.3V Power Supply, Ground, $V_{DDQ}$ & $V_{REF}$

- HSTL Input and Output levels,

- Registered Addresses, Write Enables, Synchronous Select and Data Ins.

- Registered Outputs

- Common I/O

- Asynchronous Output Enable and Power Down Inputs

- Boundary Scan using limited set of JTAG 1149.1 functions

- Byte Write Capability & Global Write Enable

- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order.

## Description

The IBM041841QLAD and IBM043641QLAD 4Mb SRAMs are Synchronous Pipeline Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 4.0ns cycle times. Dual differential K clocks are used to initiate the read/write operation, and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. These chips operate with a +3.3V power supply, have a 1.5V output power supply, and are compatible with HSTL I/O interfaces.

## x36 BGA Bump Layout (Top View)

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DQ}$ | SA5 | SA7 | NC | SA16 | SA14 | $V_{DDQ}$ |
| **B** | NC | NC | SA8 | NC | SA11 | NC | NC |
| **C** | NC | SA6 | SA9 | $V_{DD}$ | SA10 | SA15 | NC |
| **D** | DQc18 | DQc19 | $V_{SS}$ | ZQ | $V_{SS}$ | DQb10 | DQb9 |
| **E** | DQc20 | DQc21 | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | DQb12 | DQb11 |
| **F** | $V_{DDQ}$ | DQc22 | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQb13 | $V_{DDQ}$ |
| **G** | DQc23 | DQc24 | $\overline{SBWc}$ | NC | $\overline{SBWb}$ | DQb15 | DQb14 |
| **H** | DQc25 | DQc26 | $V_{SS}$ | NC | $V_{SS}$ | DQb17 | DQb16 |
| **J** | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| **K** | DQd34 | DQd35 | $V_{SS}$ | K | $V_{SS}$ | DQa8 | DQa7 |
| **L** | DQd32 | DQd33 | $\overline{SBWd}$ | $\overline{K}$ | $\overline{SBWa}$ | DQa6 | DQa5 |
| **M** | $V_{DDQ}$ | DQd31 | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | DQa4 | $V_{DDQ}$ |
| **N** | DQd29 | DQd30 | $V_{SS}$ | SA0 | $V_{SS}$ | DQa3 | DQa2 |
| **P** | DQd27 | DQd28 | $V_{SS}$ | SA1 | $V_{SS}$ | DQa1 | DQa0 |
| **R** | NC | SA4 | M1* | $V_{DD}$ | M2* | SA12 | NC |
| **T** | NC | NC | SA3 | SA2 | SA13 | NC | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to $V_{SS}$ and $V_{DD}$, respectively.

## x18 BGA Bump Layout (Top View)

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | SA5 | SA7 | NC | SA16 | SA14 | $V_{DDQ}$ |
| **B** | NC | NC | SA8 | NC | SA11 | NC | NC |
| **C** | NC | SA6 | SA9 | $V_{DD}$ | SA10 | SA15 | NC |
| **D** | DQb9 | NC | $V_{SS}$ | ZQ | $V_{SS}$ | DQa1 | NC |
| **E** | NC | DQb12 | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | DQa2 |
| **F** | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQa4 | $V_{DDQ}$ |
| **G** | NC | DQb15 | $\overline{SBWb}$ | NC | VSS | NC | DQa5 |
| **H** | DQb16 | NC | $V_{SS}$ | NC | $V_{SS}$ | DQa8 | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | DQb17 | $V_{SS}$ | K | $V_{SS}$ | NC | DQa7 |
| **L** | DQb14 | NC | $V_{SS}$ | $\overline{K}$ | $\overline{SBWa}$ | DQa6 | NC |
| **M** | $V_{DDQ}$ | DQb13 | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| **N** | DQb11 | NC | $V_{SS}$ | SA0 | $V_{SS}$ | DQa3 | NC |
| **P** | NC | DQb10 | $V_{SS}$ | SA1 | $V_{SS}$ | NC | DQa0 |
| **R** | NC | SA4 | M1 | $V_{DD}$ | M2 | SA13 | NC |
| **T** | NC | SA2 | SA3 | NC | SA17 | SA12 | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to $V_{SS}$ and $V_{DD}$ respectively.

## Pin Description

| | | | |
|---|---|---|---|
| SA0-SA17 | Address Input | $\overline{G}$ | Asynchronous Output Enable |
| DQ0-DQ35 | Data I/O | $\overline{SS}$ | Synchronous Select |
| K, $\overline{K}$ | Differential Input Register Clocks | M1, M2 | Clock Mode Inputs - Selects Single or Dual Clock Operation. |
| $\overline{SW}$ | Write Enable, Global | $V_{REF}$(2) | HSTL Input Reference Voltage |
| $\overline{SBWa}$ | Write Enable, Byte a (DQ0-DQ8) | $V_{DD}$ | Power Supply (+3.3V) |
| $\overline{SBWb}$ | Write Enable, Byte b (DQ9-DQ17) | $V_{SS}$ | Ground |
| $\overline{SBWc}$ | Write Enable, Byte c (DQ18-DQ26) | $V_{DDQ}$ | Output Power Supply |
| $\overline{SBWd}$ | Write Enable, Byte d (DQ27-DQ35) | ZZ | Asynchronous Sleep Mode |
| TMS,TDI,TCK | IEEE 1149.1 Test Inputs (LVTTL levels) | ZQ | Output Driver Impedance Control |
| TDO | IEEE 1149.1 Test Output (LVTTL level) | NC | No Connect |

## Block Diagram
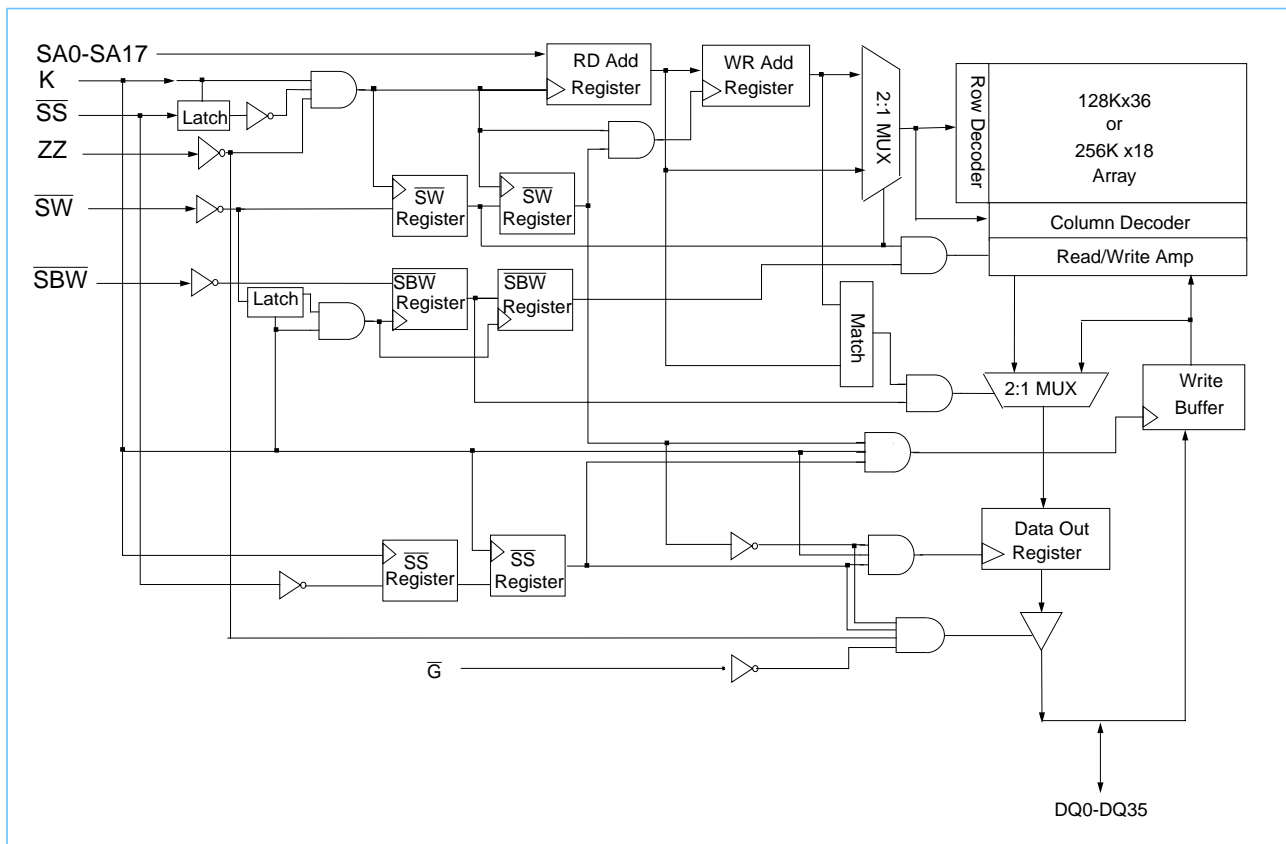
## SRAM Features

### Late Write

Late Write function allows for write data to be registered one cycle after addresses and controls. This feature will alleviate SRAM data bus contention going from a Read to Write cycle by eliminating one dead cycle. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte by byte basis. When only one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

### Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM supports Single Clock, Pipeline (M1 = $V_{SS}$, M2 = $V_{DD}$). This data sheet only describes Single Clock Pipeline functionality. Mode control inputs must be set with power up and must not change during SRAM operation.This Sram is tested only in the Pipeline mode.

### Power Down Mode

Power Down Mode or "Sleep" Mode is enabled by switching asynchronous signal ZZ High When powering the SRAM down inputs should be dropped first followed by $V_{REF}$ then $V_{DDQ}$; $V_{DD}$ must be dropped last. $V_{DDQ}$ can be simultaneously dropped with $V_{DD}$.

### Programmable Impedance / Power Up Requirements

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and $V_{SS}$ to allow for the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time towards the optimum level. The output driver has 32 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore, triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K Clock to guarantee the proper update. Power up requirements for the SRAM are that $V_{DD}$ must be powered before or simultaneously with $V_{DDQ}$ followed by $V_{REF}$; inputs should be powered last. The limitation on $V_{DDQ}$ is that it must not exceed $V_{DD}$ by more than 0.4V during power up. In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 4µs of power-up time after $V_{DD}$ reaches its operating range.To guarantee optimum output driver impedance after power up, the SRAM needs 2080 clock cycles followed by a single Low-Z to High-Z transition at the end of 2080 cycles.

### Sleep Mode Operation

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin HIGH. During sleep mode, all other inputs are ignored and outputs are brought to a High-Z state. Sleep mode current and output High Z are guaranteed after the specified sleep mode enable time. During sleep mode, the array data contents are pre-

served. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Sense amp data is lost. Normal operation can be resumed by bringing ZZ low, but only after specified sleep mode recovery time.

## Ordering Information

| Part Number | Organization | Speed | Leads |
|---|---|---|---|
| IBM041841QLAD-4 (Rev D) | 256K x 18 | 2.1ns Access / 4.0 ns Cycle | 7 x 17 PBGA |
| IBM041841QLAD-5 (Rev D) | 256K x 18 | 2.5ns Access / 5 ns Cycle | 7 x 17 PBGA |
| IBM041841QLAD-6 (Rev D) | 256K x 18 | 3.0ns Access / 6ns Cycle | 7 x 17 PBGA |
| IBM041841QLAD-7 (Rev D) | 256K x 18 | 3.5ns Access / 7ns Cycle | 7 x 17 PBGA |
| IBM043641QLAD-4 (Rev D) | 128K x 36 | 2.1ns Access / 4.0 ns Cycle | 7 x 17 PBGA |
| IBM043641QLAD-4N (Rev D) | 128K x 36 | 2.25ns Access / 4.3 ns Cycle | 7 x 17 PBGA |
| IBM043641QLAD-5 (Rev D) | 128K x 36 | 2.5ns Access / 5 ns Cycle | 7 x 17 PBGA |
| IBM043641QLAD-6 (Rev D) | 128K x 36 | 3.0ns Access / 6ns Cycle | 7 x 17 PBGA |
| IBM043641QLAD-7 (Rev D) | 128K x 36 | 3.5ns Access / 7ns Cycle | 7 x 17 PBGA |

## Clock Truth Table

| K | ZZ | $\overline{SS}$ | $\overline{SW}$ | $\overline{SBWa}$ | $\overline{SBWb}$ | $\overline{SBWc}$ | $\overline{SBWd}$ | DQ (n) | DQ (n+1) | MODE |
|---|----|------|------|--------|--------|--------|--------|--------|----------|------|
| L→H | L | L | H | X | X | X | X | X | $D_{OUT}$ 0-35 | Read Cycle All Bytes |
| L→H | L | L | L | L | H | H | H | X | $D_{IN}$ 0-8 | Write Cycle 1st Byte |
| L→H | L | L | L | H | L | H | H | X | $D_{IN}$ 9-17 | Write Cycle 2nd Byte |
| L→H | L | L | L | H | H | L | H | X | $D_{IN}$ 18-26 | Write Cycle 3rd Byte |
| L→H | L | L | L | H | H | H | L | X | $D_{IN}$ 27-35 | Write Cycle 4th Byte |
| L→H | L | L | L | L | L | L | L | X | $D_{IN}$ 0-35 | Write Cycle All Bytes |
| L→H | L | L | L | H | H | H | H | X | High-Z | Abort Write Cycle |
| L→H | L | H | X | X | X | X | X | X | High-Z | Deselect Cycle |
| X | H | X | X | X | X | X | X | High-Z | High-Z | Sleep Mode |

## Output Enable Truth Table

| Operation | $\overline{G}$ | DQ |
|-----------|-----|-----|
| Read | L | $D_{OUT}$ 0-35 |
| Read | H | High-Z |
| Sleep (ZZ=H) | X | High-Z |
| Write ($\overline{SW}$=L) | X | High-Z |
| Deselect ($\overline{SS}$=H) | X | High-Z |

## Absolute Maximum Ratings

| Item | Symbol | Rating | Units | Notes |
|------|--------|--------|-------|-------|
| Power Supply Voltage | $V_{DD}$ | -0.5 to 3.9 | V | 1 |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 | V | 1 |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DD}$+0.5 | V | 1 |
| Output Power Supply Voltage | $V_{DDQ}$ | $V_{DD}$ | V | 1 |
| Operating Temperature | $T_J$ | 0 to +110 | °C | 1 |
| Storage Temperature | $T_{STG}$ | -55 to +125 | °C | 1 |
| Short Circuit Output Current | $I_{OUT}$ | 25 | mA | 1 |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions ($T_A$=0 to 85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.135 | 3.3 | 3.63 | V | 1 |
| Output Driver Supply Voltage | $V_{DDQ}$ | 1.4 | 1.5 | 1.6 | V | 1 |
| Input High Voltage | $V_{IH}$ | $V_{REF}$ +0.1 | — | $V_{DDQ}$ + 0.3 | V | 1, 2 |
| Input Low Voltage | $V_{IL}$ | -0.3 | — | $V_{REF}$ -0.1 | V | 1, 3 |
| Input Reference Voltage | $V_{REF}$ | 0.68 | 0.75 | 0.90 | V | 1, 6 |
| Clocks Signal Voltage | $V_{IN - CLK}$ | -0.3 | — | $V_{DDQ}$ + 0.3 | V | 1, 4 |
| Differential Clocks Signal Voltage | $V_{DIF - CLK}$ | 0.1 | — | $V_{DDQ}$ + 0.6 | V | 1, 5 |
| Clocks Common Mode Voltage | $V_{CM - CLK}$ | 0.55 | — | 0.90 | V | 1 |
| Output Current | $I_{OUT}$ | — | 5 | 8 | mA | |

1. All voltages referenced to $V_{SS}$. All $V_{DD}$, $V_{DDQ}$ and $V_{SS}$ pins must be connected.
2. $V_{IH}$(Max)DC = $V_{DDQ}$ + 0.3 V, $V_{IH}$(Max)AC = $V_{DD}$ + 1.5 V (pulse width ≤ 4.0ns).
3. $V_{IL}$(Min)DC = - 0.3 V, $V_{IL}$(Min)AC= -1.5 V (pulse width ≤ 4.0ns).
4. $V_{IN-CLK}$ specifies the maximum allowable DC excursions of each differential clock (K, $\overline{K}$).
5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching.
6. Peak to Peak AC component superimposed on $V_{REF}$ may not exceed 5% of $V_{REF}$.

## DC Electrical Characteristics ($T_A$= 0 to +85°C, $V_{DD}$=3.3V -5%/+10%, $V_{DDQ}$ = 1.5V)

| Parameter | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| Average Power Supply Operating Current- x36 ($I_{OUT}$ = 0, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, ZZ & $\overline{SS}$ = $V_{IL}$) | $I_{DD4}$ $I_{DD4.3}$ $I_{DD5}$ $I_{DD6}$ $I_{DD7}$ | — — | 760 715 650 575 525 | mA | 1 |
| Average Power Supply Operating Current - x18 ($I_{OUT}$ = 0, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, ZZ & $\overline{SS}$ = $V_{IL}$) | $I_{DD4}$ $I_{DD5}$ $I_{DD6}$ $I_{DD7}$ | — — | 715 600 525 500 | mA | 1 |
| Power Supply Standby Current (ZZ= $V_{IH}$, All other inputs = $V_{IH}$ or $V_{IL}$, $I_{OUT}$ = 0) | $I_{SBZZ}$ | — | 150 | mA | 1 |
| ($\overline{SS}$=$V_{IH}$, ZZ=$V_{IL}$. All their inputs = $V_{IH}$ or $V_{IL}$, $I_{OUT}$= 0) | $I_{SBSS}$ | | 200 | mA | 1 |
| Input Leakage Current, any input ($V_{IN}$ = $V_{SS}$ or $V_{DD}$) | $I_{LI}$ | — | +1 | μA | |
| Output Leakage Current ($V_{OUT}$ = $V_{SS}$ or $V_{DD}$, DQ in High-Z) | $I_{LO}$ | — | +1 | μA | |
| Output "High" Level Voltage ($I_{OH}$=-6mA @ $V_{DDQ}$ / 2 + 0.3) | $V_{OH}$ | $V_{DDQ}$ -.4 | $V_{DDQ}$ | V | 2 |
| Output "Low" Level Voltage ($I_{OL}$=+6mA @ $V_{DDQ}$ / 2 - 0.3) | $V_{OL}$ | Vss | $V_{SS+.4}$ | V | 2 |

1. $I_{OUT}$ = Chip Output Current. $I_{DD4}$ means current at 4ns cycle time for example.
2. Minimum Impedance Output Driver.

## PBGA Thermal Characteristics

| Item | Symbol | Rating | Units |
|------|--------|--------|-------|
| Thermal Resistance Junction to Case | R$\Theta$JC | 1 | °C/W |

## PBGA Capacitance  ($T_A$=0 to + 85°C, $V_{DD}$=3.3V -5%/+10%, f=1MHz)

| Parameter | Symbol | Test Condition | Max | Units |
|-----------|--------|----------------|-----|-------|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | 4 | pF |
| Data I/O Capacitance (DQ0-DQ35) | $C_{OUT}$ | $V_{OUT}$ = 0V | 5 | pF |

## AC Input Characteristics

| Item | Symbol | Min | Max | Notes |
|------|--------|-----|-----|-------|
| AC Input Logic High (Volts) | $V_{IH}$ (ac) | $V_{REF}$+0.4 | | 3 |
| AC Input Logic Low (Volts) | $V_{IL}$ (ac) | | $V_{REF}$-0.4 | 3 |
| Clock Input Differential Voltage (Volts) | $V_{DIF}$ (ac) | 0.4 | | 2 |
| $V_{REF}$ Peak to Peak ac Voltage (Volts) | $V_{REF}$ (ac) | | 5% $V_{REF}$ (dc) | 1 |

1. The peak to peak AC component superimposed on $V_{REF}$ may not exceed 5% of the DC component of $V_{REF}$. Implies very stable signal. Sourcing from $V_{DDQ}$ not recommended. Separate board plane recommended. Do not use noisy signal line.
2. Performance is a function on $V_{IH}$ and $V_{IL}$ levels to clock inputs.
3. AC Input Definition on page 8.

## AC Input Definition
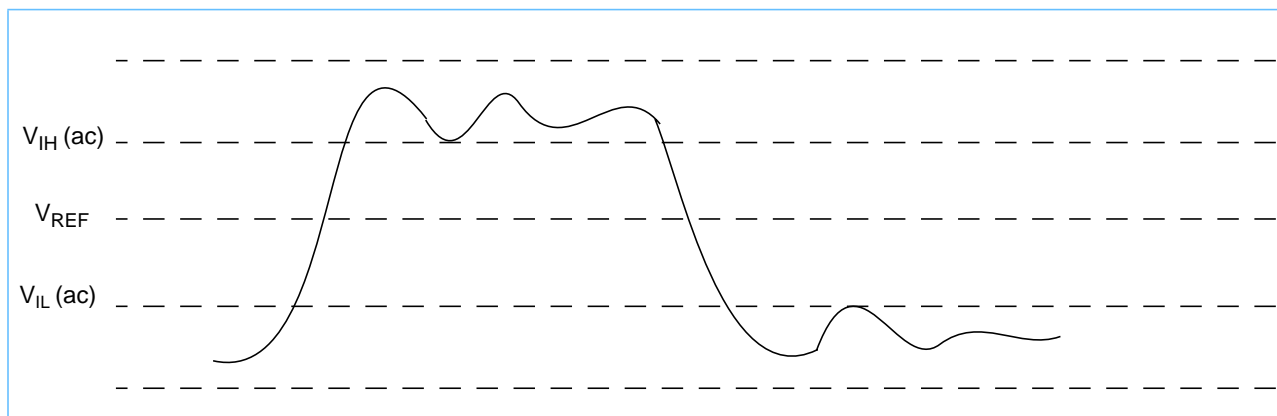
## Programmable Impedance Output Driver DC Electrical Characteristics ($T_A$= 0 to +85°C, $V_{DD}$=3.3V -5%/+10%)

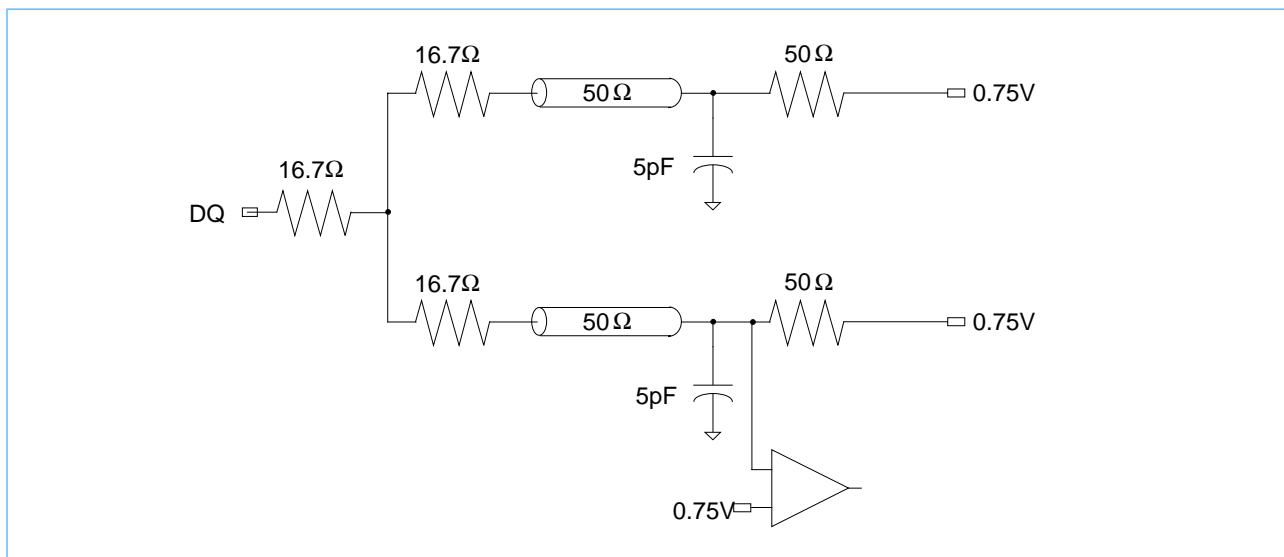| Parameter | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| Output "High" Level Voltage | $V_{OH}$ | $V_{DDQ} / 2$ | $V_{DDQ}$ | V | 1 |
| Output "Low" Level Voltage | $V_{OL}$ | $V_{SS}$ | $V_{DDQ/2}$ | V | 2 |

1. $I_{OH} = (V_{DDQ} / 2) / (RQ / 5) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $150\Omega \leq RQ \leq 350\Omega$.
2. $I_{OL} = (V_{DDQ} / 2) / (RQ / 5)$ 15% @ $V_{OL} = V_{DDQ} / 2$ For: $150\Omega \leq RQ \leq 350\Omega$.

## AC Test Conditions ($T_A$=0 to +85°C, $V_{DD}$=3.3V - 5%/+10%, $V_{DDQ}$ =1.5V)

| Parameter | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| Input High Level | $V_{IH}$ | 1.25 | V | |
| Input Low Level | $V_{IL}$ | 0.25 | V | |
| Input Reference Voltage | $V_{REF}$ | 0.75 | V | |
| Differential Clocks Voltage | $V_{DIF-CLK}$ | 0.75 | V | |
| Clocks Common Mode Voltage | $V_{CM-CLK}$ | 0.75 | V | |
| Input Rise Time | $T_R$ | 0.5 | ns | |
| Input Fall Time | $T_F$ | 0.5 | ns | |
| I/O Signals Reference Level (except K, C Clocks) | | 0.75 | V | |
| Clocks Reference Level | | Differential Cross Point | V | |
| Output Load Conditions | | | | 1 |

1. See AC Test Loading figure on page 9.

## AC Test Loading

## AC Characteristics (T$_A$=0 to 85°C, V$_{DD}$=3.3V -5%/+10%, V$_{DDQ}$=1.5V)

| Parameter | Symbol | -4 | | -4N (X36 Only) | | -5 | | -6 | | -7 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Cycle Time | t$_{KHKH}$ | 4.0 | — | 4.3 | — | 5 | — | 6.0 | — | 7.0 | — | ns | |
| Clock High Pulse Width | t$_{KHKL}$ | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | |
| Clock Low Pulse Width | t$_{KLKH}$ | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | |
| Clock to Output Valid | t$_{KHQV}$ | — | 2.1 | — | 2.25 | — | 2.5 | — | 3.0 | — | 3.5 | ns | 1 |
| Address Setup Time | t$_{AVKH}$ | 0.4 | — | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 4, 6 |
| Address Hold Time | t$_{KHAX}$ | 0.75 | — | 0.75 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | 4 |
| Sync Select Setup Time | t$_{SVKH}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 4 |
| Sync Select Hold Time | t$_{KHSX}$ | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | 4 |
| Write Enables Setup Time | t$_{WVKH}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 4 |
| Write Enables Hold Time | t$_{KHWX}$ | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | 4 |
| Data In Setup Time | t$_{DVKH}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 4 |
| Data In Hold Time | t$_{KHDX}$ | 0.75 | — | 0.75 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | 4 |
| Data Out Hold Time | t$_{KHQX}$ | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | ns | 1, 5 |
| Clock High to Output High-Z | t$_{KHQZ}$ | — | 2.5 | — | 2.5 | — | 2.5 | — | 3.0 | — | 3.5 | ns | 1, 2 |
| Clock High to Output Active | t$_{KHQX4}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 1, 2 |
| Output Enable to High-Z | t$_{GHQZ}$ | — | 2.5 | — | 2.5 | — | 2.5 | | 3.0 | — | 3.5 | ns | 1, 2 |
| Output Enable to Low-Z | t$_{GLQX}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 1, 2 |
| Output Enable to Output Valid | t$_{GLQV}$ | — | 2.5 | — | 2.5 | — | 2.5 | — | 3.0 | — | 3.5 | ns | 1 |
| Output Enable Set-up Time | t$_{GHKH}$ | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns | 1, 3 |
| Output Enable Hold TIme | t$_{KHGX}$ | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | 1, 3 |
| Sleep Mode Recovery TIme | t$_{ZZR}$ | 4 | — | 4.3 | — | 5 | — | 6 | — | 7 | — | ns | |
| Sleep Mode Enable TIme | t$_{ZZE}$ | — | 4 | — | 4.3 | — | 5 | — | 6 | — | 7 | ns | |

1. See AC Test Loading figure on page 9.
2. Verified by design and tested without guardband
3. Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and Deselect cycles will also induce Output Driver updates during High-Z.
4. In use conditions V$_{IH}$,V$_{IL}$,Trise, Tfall of inputs must be within 20% of V$_{IH}$, V$_{IL}$, Trise, Tfall of Clock.
5. Verified by design to 0.6ns. Strobed at 0.6ns for -4 and -4N sort, 0.7 for others.
6. For the -4 & 4N sort, this spec is verified by design to 0.4ns. Strobed at 0.3ns
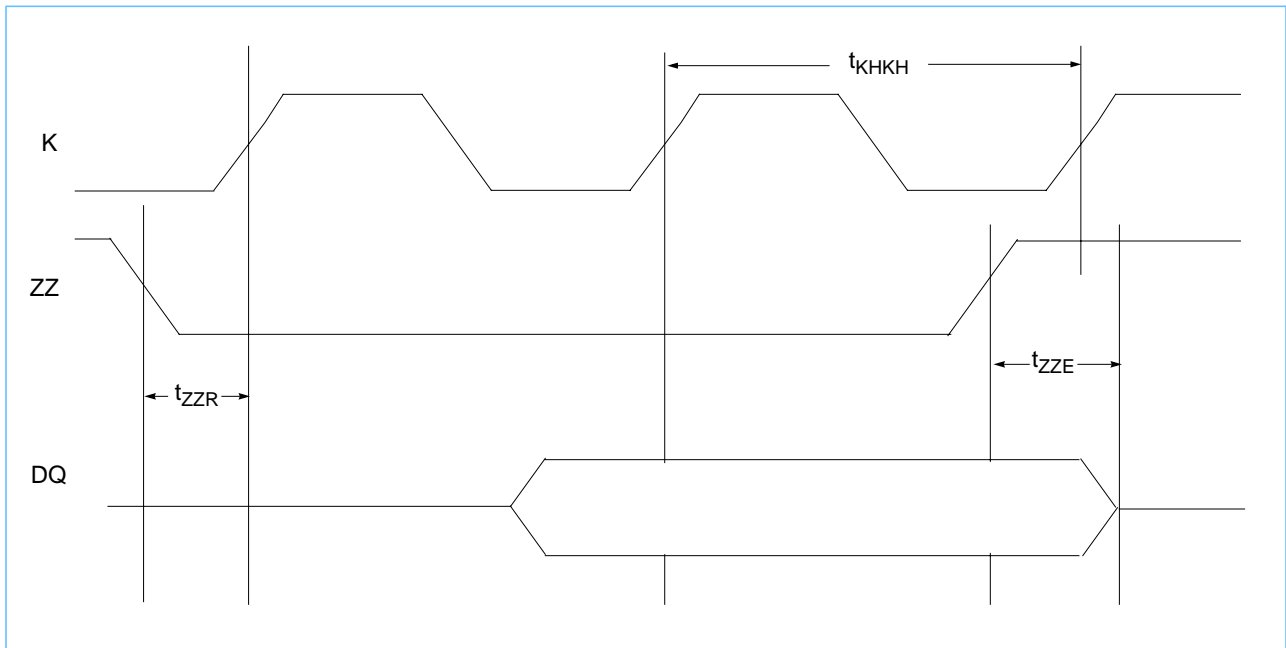
## Timing Diagram (Read and Deselect Cycles)
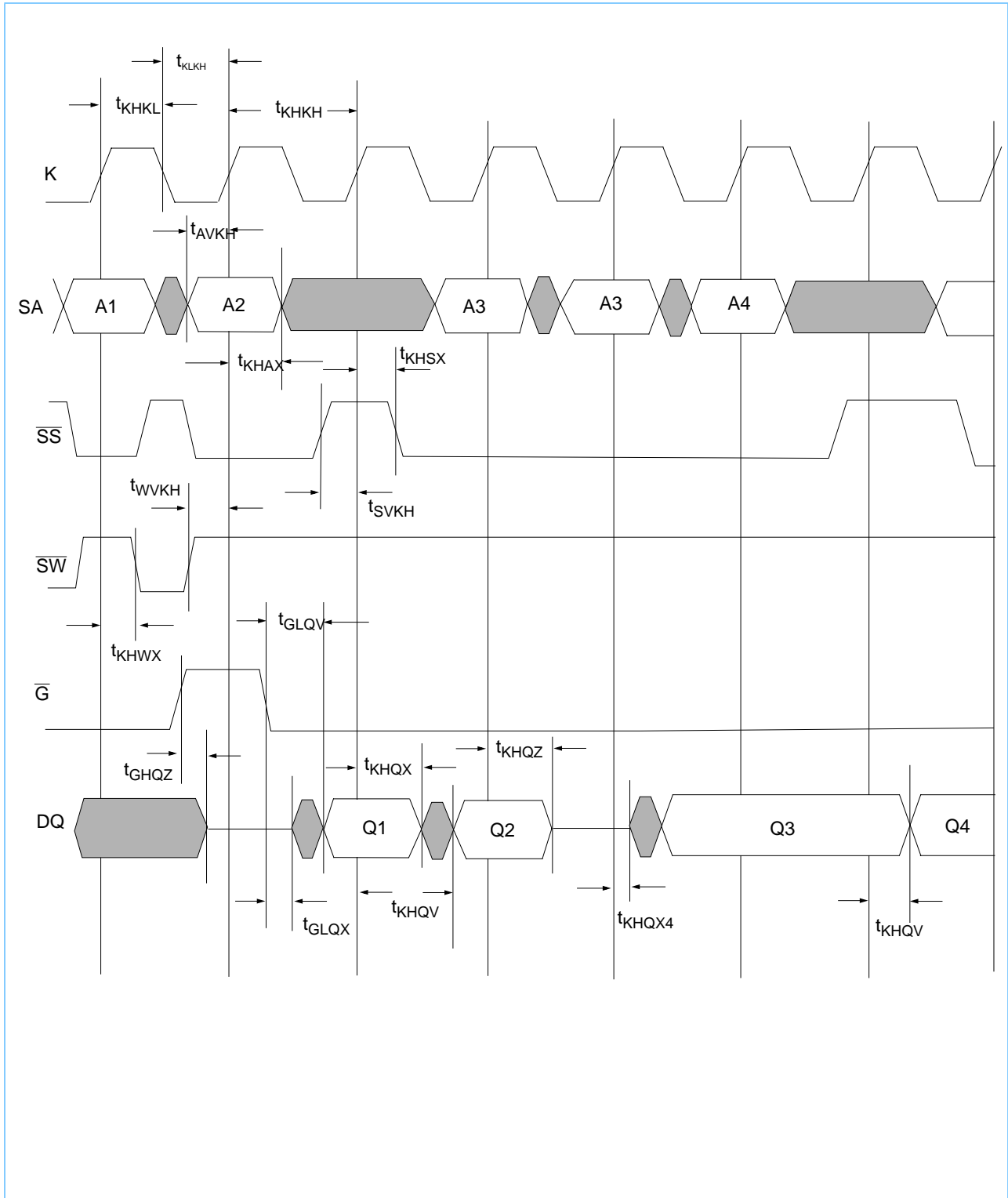
## Timing Diagram (Read Write Cycles)
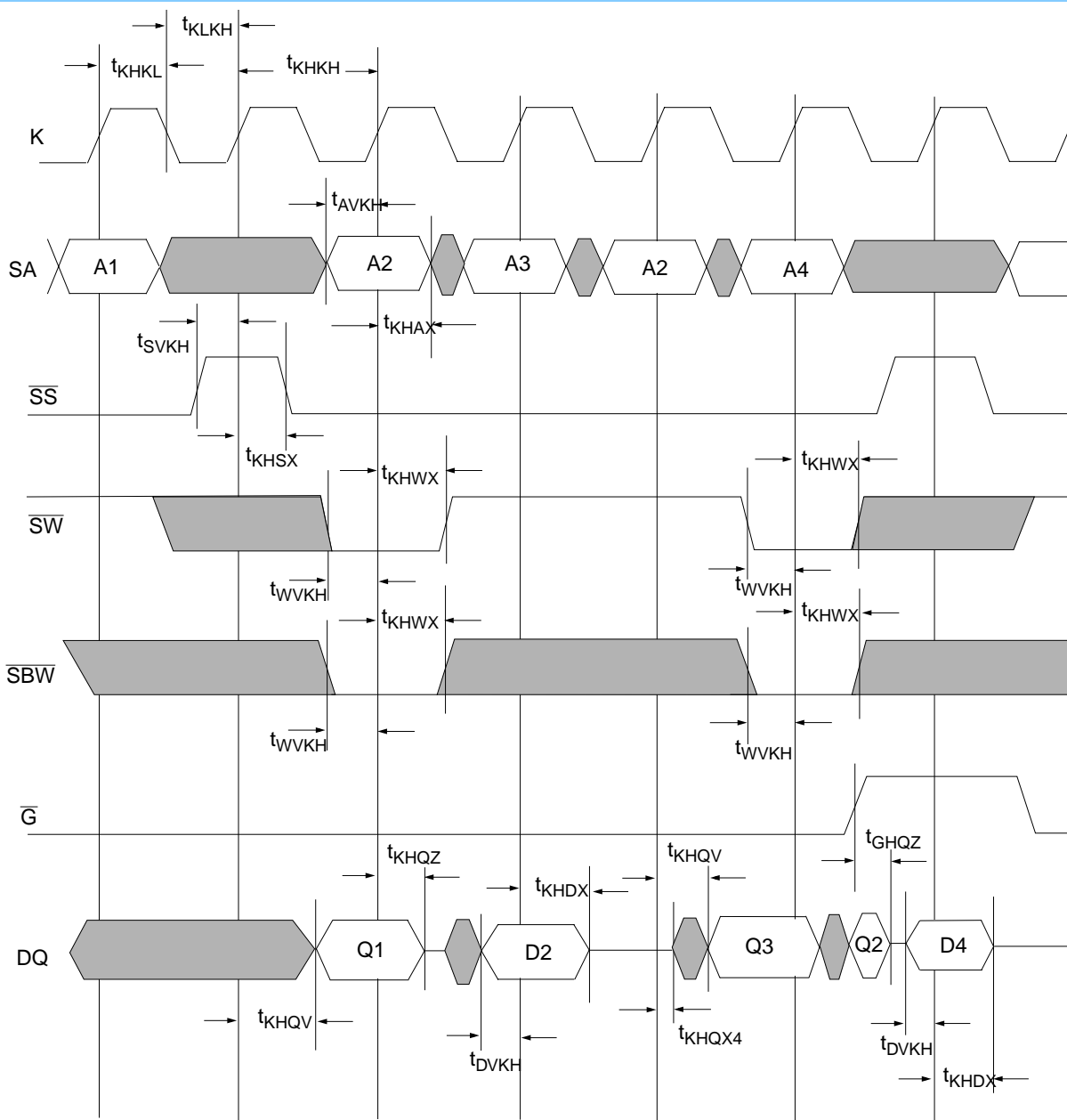


**NOTES:**

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

## Timing Diagram (Sleep Mode)

## IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/O and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

> **Caution:** TCK,TMS,TDI must be tied down, even if JTAG is not used. TCK tied off will not allow any data to be clocked in, however.

**JTAG Recommended DC Operating Conditions** ($T_A$=0 to 85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| JTAG Input High Voltage | $V_{IH1}$ | 2.2 | — | $V_{DD}$+0.3 | V | 1 |
| JTAG Input Low Voltage | $V_{IL1}$ | -0.3 | — | 0.8 | V | 1 |
| JTAG Output High Level | $V_{OH1}$ | 2.4 | — | — | V | 1, 2 |
| JTAG Output Low Level | $V_{OL1}$ | — | — | 0.4 | V | 1, 3 |

1. All JTAG Inputs/Outputs are LVTTL Compatible only.
2. $I_{OH1}$ = -8mA at 2.4V.
3. $I_{OL1}$ = +8mA at 0.4V.

**JTAG AC Test Conditions** ($T_A$=0 to +85°C, $V_{DD}$=3.3V ±5%)

| Parameter | Symbol | Conditions | Units | Notes |
|---|---|---|---|---|
| Input Pulse High Level | $V_{IH1}$ | 3.0 | V | |
| Input Pulse Low Level | $V_{IL1}$ | 0.0 | V | |
| Input Rise Time | $T_{R1}$ | 2.0 | ns | |
| Input Fall Time | $T_{F1}$ | 2.0 | ns | |
| Input and Output Timing Reference Level | | 1.5 | V | 1 |

1. See AC Test Loading on page 9.

## JTAG AC Characteristics ($T_A$=0 to +85°C, $V_{DD}$=3.3V -5%/+10%)

| Parameter | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| TCK Cycle Time | $t_{THTH}$ | 20 | — | ns | |
| TCK High Pulse Width | $t_{THTL}$ | 7 | — | ns | |
| TCK Low Pulse Width | $t_{TLTH}$ | 7 | — | ns | |
| TMS Setup | $t_{MVTH}$ | 4 | — | ns | |
| TMS Hold | $t_{THMX}$ | 4 | — | ns | |
| TDI Setup | $t_{DVTH}$ | 4 | — | ns | |
| TDI Hold | $t_{THDX}$ | 4 | — | ns | |
| TCK Low to Valid Data | $t_{TLOV}$ | — | 7 | ns | 1 |

1. See AC Test Loading on page 9.

## JTAG Timing Diagram
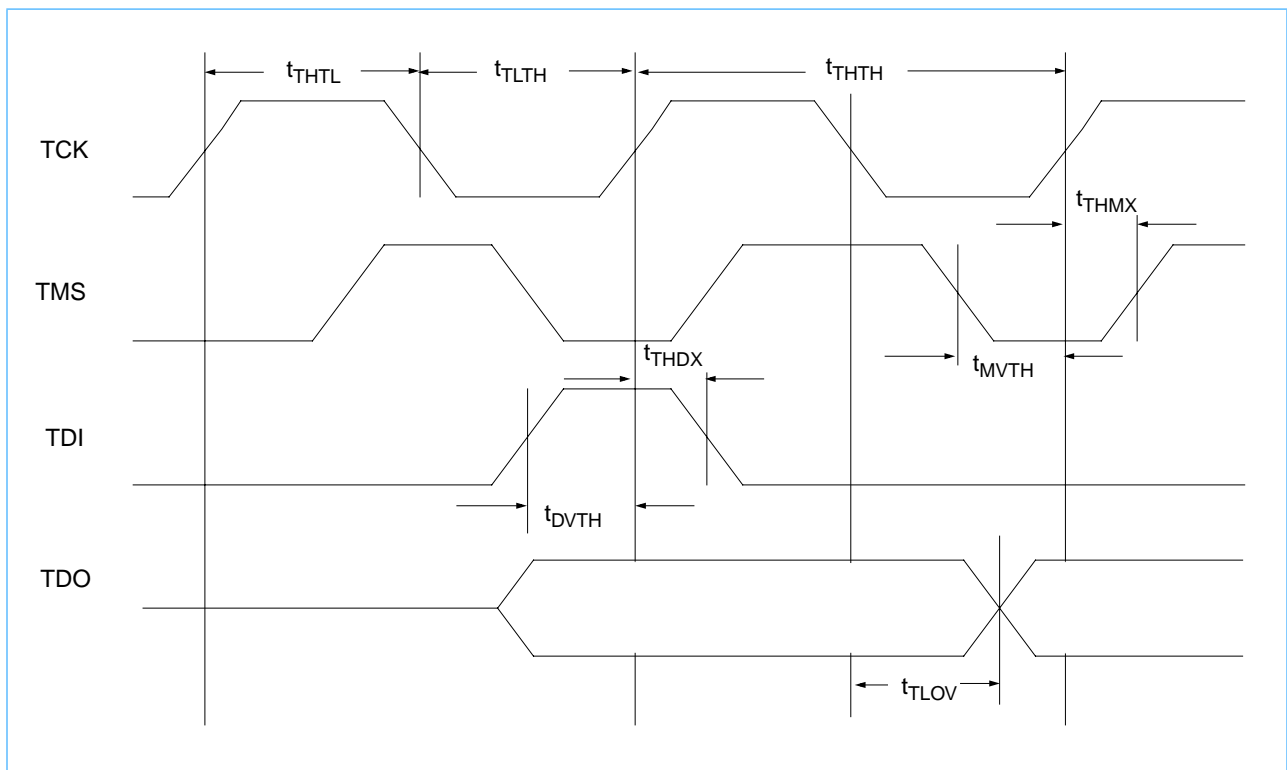
## Scan Register Definition

| Register Name | Bit Size x18 | Bit Size x36 |
|---|---|---|
| Instruction | 3 | 3 |
| Bypass | 1 | 1 |
| ID | 32 | 32 |
| Boundary Scan * | 51 | 70 |

* The Boundary Scan chain consists of the following bits:
  - 36 or 18 bits for Data Inputs Depending on x18 or x36 Configuration
  - 17 bits for SA0 - SA16 for x36, 18 bits for SA0 - SA17 for x18
  - 4 bits for $\overline{SBWa}$ - $\overline{SBWd}$ in x36, 2 bits for $\overline{SBWa}$ and $\overline{SBWb}$ in x18
  - 9 bits for K, $\overline{K}$, ZQ, $\overline{SS}$, $\overline{G}$, $\overline{SW}$, ZZ, M1 and M2
  - 4 bits for Place Holders

* K and $\overline{K}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

## ID Register Definition

| Part | Field Bit Number and Description | | | | |
|---|---|---|---|---|---|
| | Revision Number (31:28) | Device Density and Configuration (27:18) | Vendor Definition (17:12) | Manufacture JEDEC Code (11:1) | Start Bit(0) |
| 256K x 18 | 0001 | 011 100 1011 | 001000 | 000 101 001 00 | 1 |
| 128K x 36 | 0001 | 011 010 1100 | 001000 | 000 101 001 00 | 1 |

## Instruction Set

| Code | Instruction | Notes |
|---|---|---|
| 000 | SAMPLE-Z | 1,5 |
| 001 | IDCODE | 2 |
| 010 | SAMPLE-Z | 1,5 |
| 011 | PRIVATE | |
| 100 | SAMPLE | 4,5 |
| 101 | PRIVATE | |
| 110 | PRIVATE | |
| 111 | BYPASS | 3 |

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. SRAM must not be in Sleep mode (ZZ = H) when SAMPLE-Z or SAMPLE instructions are invoked.

## List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

## Boundary Scan Order (x36) (PH =Place Holder)

| Exit Order | Signal | Bump # | Exit Order | Signal | Bump # | Exit Order | Signal | Bump # |
|---|---|---|---|---|---|---|---|---|
| 1 | M2 | 5R | 25 | DQ13 | 6F | 49 | DQ26 | 2H |
| 2 | SA1 | 4P | 26 | DQ11 | 7E | 50 | DQ25 | 1H |
| 3 | SA2 | 4T | 27 | DQ12 | 6E | 51 | $\overline{SBW}c$ | 3G |
| 4 | SA12 | 6R | 28 | DQ9 | 7D | 52 | ZQ | 4D |
| 5 | SA13 | 5T | 29 | DQ10 | 6D | 53 | SS | 4E |
| 6 | ZZ | 7T | 30 | SA14 | 6A | 54 | C=0[2] | 4G |
| 7 | DQ1 | 6P | 31 | SA15 | 6C | 55 | C=1[2] | 4H |
| 8 | DQ0 | 7P | 32 | SA10 | 5C | 56 | SW | 4M |
| 9 | DQ3 | 6N | 33 | SA16 | 5A | 57 | $\overline{SBW}d$ | 3L |
| 10 | DQ2 | 7N | 34 | PH[1] | 6B | 58 | DQ34 | 1K |
| 11 | DQ4 | 6M | 35 | SA11 | 5B | 59 | DQ35 | 2K |
| 12 | DQ6 | 6L | 36 | SA8 | 3B | 60 | DQ32 | 1L |
| 13 | DQ5 | 7L | 37 | PH[1] | 2B | 61 | DQ33 | 2L |
| 14 | DQ8 | 6K | 38 | SA7 | 3A | 62 | DQ31 | 2M |
| 15 | DQ7 | 7K | 39 | SA9 | 3C | 63 | DQ29 | 1N |
| 16 | $\overline{SBW}a$ | 5L | 40 | SA6 | 2C | 64 | DQ30 | 2N |
| 17 | K | 4L | 41 | SA5 | 2A | 65 | DQ27 | 1P |
| 18 | K | 4K | 42 | DQ19 | 2D | 66 | DQ28 | 2P |
| 19 | G | 4F | 43 | DQ18 | 1D | 67 | SA3 | 3T |
| 20 | SBWb | 5G | 44 | DQ21 | 2E | 68 | SA4 | 2R |
| 21 | DQ16 | 7H | 45 | DQ20 | 1E | 69 | SA0 | 4N |
| 22 | DQ17 | 6H | 46 | DQ22 | 2F | 70 | M1 | 3R |
| 23 | DQ14 | 7G | 47 | DQ24 | 2G | | | |
| 24 | DQ15 | 6G | 48 | DQ23 | 1G | | | |

1. Input of PH register connected to $V_{SS}$.
2. Balls 4G and 4H are unused C Clock pins in this application.

## Boundary Scan Order (x 18)

(PH =Place Holder)

| Exit Order | Signal | Bump # | Exit Order | Signal | Bump # |
|---|---|---|---|---|---|
| 1 | M2 | 5R | 27 | PH[1] | 2B |
| 2 | SA12 | 6T | 28 | SA7 | 3A |
| 3 | SA1 | 4P | 29 | SA9 | 3C |
| 4 | SA13 | 6R | 30 | SA6 | 2C |
| 5 | SA17 | 5T | 31 | SA5 | 2A |
| 6 | ZZ | 7T | 32 | DQ9 | 1D |
| 7 | DQ0 | 7P | 33 | DQ12 | 2E |
| 8 | DQ3 | 6N | 34 | DQ15 | 2G |
| 9 | DQ6 | 6L | 35 | DQ16 | 1H |
| 10 | DQ7 | 7K | 36 | $\overline{S}$BWb | 3G |
| 11 | $\overline{S}$BWa | 5L | 37 | ZQ | 4D |
| 12 | K | 4L | 38 | SS | 4E |
| 13 | K | 4K | 39 | C=0[2] | 4G |
| 14 | G | 4F | 40 | C=1[2] | 4H |
| 15 | DQ8 | 6H | 41 | SW | 4M |
| 16 | DQ5 | 7G | 42 | DQ17 | 2K |
| 17 | DQ4 | 6F | 43 | DQ14 | 1L |
| 18 | DQ2 | 7E | 44 | DQ13 | 2M |
| 19 | DQ1 | 6D | 45 | DQ11 | 1N |
| 20 | SA14 | 6A | 46 | DQ10 | 2P |
| 21 | SA15 | 6C | 47 | SA3 | 3T |
| 22 | SA10 | 5C | 48 | SA4 | 2R |
| 23 | SA16 | 5A | 49 | SA0 | 4N |
| 24 | PH[1] | 6B | 50 | SA2 | 2T |
| 25 | SA11 | 5B | 51 | M1 | 3R |
| 26 | SA8 | 3B | | | |

1. Input of PH register connected to $V_{SS}$
2. Balls 4G and 4H are unused C Clock pins in this application.

## TAP Controller State Machine

## 7 x 17 PBGA Dimensions



Note: All dimensions in Millimeters Unless Otherwise noted
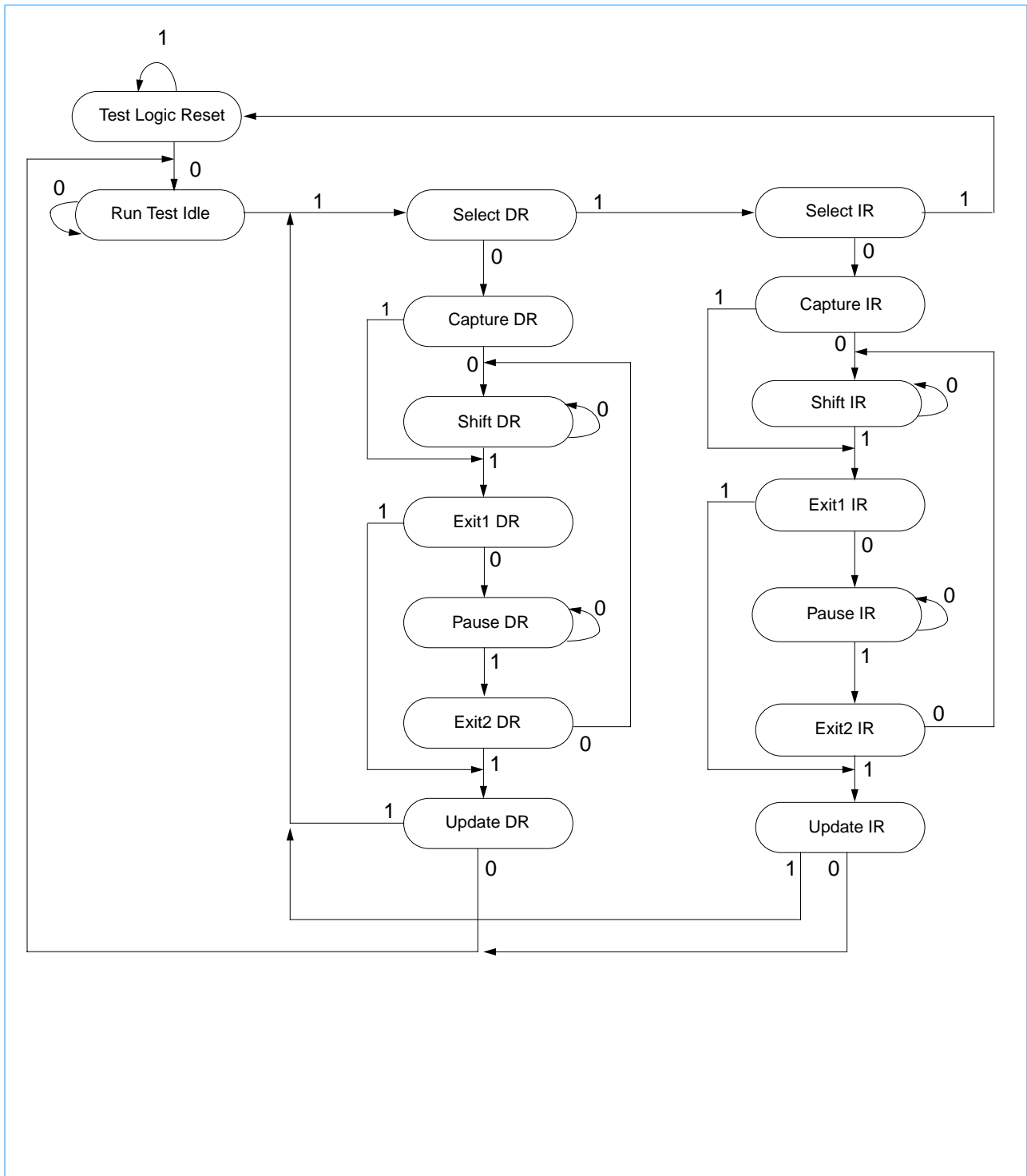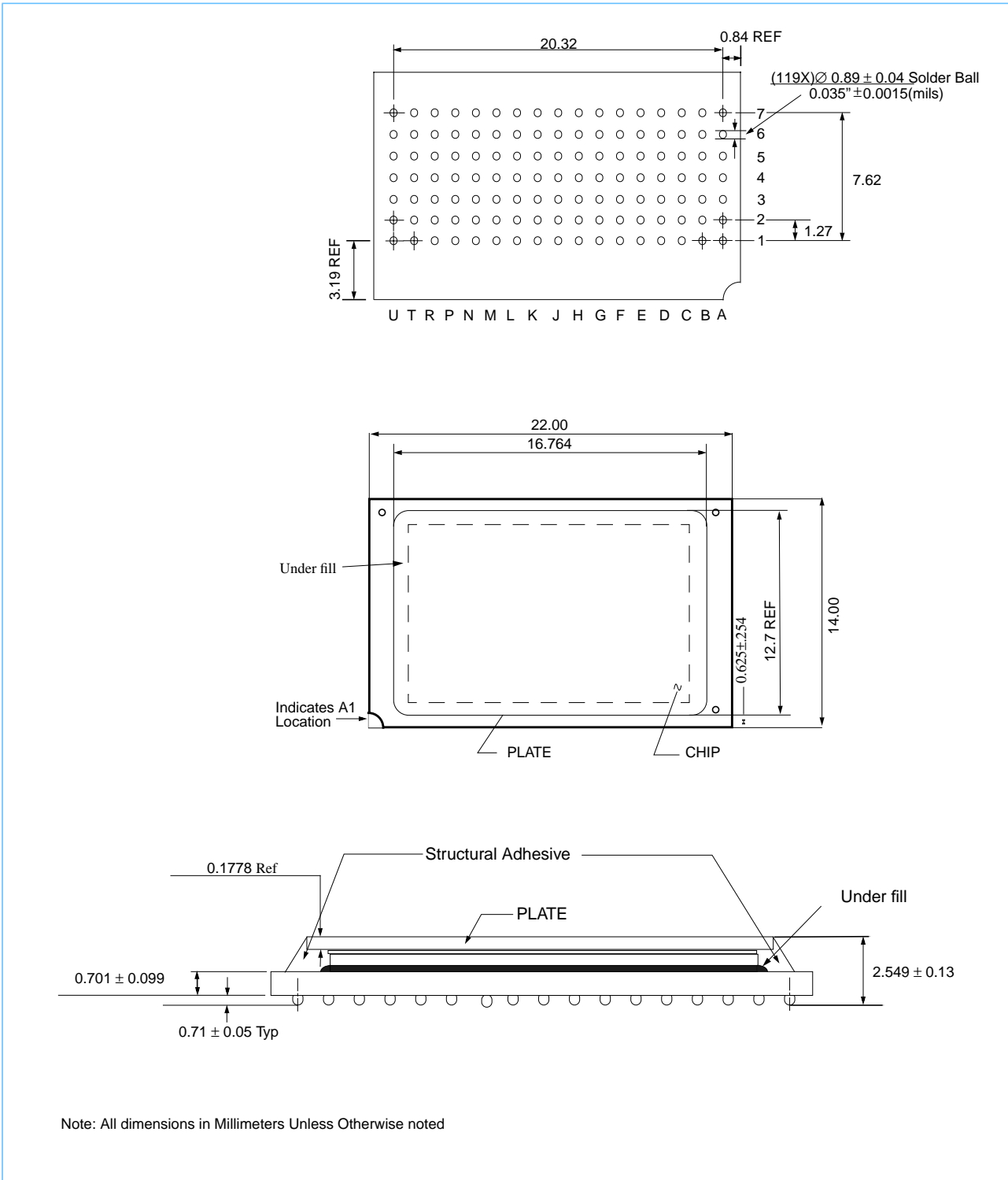
## References Rev "D" - Last Character in Part Number (D)

The following documents give recommendations, restrictions and limitations for 2nd level attach process:

C4 SRAM Assembly Guide for Single Sided Assembly

Double Sided 4Meg Coupled Cap PBGA Card Assembly Guide

There is qualification information, including scope of application conditions qualified, available from your marketing representative.

## Revision Log

| Rev | Contents of Modification |
|---|---|
| 9/95 | Initial Release of the 128K x 36 & 256K x 18, (5/6/7 cycle), BGA, HSTL, PIPE LINE Application Spec. |
| 11/95 | Update scan chain. |
| 2/96 | Update part numbers, updated package drawing. |
| 5/13/96 | Update part number. |
| 7/16/96 | Add thermal resistance, update timings and currents. |
| 11/24/96 | Cleanup |
| 1/97 | Updated package drawing. |
| 8/20/97 | Updated JTAG definitions. Power Up/Down requirements. Tkhqx4 updated. |
| 9/17/97 | Updated Power up/down definitions. Updated -4 part number and added +10% power supply. |
| 9/97 | Updated Tkhqz for -4 part number. |
| 12/97 | Updated capacitance and -4 part. Added x18 ceramic part |
| 5/98 | Updated Tri-state measurement point (Test did not change). Added -4 & -4N x36 sorts |
| 6/98 | Updated AC input data. Changed Pimp tolerance to ±15% and 2080 max cycle update. Changed Rev B to Rev D. Added references for Rev D and changed package diagram. Added Sleep mode statement. Removed Ceramic parts. Minor update to Boundary Scan. |
| 2/99 | Tightened the BGA ball diameter tolerance. |

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