NLAS7222A

3.3 V, Wide Bandwidth, 2- to -1-Port (DPDT) Switch with Enable

ON Semiconductor’s NLAS7222A series of analog switch circuits are produced using the company’s advanced sub−micron CMOS technology, achieving industry−leading performance.

The NLAS7222A is a 2− to 1−port analog switch. Its wide bandwidth and low bit−to−bit skew allow it to pass high−speed differential signals with good signal integrity. The switch is bidirectional and offers little or no attenuation of the high−speed signals at the outputs. Industry−leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Its high channel−to−channel crosstalk rejection results in minimal noise interference. Its bandwidth is wide enough to pass High−Speed USB 2.0 differential signals (480 Mb/s).

Features

- R_{ON} is Typically 6.5 Ω at V_{CC} = 3 V
- Low Bit−to−Bit Skew: Typically 50 ps
- OVT on D+ and D− up to 3.6 V
- Power OFF Protection:
  When V_{CC} = 0 V, D+ and D− Can Tolerate up to 3.6 V
- Low Crosstalk: −45 dB @ 250 MHz
- Low Current Consumption: 1 μA
- Near−Zero Propagation Delay: 250 ps
- Channel On−Capacitance: 6.5 pF (Typical)
- V_{CC} Operating Range: +3.0 V to +3.6 V
- > 720 MHz Bandwidth (or Data Frequency)
- This is a Pb−Free Device

Typical Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

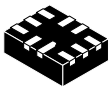
Important Information

- Continuous Current Rating Through Each Switch ±50 mA

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



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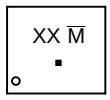
WQFN−10
CASE 488AQ



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

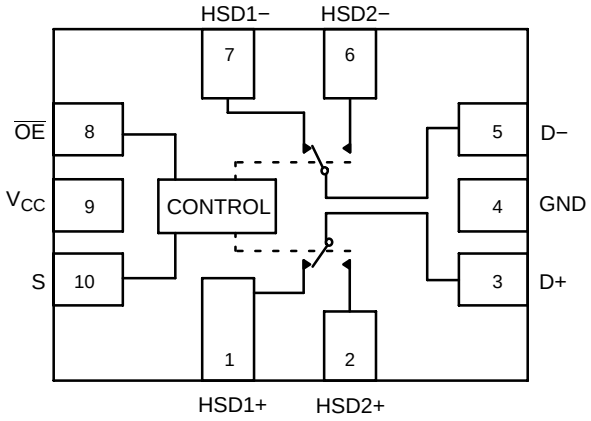


Figure 1. Pin Connections and Logic Diagram
(Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Select Input
$\overline{OE}$	Output Enable
HSD1+, HSD1−, HSD2+, HSD2−, D+, D−	Data Ports

Table 2. TRUTH TABLE

$\overline{OE}$	S	HSD1+, HSD1−	HSD2+, HSD2−
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	−0.5 to +4.6	V
V_{IS}	Analog Switch Input Voltage HSD1+, HSD1−, HSD2+, HSD2− D+, D−	 −0.5 to V_{CC} + 0.3 −0.5 to +4.6	V
V_{IN}	Digital Select Input Voltage	−0.5 to +4.6	V
I_D	Continuous DC Current (Through Analog Switch)	50	mA
P_D	Power Dissipation	0.5	W
T_S	Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	3.0	3.6	V
V_{IS}	Analog I/O Voltage (HSD1+, HSD1−, HSD2+, HSD2−)	GND	V_{CC}	V
V_{OS}	Analog Common Output Voltage (D+, D−)	GND	3.6	V
V_{IN}	Digital Select Input Voltage	GND	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C
t_r, t_f	Input Rise or Fall Time V_{CC} = 3.3 V ± 0.3 V	0	15	ns

DC ELECTRICAL CHARACTERISTICS FOR USB 2.0 SWITCHING OVER OPERATIONAL RANGE

Symbol	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
				Min	Typ (Note 1)	Max	
V_{IH}	Input HIGH Voltage (V_{IN})		3.0 to 3.6	1.3	−	−	V
V_{IL}	Input LOW Voltage (V_{IN})		3.0 to 3.6	−	−	0.5	V
V_{IK}	Clamp Diode Voltage	I_{IS} = −18 mA	3.0	−	−	−1.2	V
I_{CC}	Quiescent Supply Current	V_{IS} = V_{CC} or GND; I_D = 0 A	3.6	−	−	1.0	μA
I_{CCT}	Increase in I_{CC} per Control Voltage	V_{IN} = 2.6 V	3.6	−	−	10.0	μA
I_I	Input Leakage Current	0 ≤ V_{IS} ≤ V_{CC}	3.6	−	−	±1.0	μA
I_{OZ}	OFF State Leakage	0 ≤ $V_{IS;}$ V_{OS} ≤ V_{CC}	3.6	−	−	±1.0	μA
I_{OFF}	Power OFF Leakage Current (D+, D−)	0 ≤ $V_{IS;}$ V_{OS} ≤ V_{CC}	0	−	−	±1.0	μA
R_{ON}	Switch On−Resistance	V_{IS} = 0 to 0.4 V; I_D = 8 mA	3.0	−	6.5	9.0	Ω
$R_{FLAT(ON)}$	On−Resistance Flatness	V_{IS} = 0 to 1.0 V; I_D = 8 mA	3.0	−	2.0	−	Ω
ΔR_{ON}	On−Resistance match from center ports to any other ports	V_{IS} = 0 to 0.4 V; I_D = 8 mA	3.0	−	0.35	−	Ω

1. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
				Min	Typ (Note 2)	Max	
t_{ON}	Turn−ON Time	V_{IS} = 0.8 V	3.0 to 3.6	−	13.0	30.0	ns
t_{OFF}	Turn−OFF Time	V_{IS} = 0.8 V	3.0 to 3.6	−	12.0	25.0	ns
t_{BBM}	Break−Before−Make Delay	V_{IS} = 0.8 V	3.0 to 3.6	2.0	4.7	6.5	ns
t_{PD}	Propagation Delay	C_L = 10 pF	3.0 to 3.6	−	0.25	−	ns
O_{IRR}	OFF−Isolation	f = 250 MHz; R_L = 50 Ω	3.0 to 3.6	−	−28	−	dB
X_{TALK}	Non−Adjacent Channel Crosstalk	f = 250 MHz; R_L = 50 Ω	3.0 to 3.6	−	−45	−	dB
BW	−3 dB Bandwidth	R_L = 50 Ω; C_L = 0 pF	3.0 to 3.6	−	720	−	MHz
		R_L = 50 Ω; C_L = 5 pF		−	500	−	

AC ELECTRICAL CHARACTERISTICS FOR USB 2.0 SWITCHING OVER OPERATIONAL RANGE

$t_{SK(O)}$	Channel−to−Channel Skew	C_L = 10 pF	3.0 to 3.6	−	0.05	−	ns
T_{JITTER}	Total Jitter	R_L = 50 Ω; C_L = 10 pF t_r = t_f = 500 ps at 480 Mbps	3.0 to 3.6	−	0.2	−	ns

2. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

CAPACITANCE

Symbol	Parameter	Test Conditions	−40°C to +85°C			Unit
			Min	Typ (Note 3)	Max	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V	−	4.5	−	pF
C_{ON}	HSD+, HSD− ON Capacitance	V_{CC} = 3.3 V; $\overline{OE}$ = 0 V	−	14	−	pF
C_{OFF}	HSD+, HSD− OFF Capacitance	V_{CC} = V_{IS} = 3.3 V; $\overline{OE}$ = 3.3 V	−	12	−	pF

3. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

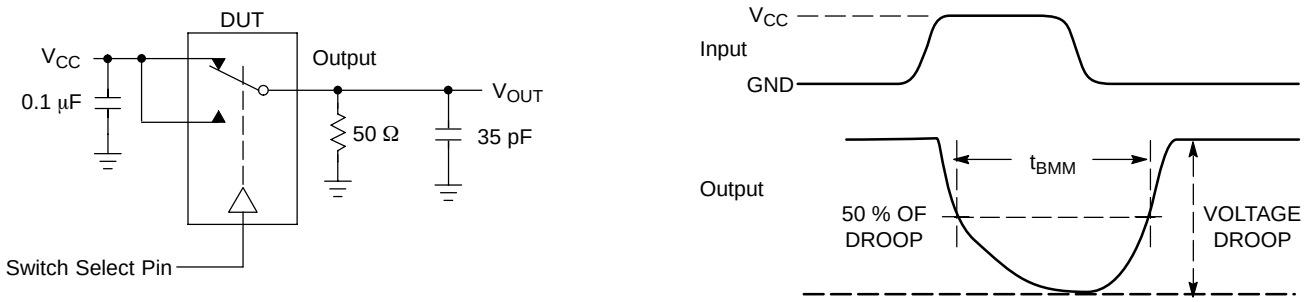


Figure 2. t_{BBM} (Time Break−Before−Make)

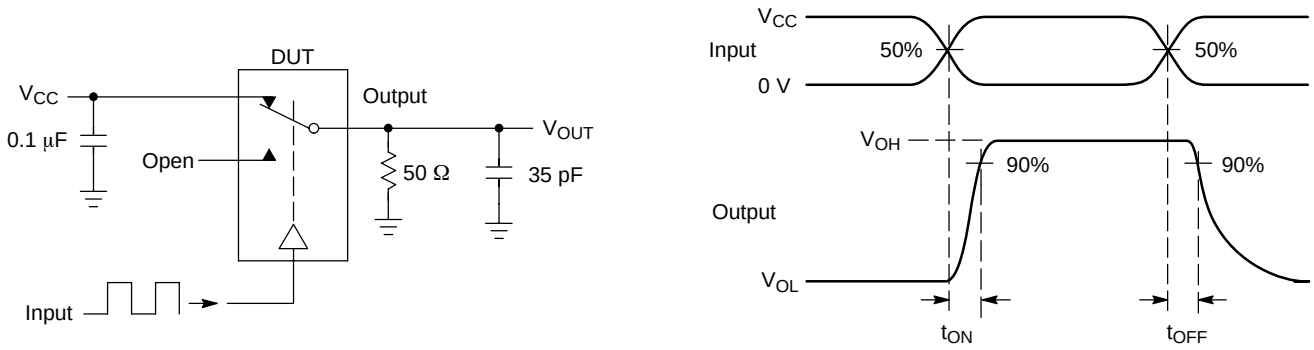


Figure 3. t_{ON}/t_{OFF}

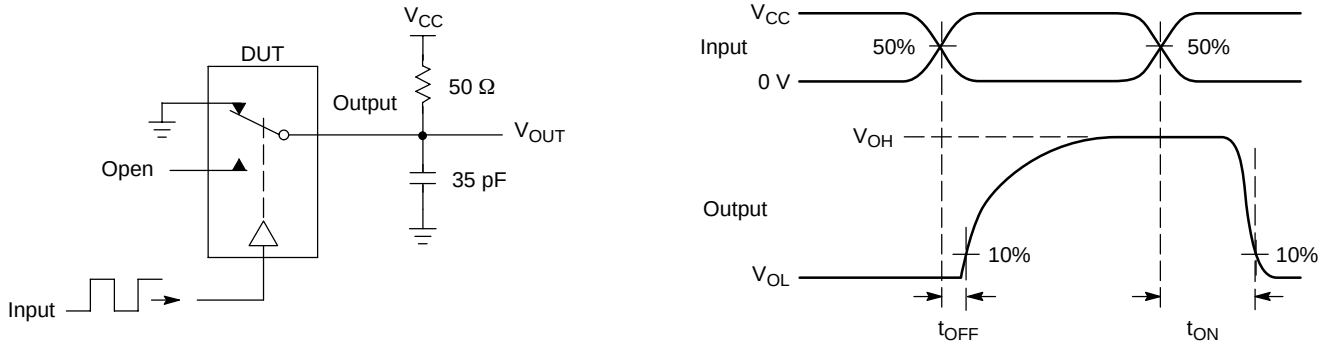
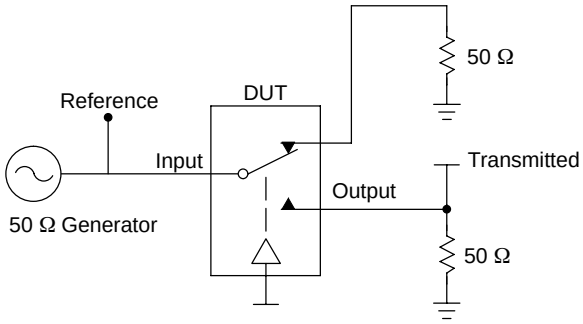


Figure 4. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log$\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log$\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

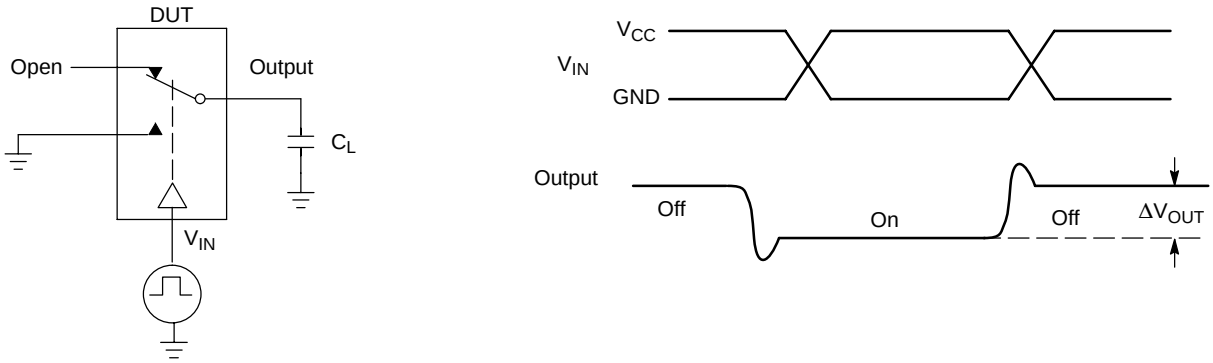


Figure 6. Charge Injection: (Q)

APPLICATIONS INFORMATION

The low on resistance and capacitance of the NLAS7222A provides for a high bandwidth analog switch suitable for applications such as USB data switching. Results for the USB 2.0 signal quality tests will be shown in this section, along with a description of the evaluation test board. The data for the eye diagram signal quality and jitter tests verifies that the NLAS7222A can be used as a data switch in low, full and high speed USB 2.0 systems.

Figures 7, 8 and 9 provide a description of the test evaluation board. The USB tests were conducted per the procedures provided by the USB Implementers Forum (www.usb.org), the industry group responsible for defining the USB certification requirements. The test patterns were generated by a PC and MATLAB software, and were inputted to the analog switch through USB connectors J1 (HSD1) or J2 (HSD2). A USB certified device was plugged into connector J4 to function as a data transceiver. The high speed and full speed tests used a flash memory device, while the low speed tests used a mouse. Test connectors J3 and J5 provide a direct connection of the USB device and were used to verify that the analog switch does not distort the data signals.

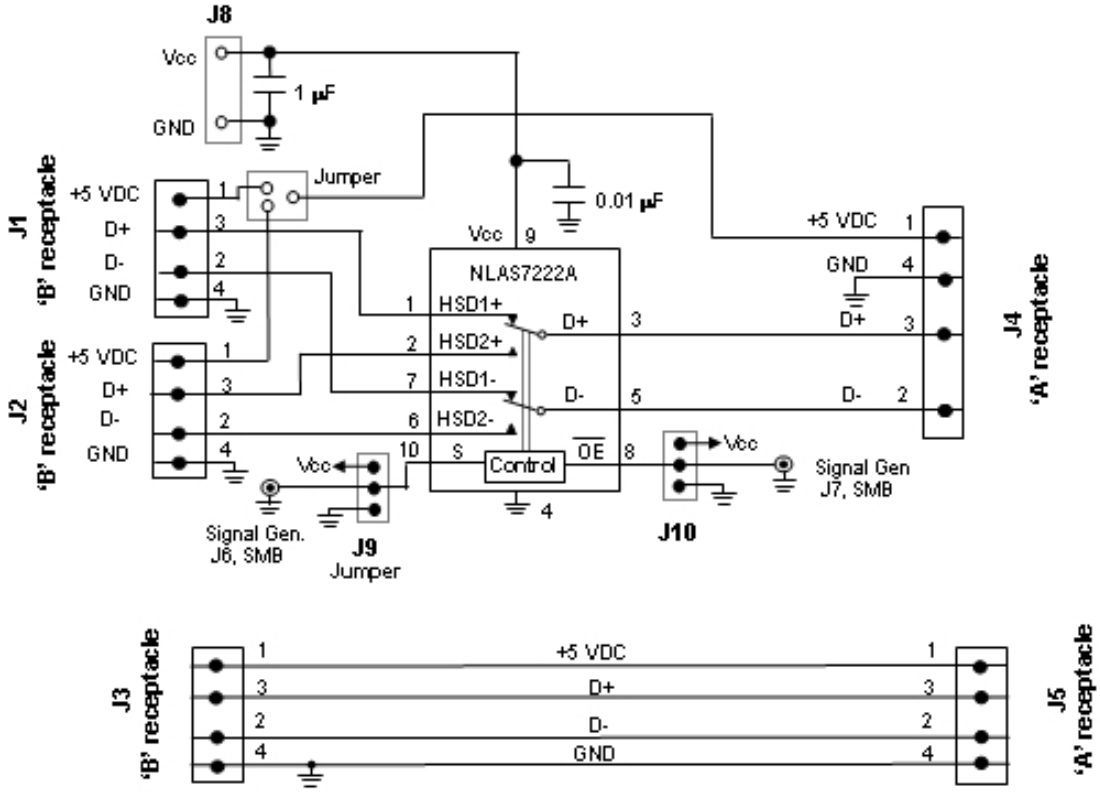


Figure 7. Schematic of the NLAS7222A USB Demo Board

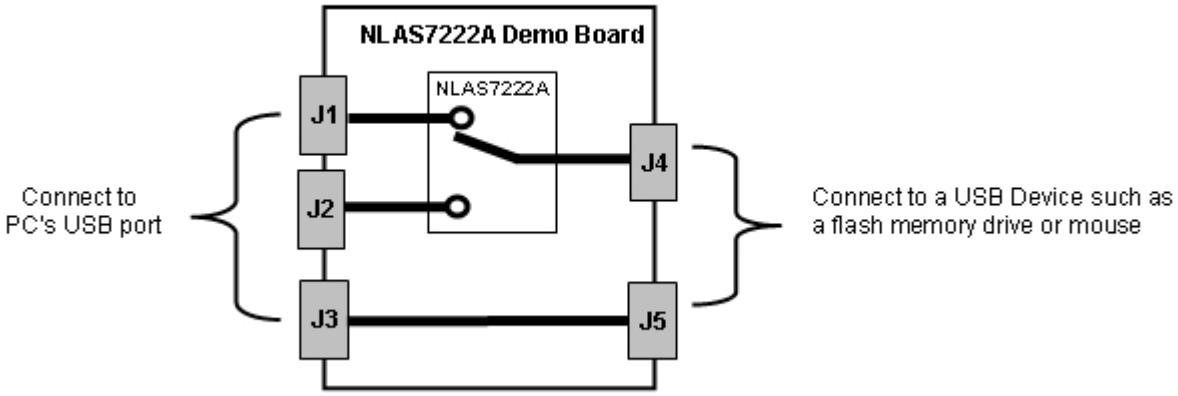


Figure 8. Block Diagram of the NLAS7222A USB Demo Board

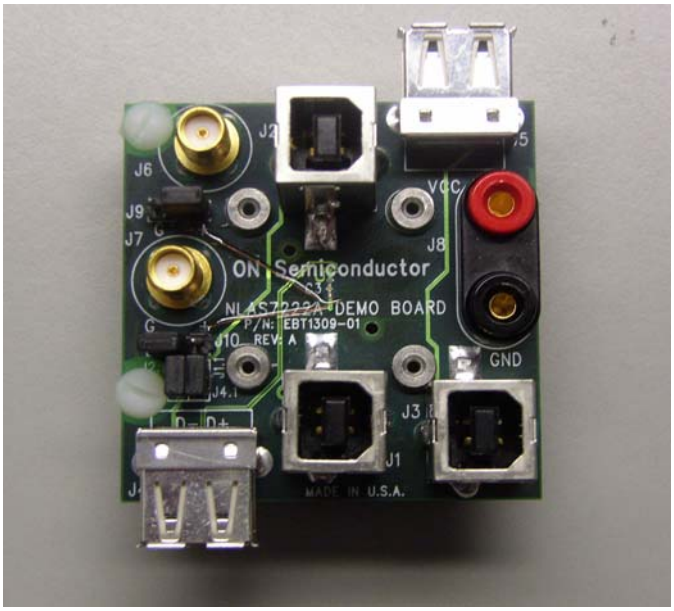


Figure 9. Photograph of the NLAS7222A USB Demo Board

AND8267/D – NLAS7222A USB 2.0 Signal Quality Compliance Tests

Figures 10, 11 and 12 show the test results for USB eye diagram tests. A summary of the USB tests is provided in Table 3. The NLAS7222A passes the low, full and high speed signal quality, eye diagram and jitter tests. Application note AND8267/D provides a detailed description of the USB 2.0 test results.

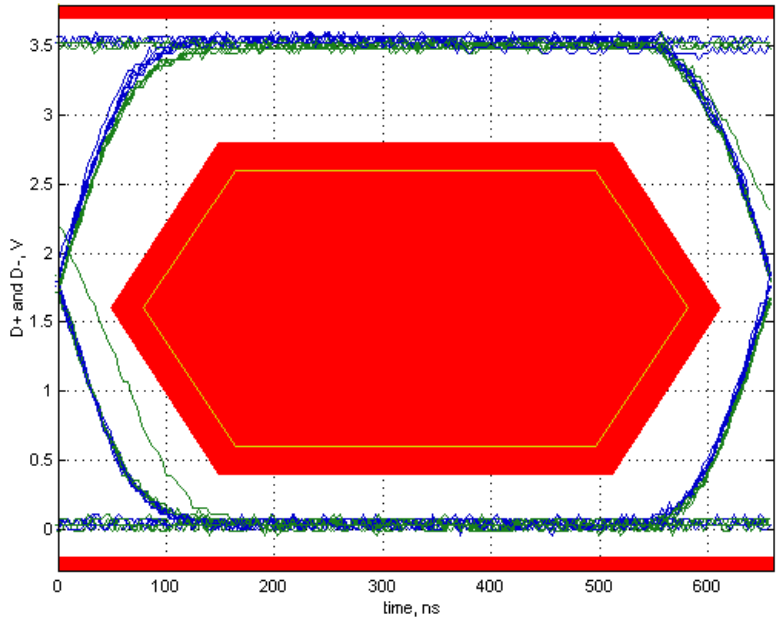


Figure 10. Low Speed Signal Quality Eye Diagram Test (NLAS7222A with V_{CC} = 3.6 V)

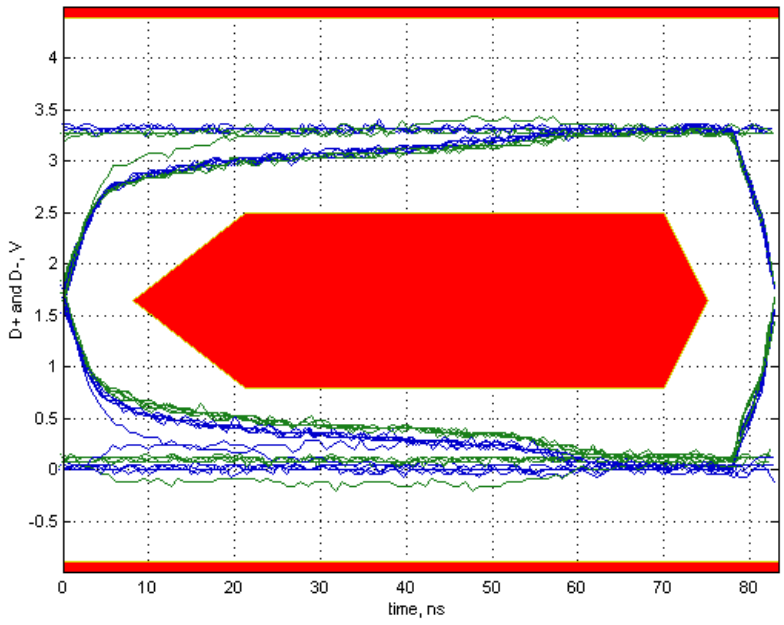


Figure 11. Full Speed Signal Quality Eye Diagram Test (NLAS7222A with V_{CC} = 3.6 V)

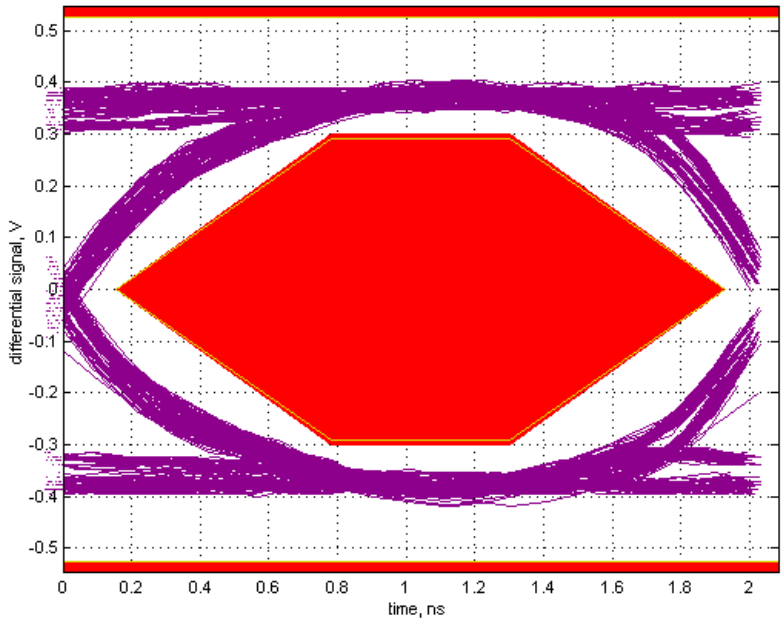


Figure 12. High Speed Signal Quality Eye Diagram Test (NLAS7222A with V_{CC} = 3.0 V)

Table 3. Summary of the USB 2.0 Signal Quality Tests Results

Compliance Test	Low Speed	Full Speed	High Speed
Signal Quality Test	Pass	Pass	Pass
Signal Eye Test	Pass	Pass	Pass
EOP Width	1.29 ms	166.86 ns	7.98 bits
Measured Signal Rate	1.5140 MHz	12.0016 MHz	480.0685 MHz
Crossover Voltage Range	1.75 to 1.83 V, mean crossover = 1.78 V	1.70 to 1.73 V, mean crossover = 1.71 V	N/A
Connective Jitter Range	−2.2 to 2.2 ns, RMS jitter = 1.3 ns	−0.2 to 0.2 ns, RMS jitter = 0.1 ns	−79.4 to 77.4 ps, RMS jitter = 35.0 ps
Paired JK Jitter Range	−1.4 to 2.7 ns, RMS jitter = 1.3 ns	−0.1 to 0.1 ns, RMS jitter = 0.1 ns	−93.2 to 78.7 ps, RMS jitter = 24.4 ps
Paired KJ Jitter Range	−1.9 to 1.1 ns, RMS jitter = 1.0 ns	−0.2 to 0.1 ns, RMS jitter = 0.1 ns	−72.8 to 50.9 ps, RMS jitter = 15.6 ps

ORDERING INFORMATION

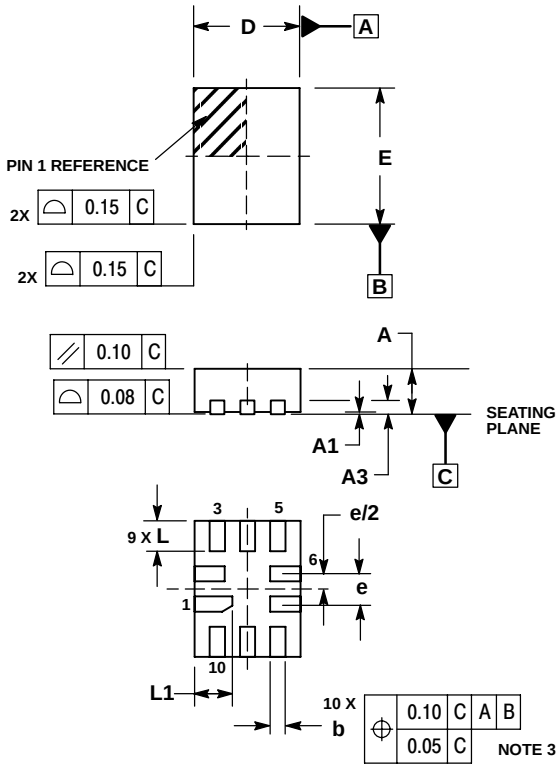
Device Order Number	Device Nomenclature				Package	Shipping†
	Circuit Indicator	Technology	Device Function	Tape & Reel Suffix		
NLAS7222AMTR2G	NL	AS	7222	R2	WQFN−10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLAS7222A

PACKAGE DIMENSIONS

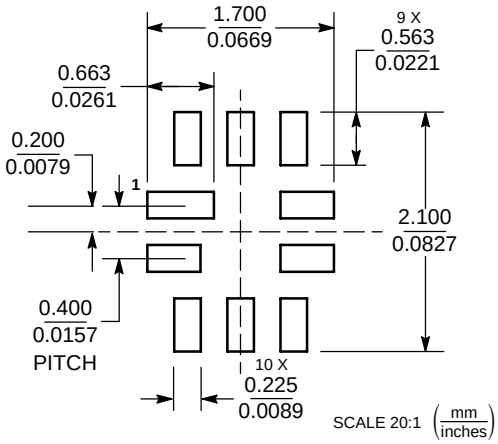
WQFN10, 1.4x1.8x0.4P
CASE 488AQ−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.40	0.60

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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