

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

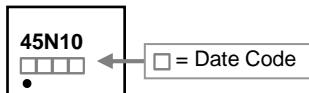
DESCRIPTION

The SSP45N10 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .The SSP45N10 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

FEATURES

- Simple Drive Requirement
- Small Package Outline

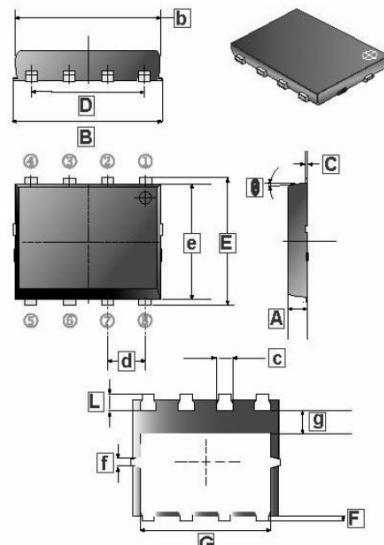
MARKING



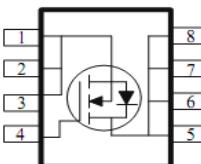
PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8PP	3K	13 inch

SOP-8PP



TOP VIEW



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	0.80	1.00	θ	0°	10°
B	5.3 BSC.		b	5.2 BCS	
C	0.15	0.25	c	0.20	0.50
D	3.8 BCS.		d	1.27 BSC	
E	6.05 BCS.		e	5.65 BCS.	
F	0.03	0.30	f	0.10	0.40
G	4.35 BCS.		g	1.3 BCS.	
L	0.40	0.70			

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ , $V_{GS} @ 10\text{V}$	I_D	45	A
		28	
Pulsed Drain Current ²	I_{DM}	100	A
Power Dissipation ⁴	P_D	90	W
Single Pulse Avalanche Energy ³	E_{AS}	98	mJ
Single Pulse Avalanche Current	I_{AS}	41	A
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55~150	°C
Thermal Resistance Rating			
Maximum Junction to Case ¹	$R_{\theta JC}$	1.4	°C / W
Maximum Junction to Ambient ¹	$R_{\theta JA}$	36	°C / W

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0$, $I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(\text{th})}$	2.5	-	4.5	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	27	-	S	$V_{DS}=5\text{V}$, $I_D=30\text{A}$
Gate Resistance	R_G	-	1.9	3.8	Ω	$f=1\text{MHz}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	$T_J=25^\circ\text{C}$	I_{DSS}	-	-	1	$V_{DS}=80\text{V}$, $V_{GS}=0$
			-	-	5	
Drain-Source On-Resistance ²	$T_J=55^\circ\text{C}$	$R_{DS(\text{ON})}$	-	19	22	$V_{GS}=10\text{V}$, $I_D=30\text{A}$
			-	25	30	
Dynamic						
Total Gate Charge	Q_g	-	27.6	-	nC	$V_{DS}=80\text{V}$, $V_{GS}=10\text{V}$, $I_D=30\text{A}$
Gate-Source Charge	Q_{gs}	-	11.4	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	7.9	-		
Turn-on Delay Time ²	$T_{d(\text{on})}$	-	15.6	-	nS	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\Omega$, $I_D=30\text{A}$
Rise Time	T_r	-	17.2	-		
Turn-off Delay Time	$T_{d(\text{off})}$	-	16.8	-		
Fall Time	T_f	-	9.2	-		
Input Capacitance	C_{iss}	-	1890	-	pF	$V_{GS}=0$, $V_{DS}=15\text{V}$, $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	268	-		
Reverse Transfer Capacitance	C_{rss}	-	67	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ⁵	EAS	53	-	-	mJ	$V_{DD}=50\text{V}$, $L=0.1\text{mH}$, $I_{AS}=30\text{A}$
Source-Drain Diode						
Diode Forward Voltage ²	V_{SD}	-	-	1	V	$I_S=1\text{A}$, $V_{GS}=0$
Continuous Source Current ^{1,6}	I_S	-	-	45	A	$V_D=V_G=0$, Force Current
Pulsed Source Current ^{2,6}	I_{SM}	-	-	100	A	
Reverse Recovery Time	T_{RR}	-	34	-	ns	$I_F=30\text{A}$, $T_J=25^\circ\text{C}$ $dI/dt=100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	-	47	-	nC	

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $\leq 10\text{sec}$, $125^\circ\text{C}/\text{W}$ at steady state
- The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=53.8\text{A}$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation

CHARACTERISTIC CURVES

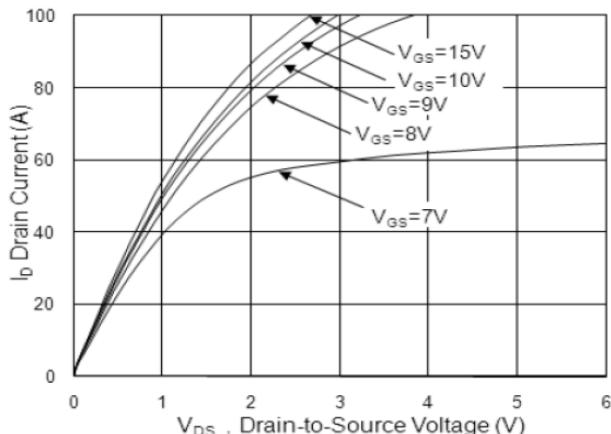


Fig.1 Typical Output Characteristics

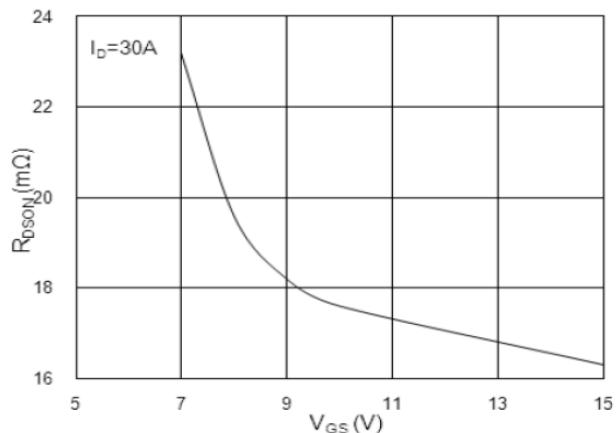


Fig.2 On-Resistance v.s Gate-Source

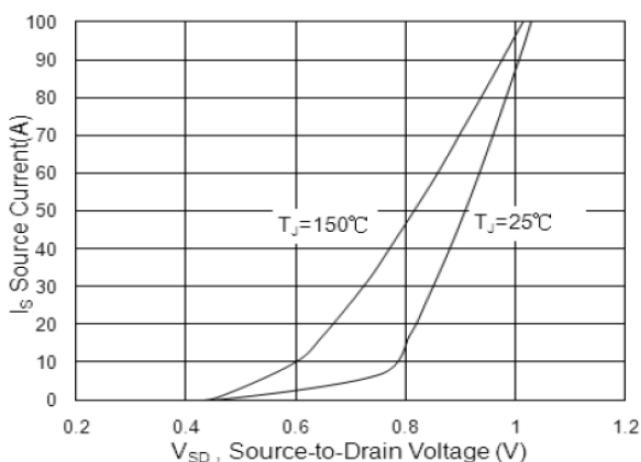


Fig.3 Forward Characteristics of Reverse

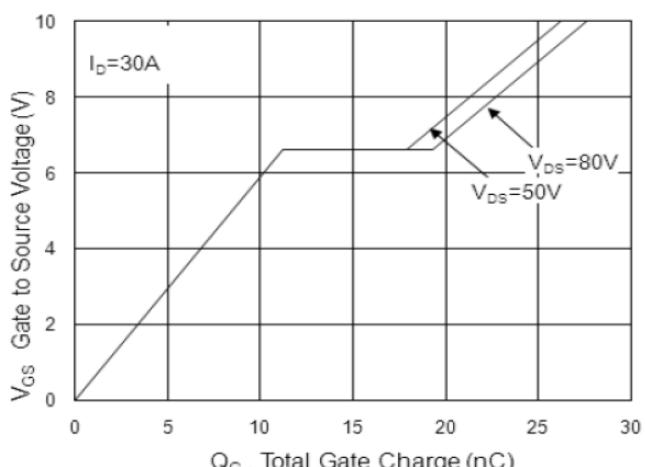


Fig.4 Gate-Charge Characteristics

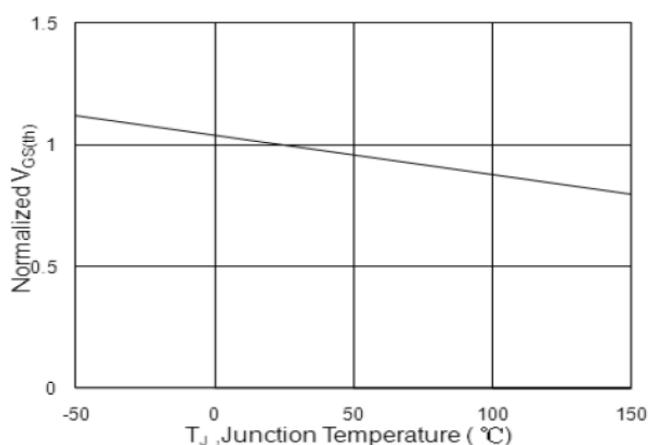


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

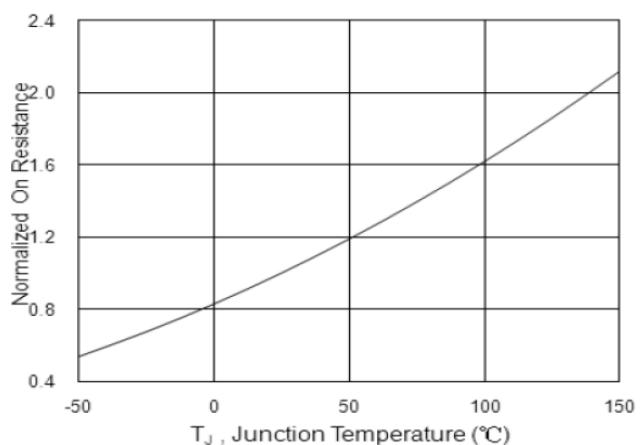


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

CHARACTERISTIC CURVES

