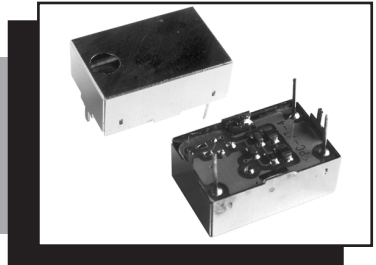TTL / CMOS AND SINE WAVE • CRYSTAL OSCILLATORS

TEMPERATURE-COMPENSATED XTAL OSCILLATORS
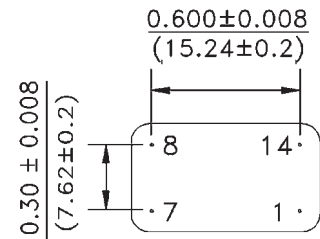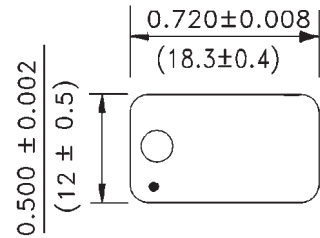
ACTX 1018 and ACVTX 1018 Series

FEATURES:

- Compatible with 14 Pin Dual in Line.
- Compact Size.
- Tight Stability Available.
- Low Current Consumption.
- Control Voltage Function.
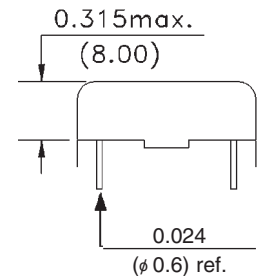- Low can height option.

APPLICATIONS:

- Cellular and Cordless Phones.
- Facsimile and Computer Control.
- Car Telephones.
- Communication Equipment

STANDARD SPECIFICATIONS

PARAMETERS		ACTX 1018 (A) ACVTX1018 (A)	ACTX 1018 S ACVTX1018S (A)
Frequency Range	(F_O)	1 MHz - 26 MHz	8 MHz - 45 MHz
Operating Temperature	(T_{OPR})	-10°C to + 60°C *(See Options / Table 1)*	
Storage Temperature	(T_{STO})	-40°C to + 85°C	
Frequency Stability -vs- 25°C		± 0.5 ppm max	
-vs- Temperature		± 2.5 ppm max. *(See Options / Table 1)*	
-vs- Aging		± 1 ppm per year max.	
-vs- Supply Voltage		± 0.5 ppm max.	
Supply Voltage	(V_{dd})	5 Vdc ± 5% or 3.3 Vdc ± 5% (A Series)	
Input Current	(I_{dd})	20 mA max.	2 mA max. for F ≤ 26 MHz 4 mA max. for F > 26 MHz
Duty Cycle or Symmetry		40 / 60% max.	N / A
Rise and Fall Times	(T_R / T_F)	10 ns max.	N / A
Output Load		15 pF or 2 TTL	10 k Ω // 10 pF
Output Voltage	(V_{OH})	0.9 * Vdd min.	1 Vpp min. Clipped Sine
	(V_{OL})	0.4 Vdc max.	0.7 Vpp min. (A Series)
Frequency Adjustment (Internal Trimmer)		± 3 ppm min.	
Vc and Freq. Pulling (V Series)		0.5 V to 4.5 V or 0.3 V to 3.0 V (± 10 ppm min.)	

For test circuit, waveforms, please see page 67.
Environmental and mechanical specifications on page 68, Group 4. Marking, see p. 79.

0.720±0.008
(18.3±0.4)

0.500 ± 0.002
(12 ± 0.5)

0.600±0.008
(15.24±0.2)

0.30 ± 0.008
(7.62±0.2)

• 8   14 •
• 7   1 •

Dimensions: Inches (mm)

0.315 max.
(8.00)

0.024
(∅ 0.6) ref.

NOTE:
Pin 1 may be present with no
connection function.

ORDERING OPTIONS

ACXTX 1018 XX - **Frequency** - **Temperature & Frequency Stability** - **Max. Can Height**

Blank or V

Blank or S

Blank or A

XX.XXXXX MHz
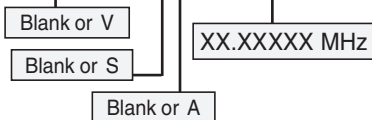
H5 for 5.08 mm

PIN #	FUNCTION
1	Vc or N/A
7	GND / Case
8	Output
14	V_{CC}

TABLE 1				*Frequency - vs.- Temperature*			
TEMPERATURE RANGE °C	± 0.5 ppm max.	± 1 ppm max.	± 1.5 ppm max.	± 2 ppm max.	± 2.5 ppm max.	± 3 ppm max.	± 5 ppm max.
0°C to +50°C	C 05	C 10	C 15	C 20	C 25	C 30	C 50
-10°C to +60°C		D 10	D 15	D 20	Standard	D 30	D 50
-20°C to +70°C				E 20	E 25	E 30	E 50
-30°C to +75°C				F 20 (∗)	F 25 (∗)	F 30 (∗)	F 50 (∗)
-40°C to +85°C						G 30 (∗)	G 50 (∗)

(∗) DEPENDING ON FREQUENCY

TECHNICAL TERMS

Nominal frequency: The center or nominal output frequency of a crystal oscillator.

Package: Crystal oscillators are packaged in various styles from lead through holes to surface-mount types. Various sizes and functions are suitable for different applications.

Frequency tolerance: The deviation from the nominal frequency in terms of parts per millions (ppm) at room temperature. (25° ± 5°C)

Frequency range: The frequency band that the oscillator type or model can be offered.

Frequency stability: The maximum allowable frequency deviation compared to the measured frequency at 25 °C over the temperature window, i.e., 0° C to +70° C. Typical stability is ± 0.01% (±100 ppm).

Operating temperature: Temperature range within which output frequency and other electrical, environmental characteristics meet the specifications.

Aging: The relative frequency change over a certain period of time. This rate of change of frequency is normally exponential in character. Typically, aging is ± 5ppm over 1 year maximum.

Storage Temperature: The temperature range where the unit is safely stored without damaging or changing the performance of the unit.

Frequency vs. Power Supply Variation: Maximum frequency change allowed when the power supply voltage is changed within its specified limits (typical ± 10% in V_{CC} or ± 5% change).

Supply Voltage (Vdd max): The maximum voltage which can safely be applied to the Vcc terminal with respect to ground. Maximum supply voltage for TTL is 5.5V and for HCMOS is 7V.

Input Voltage (V_{IN}): The maximum voltage that can be safely applied to any input terminal of the oscillator.

Output HIGH voltage (V_{OH}): The minimum voltage at an output of the oscillator under proper loading.

Output LOW voltage (V_{0H}): The maximum voltage at an output of the oscillator under proper loading.

Input HIGH voltage (V_{IH}): The minimum voltage to guarantee threshold trigger at the input of the oscillator.

Input LOW voltage (V_{IL}): The maximum voltage to guarantee the threshold trigger at the input of the oscillator.

Supply Current (Icc): The current flowing into Vcc terminal with respect to ground. Typical supply current is measured without load.

Symmetry or Duty Cycle: The symmetry of the output waveform at the specified level (at 1.4V for TTL, at 1/2 Vcc for HCMOS, or 1/2 waveform peak level for ECL).

$SYM = \dfrac{TH}{T} \times 100$ (%); See Fig. 1.

Fan Out: The measure of driving ability of an oscillator, expressed as the number of inputs that can be driven by a single output. It can be represented by an equivalent load capacitance (CL) or a TTL load circuit consisting of diodes, load resistor, and a capacitor.

Rise Time (T_r): Waveform rise time from Low to High transition, measured at the specified level

    10% to 90% for HCMOS,
    20% to 80% for ECL
    0.4V to 2.4V for TTL.

Fall Time (T_f): The waveform fall time from High to Low transition, measured at the specified level

    90% to 10% for HCMOS,
    80% to % for ECL
    2.4V to 0.4V for TTL.

Jitter: The modulation in phase or frequency of oscillator output.

HCMOS/TTL Compatible: The oscillator is designed with ACMOS logic with driving capability of TTL and HCMOS loads while maintaining minimum logic HIGH of the HCMOS.

Tristate Enable: When the input is left OPEN or tied to logic "1", the normal oscillation occurs. When the input is Grounded (tied to logic "0"), the output is in HIGH IMPEDANCE state. The input has an internal pull-up resistor thus allowing the input to be left open.

Output Logic: The output of an oscillator is designed to meet various specified logic states, such as TTL, HCMOS, ECL, Sine, Clipped-Sine (DC cut).

Harmonic Distortion: The non-linear distortion due to unwanted harmonic spectrum component related with target signal frequency. Each harmonic component is the ratio of electric power against desired signal output electric power and is expressed in terms of dBc, i.e. -20dBc. Harmonic distortion specification is important especially in sine output when a clean and less distorted signal is required.

Phase Noise: The measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single side band (SSB) power density in a 1Hz bandwidth at a specified offset frequency from the carrier. It is measured in dBc/Hz.

Stand By: A function that temporary turns off the oscillator and other dividers to save power. Logic "0" will enable stand by mode. The disable current at stand by mode varies from a few micro-amperes to tens of micro-amperes (5µA typical). Because oscillation is halted, there is a maximum of 10 ms (same amount of start-up time) before output stabilizes.
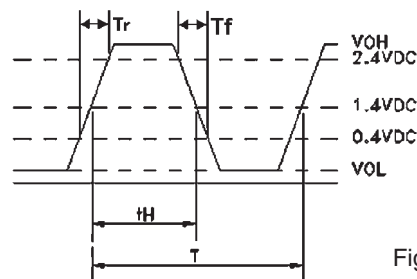
Figure 1

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CMOS RISE AND FALL TIMES

The rise and fall time on the CMOS technology depends on its speed (CMOS, HCMOS, ACMOS, BICMOS), the supply voltage, the load capacitance, and the load configuration. Typical rise and fall time for CMOS 4000 series is 30ns, HCMOS is 6ns, and for ACMOS (HCMOS, TTL compatible) is 3 ns max.

Typical rise and fall time is measured between 10% to 90% of its waveform level.

(See example of Wave Output; Fig. 1.)

OUTPUT
WAVEFORM
Figure 1
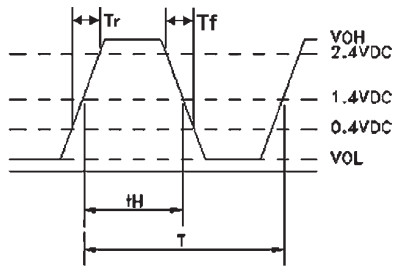
$$Symmetry = \frac{tH}{T} \times 100\%$$

ACMOS OUTPUT TERMINATION TECHNIQUES

Due to the fast transition time of the ACMOS (HCMOS/TTL compatible) device, proper termination techniques must be used when testing or measuring electrical performance characteristics.

Termination is usually used to solve the problem of voltage reflection, which essential cause steps in clock waveforms as well as overshoot and undershoot. Such effect could result in false clocking of data, as well as higher EMI and system noise.

Figure 2
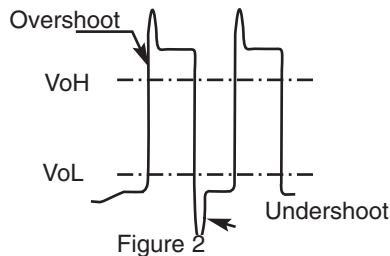
Termination is required also because of the length of the trace on the PC board and its load configuration.

There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

1) Series termination;
2) Pull-up/Pull-down termination;
3) Parallel-AC termination

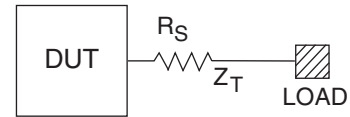**Series termination** (Fig. 3)

Figure 3

$$R_S \geq Z_T - Ro$$

In series termination, a damping resistor is placed close to the source of the clock signal. Value of Rs must satisfy the following requirement:
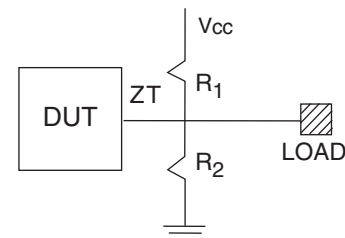
Pull-Up / Pull-Down Resistors (Fig. 4)

Figure 4

In pull-up/pull-down termination, the Thevenin's equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest, and results in no reflections, as well as EMI.

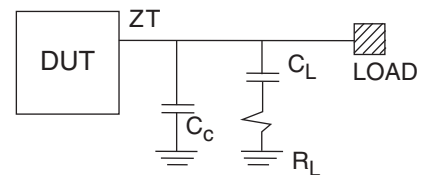$$R_T \sim Z_T$$

Parallel AC Termination (Fig. 5)

Figure 5

In parallel AC termination, a R-C combination is placed at the load. The value of the capacitor must be chosen carefully, usually smaller than the 50pF. This termination is not recommended because it will degrade the rise and fall time of the clock, although it draws no DC current.

Q: Why the Overall frequency stability is specified in crystal oscillators but not in crystals?

A: The crystal oscillator is typically used as a master clock for the microprocessor and its parameters are not affected by the internal characteristics of the microprocessor such as variation in load capacitance and other variables that could affect the change in frequency at room and over temperature. The overall frequency stability in crystal oscillators is typically ±100ppm max. and includes frequency calibration at 25°C, over temperature, frequency changes due to load, supply, aging, vibration, and shock.

Q: What is the start-up time?

A: Start-up time is the delay time between the oscillation starts from noise until it reaches its full output amplitude when power is applied. The supply voltage must be applied with a defined rate or rise. The start-up time varies from microseconds to milliseconds depending on frequency, ASIC speed and logic. Please see figure 1.
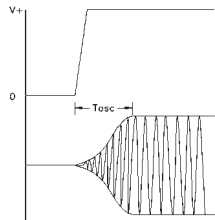
Figure 1

Q: What is Tristate Enable/Disable mode?

A: When the voltage at the control pin is set to a logic low "0", the output is in Tri-state mode that is High Impedance. The disabled current is usually lower than its normal operating current but not completely cut-off as it was seen in the Stand-by mode, where the oscillation is shut down completely.

There is an internal pull-up resistor between control pin and supply (typically 100 kΩ), therefore the control pin can be left open (floating) if unused.

Q: What is jitter and how to specify its maximum value?

A: Jitter is noise caused by many sources in crystal oscillators. Major sources of noise are:

- Power supply noise.
- Integer multiples of the signal source frequency (harmonics).
- Load and termination conditions.
- Amplifier noise.
- Circuit configuration (PLLs, Multiplier, Overtone, etc.)

The following methods can be used to suppress the noise conditions in the above sources:

- Make sure that the power supply noise is filtered by using bypass capacitors, chip beads, or RC filters.
- If jitter is critical in some applications, especially for high-frequencies noise, use low harmonics outputs or sine output.
- Make sure that load and termination conditions are optimized to avoid reflected power back to its output.

- Typically, PLLs, Multiplier or Programmable designs produce higher jitter than the conventional fundamental design.

It is very important to understand the jitter requirements from the application to specify the right specification for crystal oscillators.

We can classify two types of jitters:

- Cycle to cycle jitter
- Period jitter.

CYCLE TO CYCLE JITTER

The Cycle to cycle jitter is the maximum difference in time between several measured periods. Usually a minimum of ten (10) cycles is used where T1 to T10 were recorded . See fig. 2.
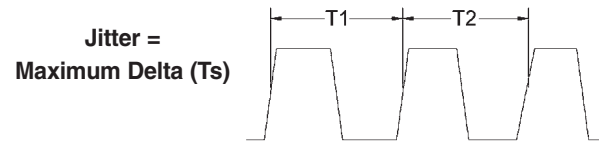
Jitter = Maximum Delta (Ts)

Figure 2

PERIOD JITTER.

The period jitter is the maximum change of a clock edge. It is usually expressed as peak-to-peak jitter and can be converted to rms value by multiplying to (0.5) x (0.707). The period jitter can only be measured at each cycle but not multiple cycles. See figure 3.
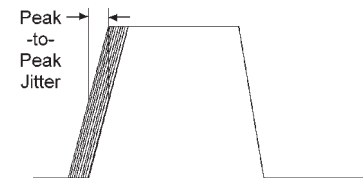
Typical jitter recorded in Abracon oscillators varies from 20ps to 60ps rms.

Figure 3

Q: What is phase noise and how to measure it?

A: Phase noise is the expression of noise in the frequency domain. It is a measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single sideband power density in a 1Hz bandwidth at a specified offset frequency from the carrier.
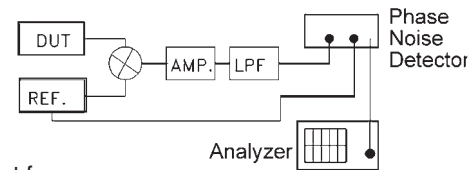
Figure 4

In order to measure phase noise, it is necessary to pair a similar device-under-test with one unit set a VCXO and other set a fixed XO. Please see block diagram in figure 4.

Typical phase noise in Abracon VCXO and oscillators:

OFFSET FREQUENCY (Hz)	PHASE NOISE (dBc/Hz)
10	-70
100	-110
1,000	-125
10,000	-150
100,000	-160

Q: What are the factors that affect frequency pullability?

A: The frequency pullability or deviation in VCXO is the change in the output frequency with respect to change in control voltage. Pullability is usually specified as minimum; however, in some applications, a maximum pulling value is also specified to avoid circuit instability. Please refer to figure 1 for a typical Colpitts VCXO circuit:
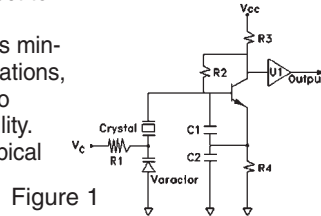
Figure 1

Some major factors that affect the frequency deviation in VCXO:
- Load capacitance value C1 and C2.
- Frequency.
- Crystal characteristics (C1, C0/C1, size)
- Varactor type and capacitance.
- Voltage control Vc.
- Operating temperature.

The frequency pullability can be increased either by using a low capacitance with sharp slope varactor, connect in series another varactor or an inductor, adjusting load capacitor values C1 and C2, or increasing control voltage.
Be very careful when considering any above methods because it may create circuit instability which has a severe effect on jitter, linearity, unwanted modes, frequency hysteresis, or frequency shift over temperature.

Q: What is the typical input impedance?

The input impedance is a function of modulation frequency. Its minimum input impedance is 50kW at 10kHz.

Q: What is the transfer function?

A: The transfer function is the direction of change in frequency versus the change in control voltage. Most applications require a positive transfer function, which the frequency rises when increasing control voltage.

Q: What is linearity and what are the factors that affect it?

A: Linearity is the deviation from the best straight-line slope of the frequency versus control voltage curve. The typical linearity in Abracon VCXO is ±10% maximum for standard pullability. Larger pulling may worsen the linearity.
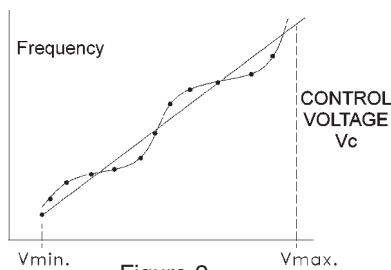
Figure 2

Q: What is the modulation bandwidth?

A: The modulation bandwidth is the minimum ±3dB bandwidth frequency, relative to a 1kHz to 10kHz modulation frequency. Unless otherwise specified as default, other values of modulation bandwidth and frequency must be specified when ordering.

Q: What is the control voltage?

A: The control voltage is the external voltage applied to the input of the VCXO. It consists of a minimum, a maximum, and a center voltage. The center control voltage is the nominal voltage that sets the oscillation frequency to its minimal value.

Standard control voltages:

Vc min = 0.5Vdc; Vc max. = 4.5Vdc; Vc center = 2.5Vdc ± 0.5V

Q: What is a TCXO?

A: A TCXO (Temperature-Compensated Crystal Oscillator) is a crystal oscillator that has a high-precision crystal, a temperature-compensated network. There are several methods to design a compensated network, which could vary from simple, less expensive to, complicate and very expensive:
- **Method 1**: Thermistor/Capacitor networks (Direct compensation). Lowest cost, no varactor needed.
- **Method 2:** Traditional thermistor network.
- **Method 3**: Analog Polynomial Generator
- **Method 4:** Digitally segmented analog
- **Method 5:** Digital compensation
- **Method 6:** Digital compensation with DAC voltage summers.

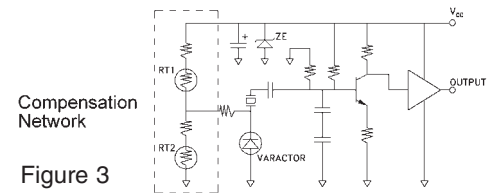Figure 3 shows a traditional thermistor network:

Figure 3

Q: Why and when we need to use a TCXO?

A: We need to use a TCXO when the frequency stability of the oscillator falls beyond the design limitation of a standard simple (fixed) crystal oscillator which is typically less than ±5ppm over a standard or extended temperature window. The TCXO costs more due to its complex circuit and manufacturing.

Q: Why there is an internal trimmer or control voltage on a TCXO?

A: The purpose of the internal trimmer (variable capacitor) or a control voltage is to re-adjust the frequency to its nominal frequency for aging compensation or initial setting.
The internal trimmer is accessible via a hole on top of the TCXO can and can be adjusted with a special tool.
The control voltage can be set with a voltage divider or an external voltage. Both methods of adjustment usually can not produce large frequency deviation rather than 5 to 15ppm enough to offset the frequency due to standard aging.

Q: How to specify frequency stability on a TCXO?

A: Unless otherwise specified, the frequency stability on a TCXO is specified as follows:
- Due to temperature change: ± 2.5ppm @ -20°C to +70°C
- Due to aging: ± 1ppm per year max.
- Due to supply voltage (±5%): ± 0.3ppm max.

The frequency drift due to temperature change is referred to nominal frequency set at 25°C.

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- 59 -

I. ELECTRICAL

1) Supply voltage

Most of Abracon oscillators utilize a CMOS technology ASIC chip with extreme ESD sensitive. When apply power to the oscillator unit, be sure to check the polarities before connecting to the terminals. Reversed polarity connections may cause the unit to be damaged electrically (dead) or mechanically (burn, color change). Pin 1 is usually identified by a black dot marked on cover.

Be sure to apply voltage to the oscillator not exceeding the maximum specified value which is typically 7Vdc max. for most CMOS IC. Applying under rating voltage could result to no or unstable oscillation.

Although many metal can oscillators have built-in bypass capacitors, it is a good practice to add an external bypass

capacitor 0.01µF near the Vdd terminal. The external capacitor is used as an over impressed voltage and overcurrent protective device.
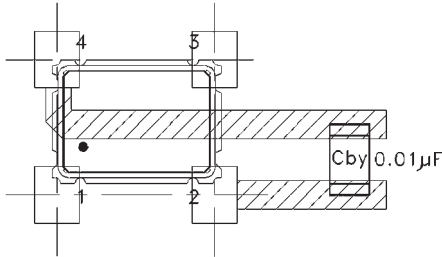

Figure 1

Figure 1
shows a typical layout for a surface-mount crystal oscillator.

2) Load impedance

Oscilloscope impedance shall be greater than 1 MΩ with probe capacitance less than 15pF. The load applied shall include probe capacitance. All lead length should be kept as short as possible especially ground trace. Output trace from oscillator output to the load (next IC) shall be kept short and avoided layout in parallel or cross with another hot signal trace. Stray capacitance and inductance have major effects on output impedance of the oscillator unit and shall be minimized.

3) Output frequency

Output frequency shall be measured with a precision frequency counter using a reference external time base. Make sure to stabilize the crystal oscillator (warm-up) before recording the final frequency value, especially on high frequency and high current units.

II. MECHANICAL

1) Vibration and shock

Do not apply or cause sudden shock and vibration exceeding its maximum specifications to the unit. Severe drop or

hit with a hard object could damage the unit electrically and mechanically. Please check the unit if dropped before assembling or using.

2) Mounting

The following precautions shall be applied during mounting through-hole crystal oscillators:

• Do not force spreading the terminals into socket or PCB holes. This will avoid breaking the glass insulation on terminals.

• Do not apply excessive soldering heat or soldering duration on terminals.

• When bending leads for surface-mount, be very careful to use appropriate tool keeping a safe distance between the terminal base and the bent area.

The following precautions shall be applied to all surface-mount oscillators:

• Use the appropriate reflow condition as recommended on the unit specification. Please make sure to not exceed the peak temperature, its maximum duration, the number of exposures, the rate of temperature change vs. time, etc.

3) Cleaning

Do not use solvents not recommended to clean to avoid discoloration or damage on ink marking permanency. Some solvents, which contain Chlorine, may cause some color discoloration on some metallic cover.

Do not exceed the maximum recommended temperature when cleaning.

III. PACKAGING

Although an anti-static protection circuit is built-in the ASIC, excessive static electricity level may damage the unit. Abracon uses conductive packing materials for all oscillators. By sure to ground with ESD strap before handling the device.

IV. HANDLING UNUSED TERMINALS

Some Abracon oscillators include Tristate function. Although there is an internal pull-up resistor to prevent floating, it is recommended to terminate the tristate terminal to Vdd with a resistor of 100 kΩ in series.

V. STORING

Please store all units at normal temperature and humidity. High humidity may cause deterioration to units. Avoid storing over a long period. Please perform visual and electrical inspections before using once the units are stored over a long period.

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