Li+ Battery Charger and Low Dropout Linear Regulator Combo

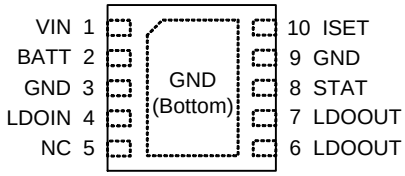
Features

- **Programmable Charge Current Up to 700mA**
- **Charge Status Output Pin**
- **Soft-Start Limits Inrush Current**
- **4.2V Charge Termination Voltage with ±1% Accuracy**
- **45mA Pre-charge Current (R_{SET}=2k)**
- **Thermal Regulation of Charge Current Simplifies Board Design**
- **Charger Enable/Disable Control**
- **Ultra Low Regulator Quiescent Current: 4μA**
- **Fixed LDO Regulator Output Voltage: 3.3V**
- **Low Regulator Dropout Voltage: 200mV@150mA**
- **LDO Regulator Current Limit Protection**
- **LDO Regulator Short Circuit Current Limit**
- **LDO Regulator Thermal Protection**
- **Small 3mmx3mm DFN 10-Pin (DFN-10) Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **PDAs**
- **MP3 Players**
- **Cell Phones**
- **Wireless Appliances**

Pin Configuration



APL3207
DFN-10 3x3 Top View

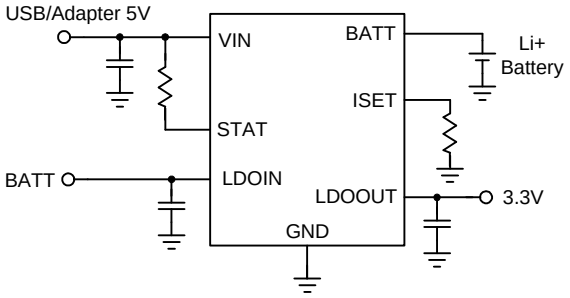
General Description

The APL3207 combines a constant-current/constant-voltage linear single cell Li+ battery charger with a low dropout linear regulator. Both charger and linear regulators can work independently. The small DFN-10 package and low external component count make the APL3207 ideally suit to portable applications.

The charger of APL3207 provides 0.7A charge current with thermal regulation protection to optimize the board design for compact size and typical thermal conditions. When the junction temperature reaches the thermal regulation threshold, the charger does not shut down but simply reduces the charge current. The charge current can be programmed by connecting an external resistor from the ISET pin to the GND. Using an external MOSFET to disconnect the resistor from the ground shuts down the charger, and reduces the input current down to 25μA. The APL3207 also has the STAT pin to indicate charge status.

The LDO regulator of APL3207 can deliver up to 150mA current and dropout voltage is only 200mV. The 4μA low quiescent current makes it ideally suit to battery-power systems. The LDO regulator also has built-in current limit and thermal shutdown protection.

Simplified Application Circuit



Ordering and Marking Information

APL3207 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QA : DFN3x3-10
Operating Ambient Temperature Range
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device G : Halogen and Lead Free Device

APL3207 QA :

APL
3207
XXXXX

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{LDOIN}	VIN, VLDOIN to GND Voltage	-0.3 to 7	V
V_{SET}, V_{STAT}, V_{BATT}	ISET, STAT, BATT to GND Voltage	-0.3 to 7	V
I_{CHG}	Charge Current	800	mA
P_D	Power Dissipation	Internally Limited	W
T_J	Maximum Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristic (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Resistance in Free Air DFN3x3-10	50	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of DFN-10 is doldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN to GND Voltage	4.35 to 6.5	V
I_{CHG}	Charge Current	0.1 to 0.7	A
V_{LDOIN}	LDOIN to GND Voltage	3.6 to 6.5	V
I_{LDO}	LDO Output Current	0 to 0.15	A
T_A	Ambient Temperature	-40 to 85	°C
T_J	Junction Temperature	-40 to 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, V_{LDOIN}=5V, T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3207			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{IN}	VIN Supply Current	Charge mode, R_{SET}=10k	-	300	600	µA
		Standby mode (Charge terminated)	-	200	500	
		Shutdown mode (R_{SET} not connect, V_{IN}<V_{BATT}, or V_{IN}<V_{UVLO})	-	25	50	
I_Q	LDO Regulator Quiescent Current	I_{OUT}=0mA	-	4	7	µA
		I_{OUT}=150mA	-	4	10	
BATT REVERSE CURRENT						
I_{BATT}	BATT Standby Input Current	Standby mode, V_{BATT}=4.2V	0	2.5	6	µA
	BATT Shutdown Input Current	Shutdown mode (R_{SET} not connected)	-	-	1	
	BATT Sleep Input Current	Sleep mode, V_{IN}=0V	-	-	1	
UNDER-VOLTAGE LOCKOUT						
V_{UVLO}	VIN UVLO Threshold	V_{IN} rising	3.75	3.85	3.95	V
	VIN UVLO Hysteresis		0.15	0.20	0.30	V
BATTERY VOLTAGE AND THRESHOLD VOLTAGE						
V_{TERM}	BATT Charge Termination Voltage		-	4.20	-	V
	BATT Charge Termination Voltage Accuracy	T_A=25 °C, V_{IN}=4.35~6.5V	-0.5	-	0.5	%
		T_A=-40~85°C	-1	-	1	
	BATT Pre-charge Threshold Voltage		2.8	2.9	3.0	V
	BATT Pre-charge Hysteresis Voltage		60	80	110	mV
V_{ASD}	V_{IN}-V_{BATT} Lockout Threshold Voltage	V_{IN} from low to high	80	120	160	mV
		V_{IN} from high to low	40	80	120	
$V_{RECHARGE}$	Recharge Battery Threshold Voltage		3.9	4.05	4.2	V
V_{MSD}	Manual Shutdown Threshold Voltage	V_{SET} rising	1.15	1.21	1.3	V
		V_{SET} falling	0.9	1.0	1.1	
BATTERY CHARGING AND PRE-CHARGE CURRENT						
I_{CHG}	Charging Current	R_{SET}=10k Without thermal regulation	91	100	109	mA
		R_{SET}=2k Without thermal regulation	455	500	545	
V_{SET}	ISET Regulation Voltage	Without thermal regulation	-	1	-	V
	ISET Regulation Voltage Accuracy	T_J=-40~125°C, V_{IN}=4.35~6.5V	-0.7	-	0.7	%
	ISET Pull-Up Current	V_{SET}=1V, T_A=25 °C	-	2.5	-	µA
K_{SET}	Charging Current Set Factor	0.1A≤ I_{CHG} ≤0.7A	940	1000	1060	
	Pre-charging Current	V_{BATT}<2.8V, R_{SET}=2k	20	45	70	mA
I_{TERM}	C/10 Termination Current Threshold	R_{SET}=2k to 10k	8.5	10	11.5	%

Electrical Characteristics

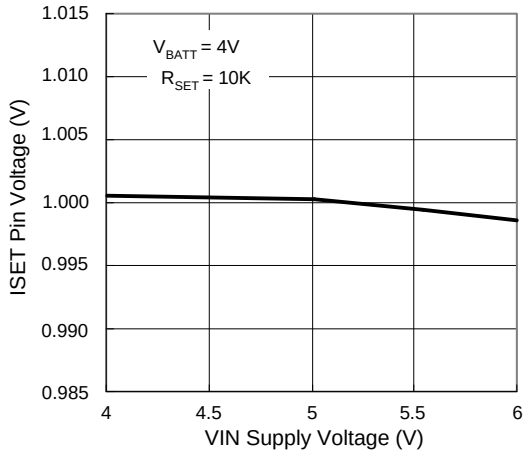
Refer to the typical application circuit. These specifications apply over V_{IN}=5V, V_{LDOIN}=5V, T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3207			Unit
			Min.	Typ.	Max.	
CHARGER DROPOUT VOLTAGE						
	Power FET On Resistance		-	800	1200	mΩ
	V_{IN} to V_{BATT} Dropout Voltage	I_{CHG}=0.5A, V_{IN}=5V	-	400	600	mV
STAT PIN AND THERMAL REGULATION						
V_{STAT}	STAT Output Low Voltage	I_{STAT}=5mA	-	0.35	0.6	V
	STAT Off-leakage Current	V_{STAT}=5V	-	-	1	μA
T_{LIM}	Thermal Regulation Threshold		-	120	-	°C
SOFT-START AND TIMING						
T_{SS}	Charge Current Soft-Start Interval	I_{CHG}=0A to full charging current T_A=25 °C	-	100	-	μs
$T_{RECHARGE}$	Recharge Comparator Filter Time	V_{BATT} high to low	0.75	2	4.5	ms
T_{TERM}	Termination Comparator Filter Time	I_{CHG} falling below I_{CHG}/10	0.4	1	2.5	ms
REGULATOR OUTPUT VOLTAGE						
V_{LDOOUT}	LDO Regulator Output Voltage		3.234	3.300	3.366	V
REG_{LINE}	LDO Regulator Line Regulation	V_{LDOOUT}+0.5V<V_{LDOIN}<6V	-	2	10	mV
REG_{LODE}	LDO Regulator Load Regulation	0mA<I_{LDO}<150mA	-	15	30	mV
V_{DROP}	LDO Regulator Dropout Voltage	I_{LDO}=150mA	-	200	300	mV
PSRR	LDO Regulator Power Supply Ripple Rejection Ratio	f=1kHz, I_{LDO}=10mA	30	40	-	dB
	LDO Regulator Output Noise	f=22KHz to 80kHz, I_{LDO}=10mA	-	200	250	μV_{RMS}
REGULATOR PROTECTION						
I_{LIM}	LDO Regulator Output Current Limit		200	300	400	mA
I_{SHORT}	LDO Regulator Short Circuit Current	V_{LDOOUT}=0V	40	50	60	mA
	Regulator Thermal Shutdown Temperature		-	135	-	°C
	Regulator Thermal Shutdown Hysteresis		-	20	-	°C

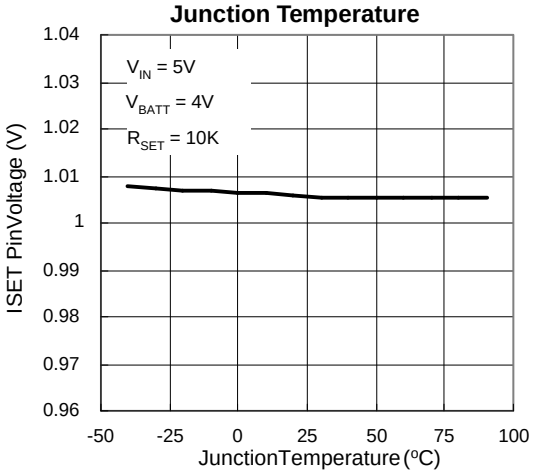
Typical Operating Characteristics

(Refer to the section "Typical Application Circuits", V_{IN}=5V, V_{LDOIN}=5V, T_A=25°C, unless otherwise specified)

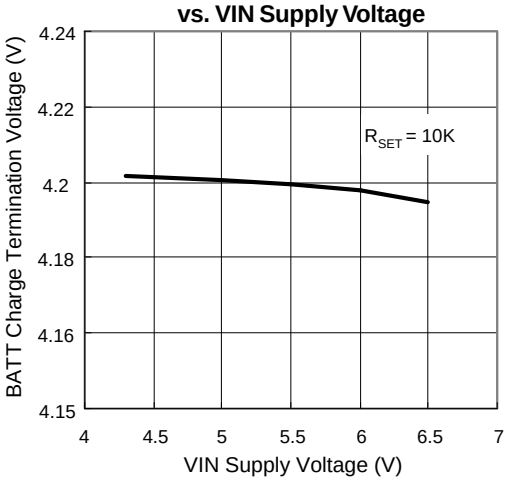
ISET Pin Voltage vs. VIN Supply Voltage



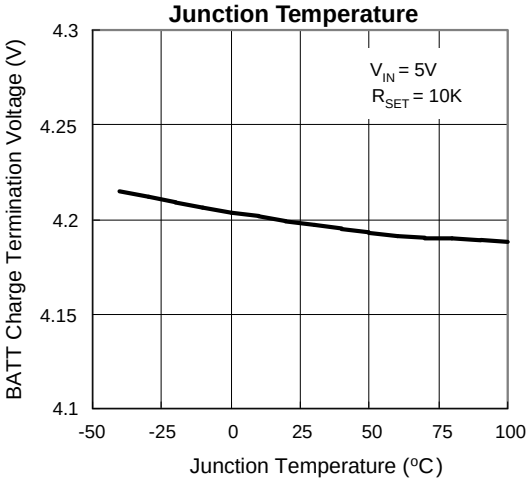
ISET Pin Voltage vs. Junction Temperature



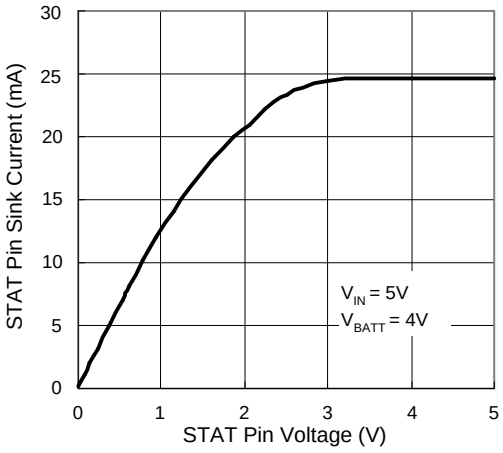
BATT Charge Termination Voltage vs. VIN Supply Voltage



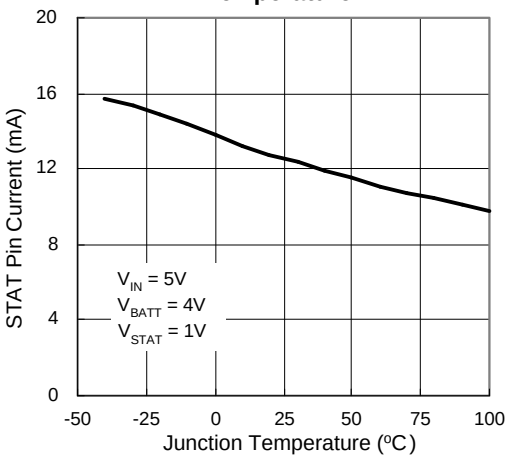
BATT Charge Termination Voltage vs. Junction Temperature



STAT Pin I-V Curve



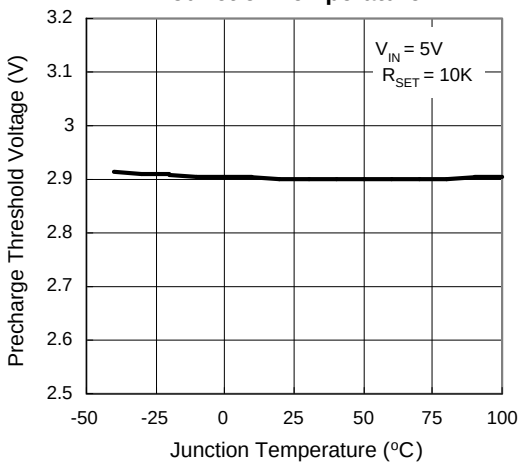
STAT Pin Current vs. Junction Temperature



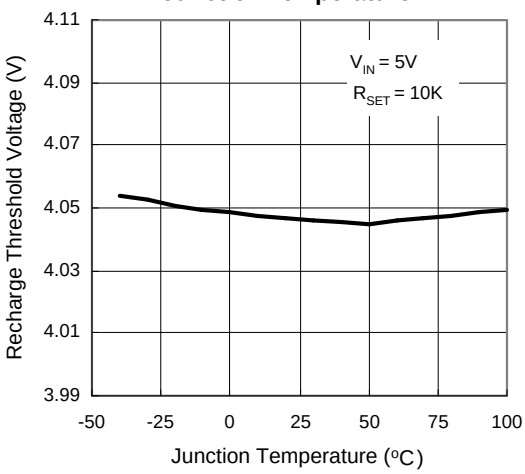
Typical Operating Characteristics (Cont.)

(Refer to the section "Typical Application Circuits", V_{IN}=5V, V_{LDOIN}=5V, T_A=25°C, unless otherwise specified)

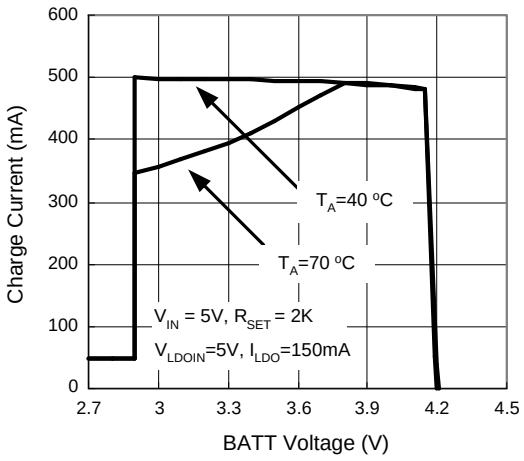
Precharge Threshold Voltage vs. Junction Temperature



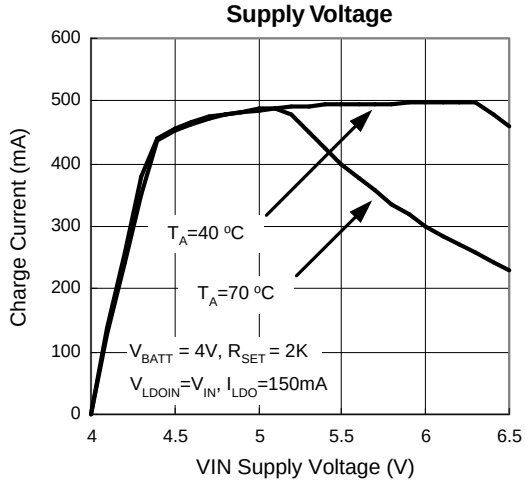
Recharge Threshold Voltage vs. Junction Temperature



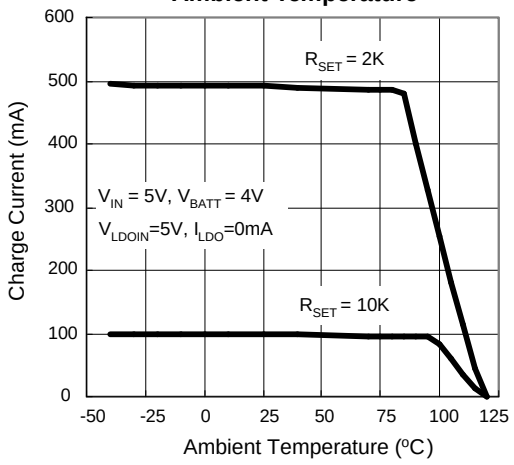
Charge Current vs. BATT Voltage



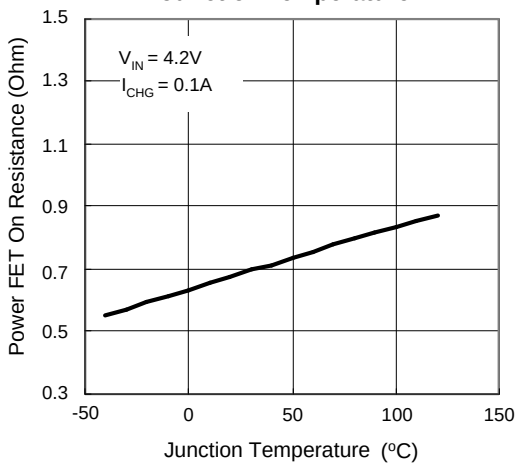
Charge Current vs. VIN Supply Voltage



Charge Current vs. Ambient Temperature



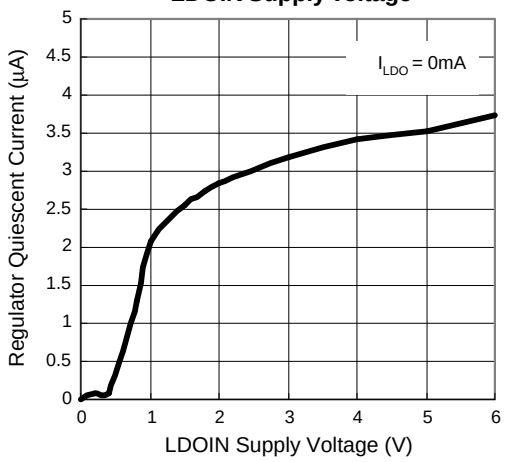
Power FET On Resistance vs. Junction Temperature



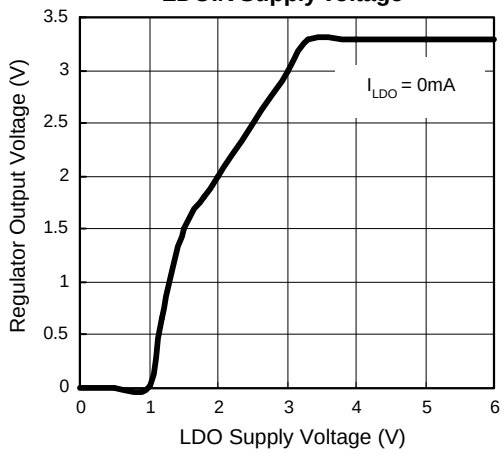
Typical Operating Characteristics (Cont.)

(Refer to the section "Typical Application Circuits", V_{IN}=5V, V_{LDOIN}=5V, T_A=25°C, unless otherwise specified)

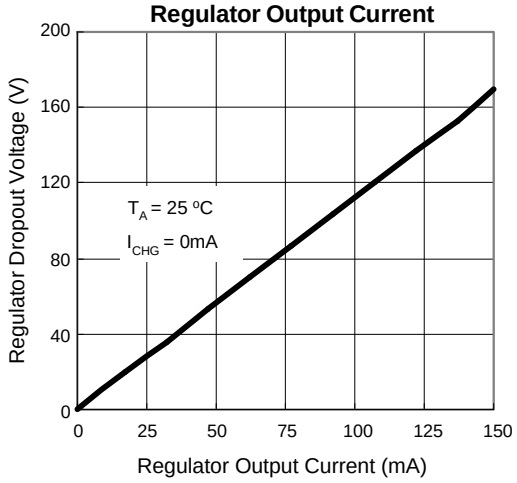
Regulator Quiescent Current vs. LDOIN Supply Voltage



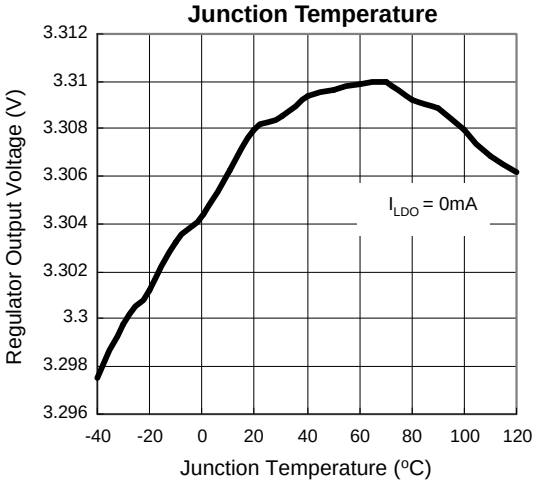
Regulator Output Voltage vs. LDOIN Supply Voltage



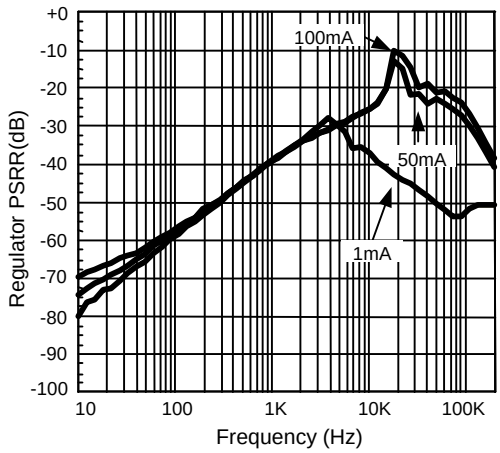
Regulator Dropout Voltage vs. Regulator Output Current



Regulator Output Voltage vs. Junction Temperature



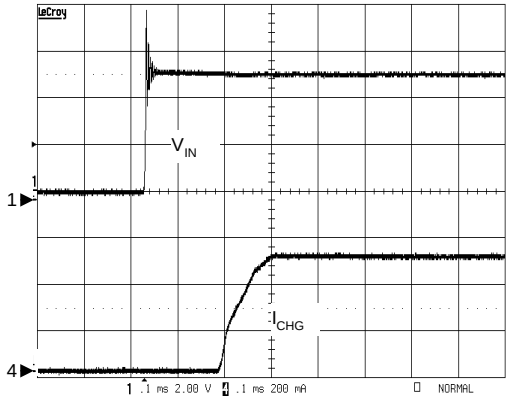
Regulator PSRR vs. Frequency



Operating Waveforms

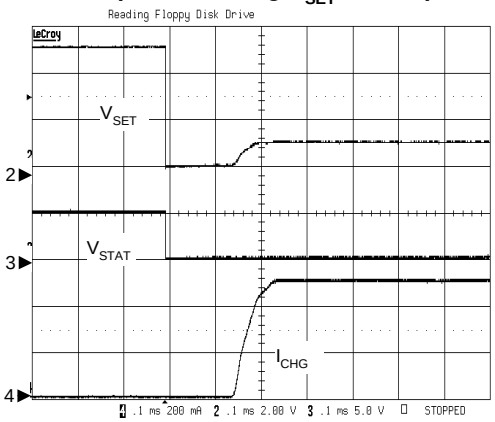
(Refer to the section "Typical Application Circuits", the test condition is V_{IN}=5V, T_A=25°C, unless otherwise specified)

V_{IN} Power On



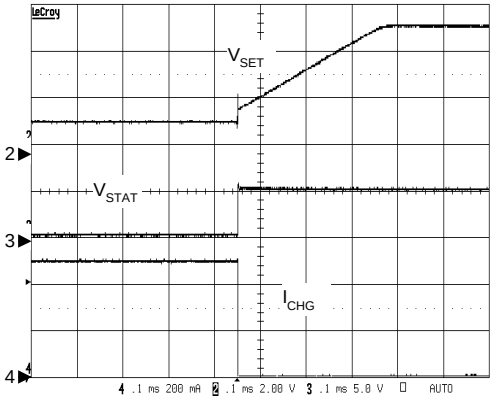
R_{SET} = 2K, V_{BATT}=3.8V
CH1: V_{IN}, 2V/div, DC
CH4: I_{CHG}, 0.2A/div, DC
TIME: 0.1ms/div

Charger Start-up (Reconnecting R_{SET} to GND)



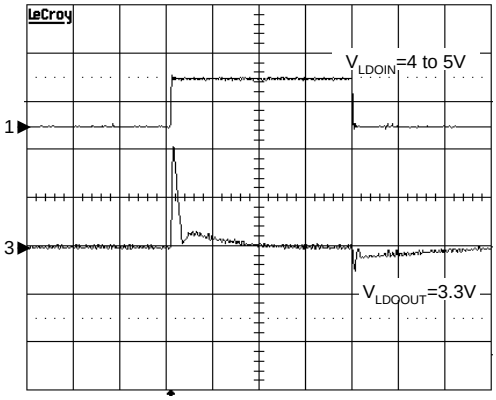
R_{SET} = 2K, V_{BATT}=3.8V
CH2: V_{SET}, 2V/div, DC
CH3: V_{STAT}, 5V/div, DC
CH4: I_{CHG}, 0.2A/div, DC
TIME: 0.1ms/div

Charger Shutdown (Disconnecting R_{SET} from GND)



R_{SET} = 2K, V_{BATT}=3.8V
CH2: V_{SET}, 2V/div, DC
CH3: V_{STAT}, 5V/div, DC
CH4: I_{CHG}, 0.2A/div, DC
TIME: 0.1ms/div

LDO Line Transient Response

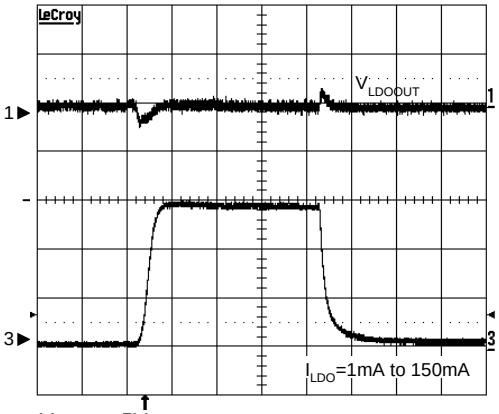


I_{LDO} = 10mA
CH1: V_{LDOIN}, 1V/div, AC
CH3: V_{LDOOUT}, 200mV/div, AC
TIME: 0.1ms/div

Operating Waveforms (Cont.)

(Refer to the section "Typical Application Circuits", the test condition is V_{LDOIN}=5V, T_A=25°C, unless otherwise specified)

LDO Load Transient Response

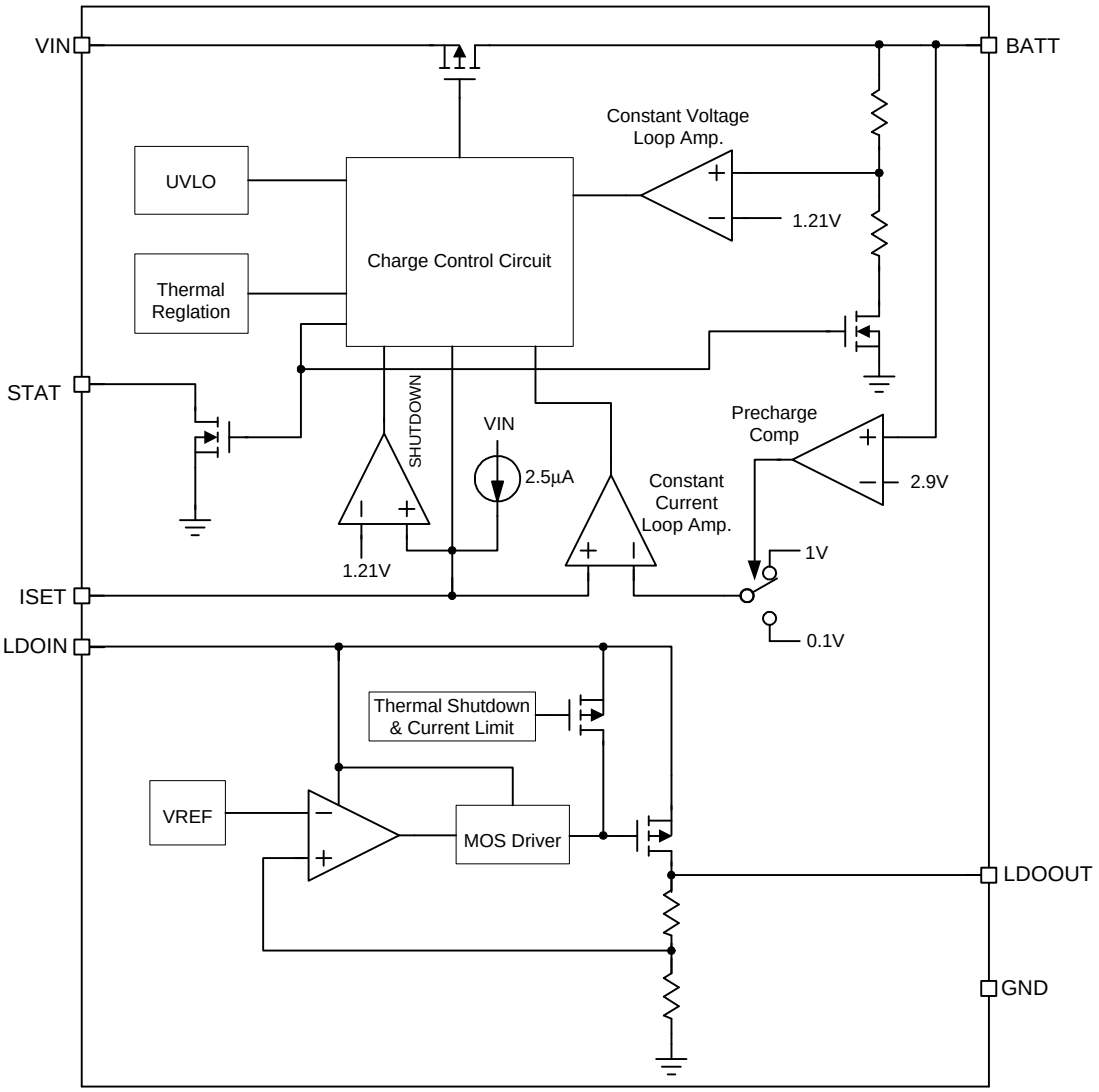


V_{LDOIN} = 5V
CH1: V_{LDOOUT}, 50mV/div, AC
CH3: I_{LDO}, 50mA/div, DC
TIME: 0.5ms/div

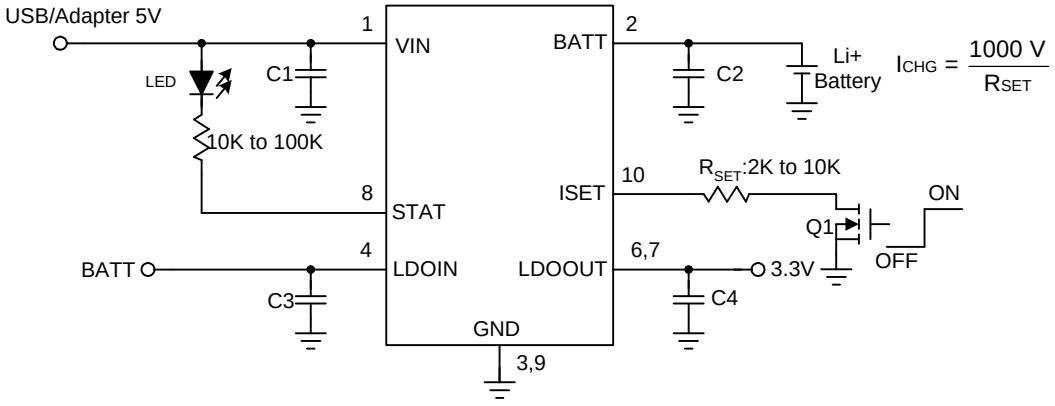
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Charger Input Supply Pin. Provides power to the charger, V_{IN} can range from 4.35V to 6.5V and should be bypassed with at least a 1µF capacitor.
2	BATT	Charger Output Pin. Connect this pin to the positive terminal of a Li+ battery.
4	LDOIN	LDO Regulator Input Supply Pin. Provides power to the regulator, V_{LDOIN} can range from 3.6V to 6.5V and should be bypassed with at least a 1µF capacitor.
5	NC	No Connection.
6,7	LDOOUT	LDO Regulator Output. Fixed at 3.3V output, sourcing up to 150mA. The pin6 and pin7 must be connected together.
8	STAT	Open-Drain Charge Status Output Pin. When the battery is charging, the STAT pin is pulled low by an internal switch. In other states the STAT pin is in a high impedance state.
3,9	GND	Ground. Pin3 and pin9 must be connected together.
10	ISET	Charging Current Setting and Shutdown Pin. Connecting a resistor from this pin to GND set the charge current when the VIN is powering the charger. Disconnecting the R_{SET} from GND allows an internal 2.5µA current to pull the ISET pin high, and when the ISET pin voltage exceeds the shutdown threshold voltage, the charger enters shutdown mode.
Bottom Pad	GND	Ground. Connect the bottom side metal pad to back side ground plane through several vias to improve power dissipation.

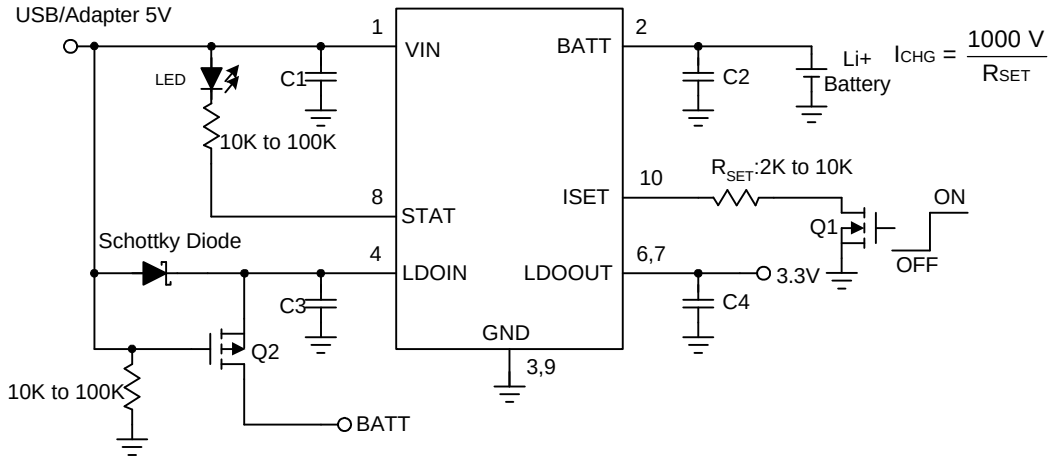
Block Diagram



Typical Application Circuit



The input power of LDO regulator is supplied by battery



When USB is present, the input power of LDO is supplied by USB

Designation	Description
C1, C3, C4	1µF, 10V, X5R, 0402 Murata GRM155R61A105KE15
C2	2.2µF, 6.3V, X5R, 0402 Murata GRM155R60J225ME15
Q1	SOT-23, N-Channel MOSFET ANPEC APM2300CA
Q2	SOT-23, P-Channel MOSFET ANPEC APM2301CA

Murata website: www.murata.com

Function Description

Charge Cycle

When the APL3207 is powered with a battery connected, the IC firstly detects if the cell voltage is ready for full charge current. If the battery voltage is below pre-charge threshold (2.9V typ.), the device supplies 1/10 the programmed charge current. On the contrary, when the battery voltage is over the pre-charge threshold, the device supplies the full charge current, as programmed by R_{SET} from the ISET pin to the GND. When the battery voltage approaches the 4.2V termination voltage, the device enters constant-voltage mode and the full charge current gradually decreases until the charge current drops to the termination current threshold, which is equal to 1/10 full charge current, and the IC stops charging (See Figure 1).

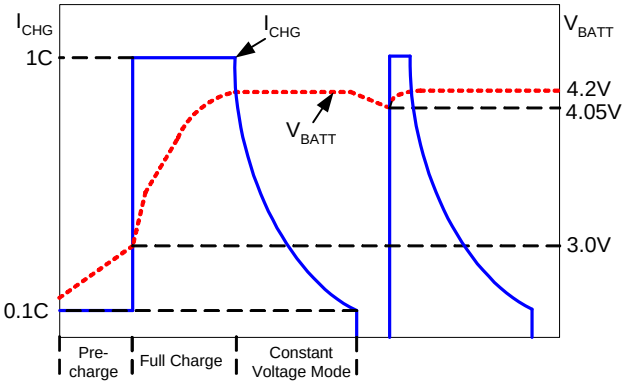


Figure 1. Typical Charging Profile

Full Charge Current Setting

The full charge current is programmed by connecting a resistor from the the ISET pin to the ground. The full charge current is 1000 times of the current flowing out of the ISET pin and can be calculated by the following equation:

$$I_{CHG} = \frac{K_{SET} \times V_{SET}}{R_{SET}}$$

where:

V_{SET} is ISET regulation voltage (1V, typcial).

K_{SET} is the charge current set factor (1000, typical).

The charge current set factor and the ISET regulation voltage are shown in the Electrical Characteristics. The ISET regulation voltage is reduced by the thermal regulation function.

Charge Termination Detection and Recharge

Charging is terminated when I_{CHG} falls to 10% of the full charge current set by R_{SET} and the charger is in voltage mode (V_{BATT} is nearly 4.2V). The charge termination is detected by monitoring the ISET pin. When the ISET pin voltage falls below 0.1V and takes longer than T_{TERM} (1ms, typical), charging is terminated. The STAT output keeps high state when the charger operates in standby mode. After charge termination, the battery voltage is monitored by the APL3207 continuously. If the battery voltage drops below 4.05V and takes longer than $T_{RECHARGE}$ (2ms, typical), a new charge cycle starts to recharge the battery.

Manual Shutdown

The ISET pin provides two functions: connecting the resistor R_{SET} from the ISET pin to the GND to set the full charge current; and disconnecting the R_{SET} from the GND to shut down the charging device. Once the R_{SET} is disconnected, an internal 2.5μA current will pull the ISET pin high. When the ISET pin voltage reaches the 1.21V shutdown threshold voltage, the charging device enters shutdown mode. In shutdown mode, the charging stops, the VIN supply current drops to 25μA and the battery drain current is below 1μA. Reconnecting R_{SET} to the GND enables the charger to operate normally. The STAT output is in high state when the charger is in shutdown mode.

Thermal Regulation

The APL3207 is thermally regulated to keep the junction temperature at 120°C. When the junction temperature reaches 120°C, the charger does not shut down but reduces charge current to keep the junction temperature at 120°C. This feature protects the APL3207 from excessive temperature and allows the charger to operate with maximum power dissipation by reducing the charge current and optimizes the board design for compact size and typical thermal conditions.

Charge Status Output (STAT)

The STAT is an open-drain output. When the charger is in charge mode, the STAT output is in pull-low state. Until the charge current drops to the termination current threshold, the charging stops, and the STAT output is in high impedance state.

Function Description (Cont.)

Charge Status Output (STAT) (Cont.)

STAT Output	Mode	V_{IN}	V_{BATT}	V_{SET}
Low	Charge mode	VIN>VUVLO & VIN>VBATT+VASD	VBATT<4.2V	0.1V<VSET<1.2V
High	Shutdown mode	VIN>VUVLO & VIN>VBATT+VASD	-	VSET>1.2V
	Standby mode		VBATT>4.2V	-
	Sleep mode	VIN<VUVLO or VIN<VBATT+VASD	Battery is connected	-

Table1. STAT Pin Summary

LDO Regulator

The APL3207 has been built in a regulator whose output voltage is fixed at 3.3V. When the system is powered by a battery, the regulator is fully powered by the battery; however, when the battery is charged, the regulator input is switched to the USB or adapter (by using external circuit) and powered by the USB or adapter, which reduces the charging time.

Regulator Current Limit and Short Circuit

The APL3207 includes a current limit circuitry for LDO regulator. The current limit circuitry senses the output current and limits the maximum output current to prevent the APL 3207 and external loads form being damaged. The point where limitation occurs is I_{LDO}=300mA (typical). When the output is shortened to the ground, the regulator reduces the current-limit threshold down to 50mA (typical). The output can be shortened to the ground for an indefinite amount of time without damaging the part.

Regulator Thermal Protection

The LDO regulator has a built-in thermal protection function. When the junction temperature exceeds +135°C, the thermal sensor generates a logic signal to turn off the regulator which makes the die cool down. When the junction temperature cools down by 20°C, the thermal sensor turns the regulator on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions.

Application Information

Input Capacitors

The APL3207 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. The 1μF ceramic capacitors are recommended to place on the input supply pins (VIN and VLDOIN) to the GND. Place the capacitors as close as possible to the input supply pins for well operation. In some start-up conditions, it may necessary to protect the device against a hot plug input voltage. Adding a 6V input zener diode between the input supply pins and the GND clamps the input voltage peak.

Output Capacitors

The APL3207 has two output pins, which are charger output pin BATT and regulator 3.3V output pin LDOOUT. The output capacitor of charger is recommended to use 2.2μF ceramic capacitor to ensure the battery charge stability.

The output capacitor of regulator also can use ceramic capacitor, and its proper value is between 1μF and 2.2μF, ESR must above 10mΩ. Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. With X5R and X7R dielectrics, 1μF is sufficient at all operating temperatures.

STAT Pin

The STAT pin can be used to drive a LED or communicate with the host processor to show the charge status. When the status is displayed by a LED, which has a current rating less than 5mA, a resistor should be selected to connect LED in series, for programming at the desired current value. The resistor is calculated by the following equation:

$$R_{LED} = \frac{V_{IN} - V_{LED-ON}}{I_{LED}}$$

When STAT pin is monitored by a processor, there should be a 10kΩ to 100kΩ pull-up resistor to connect the STAT pin and the supply voltage of the processor.

Thermal Consideration

The most common measurement of package thermal performance is thermal resistance measured from the device junction to the air surrounding the package surface (θ_{JA}). The θ_{JA} can be calculated by the following equation:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

where:

T_J= device junction temperature, maximum T_J=120°C

T_A= ambient temperature

P_D= device power dissipation

The device power dissipation, P_D, is a function of the charge rate, the LDO output current and the voltages drop across the internal FETs.

It can be calculated by the following equation:

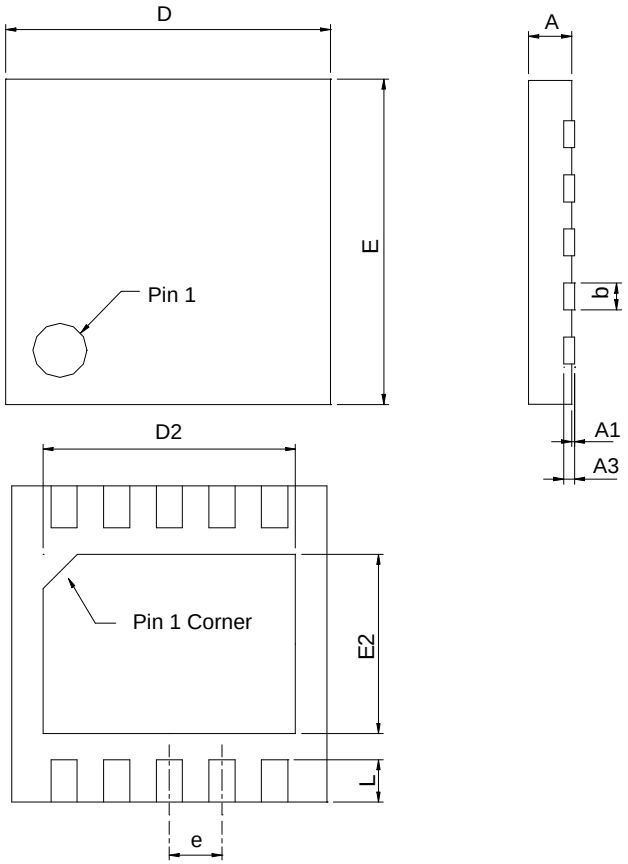
$$P_D = (V_{IN} - V_{BATT}) \times I_{CHG} + (V_{LODIN} - V_{LDOUT}) \times I_{LDO}$$

PCB Layout Consideration

Connecting the battery to BATT as close as possible provides accurate battery voltage sensing. The input and output decoupling capacitors and the programmed resistor R_{SET} should be placed as close as possible to the device. The high current paths (VIN and LDOIN pins for input and BATT and LDOOUT pins for output) must be short and wide to minimize voltage drop.

Package Information

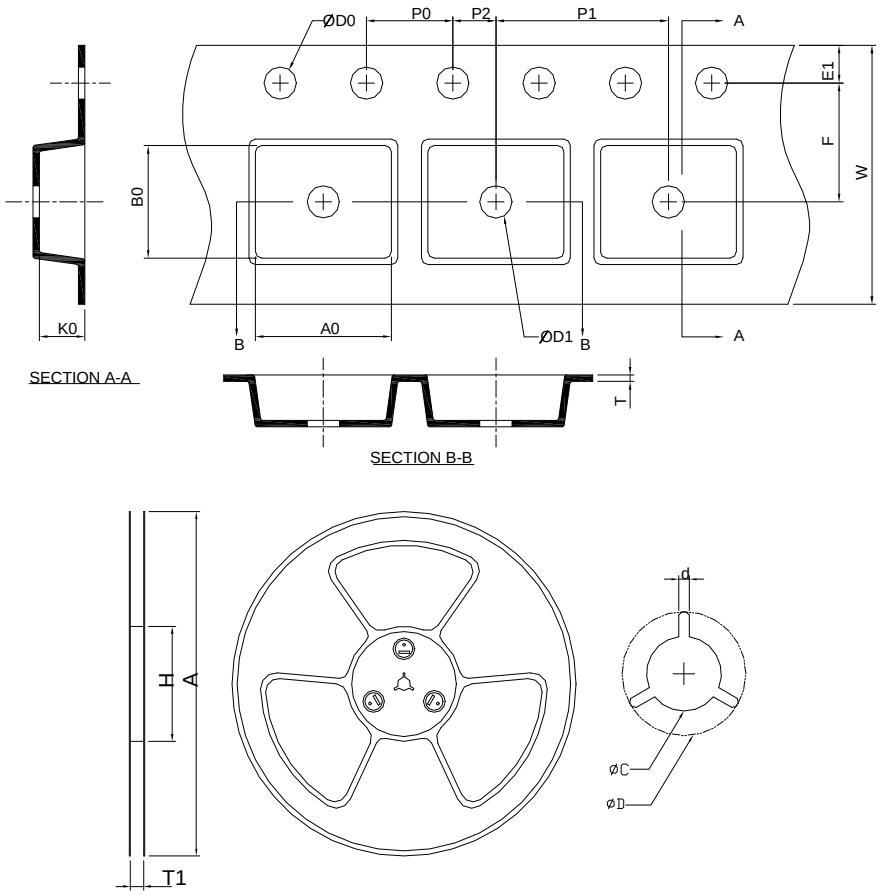
DFN3x3-10



SYMBOL	DFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
DFN3x3-10	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

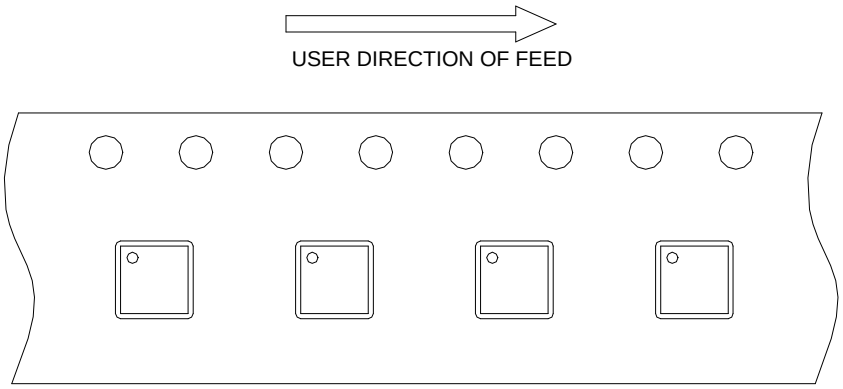
(mm)

Devices Per Unit

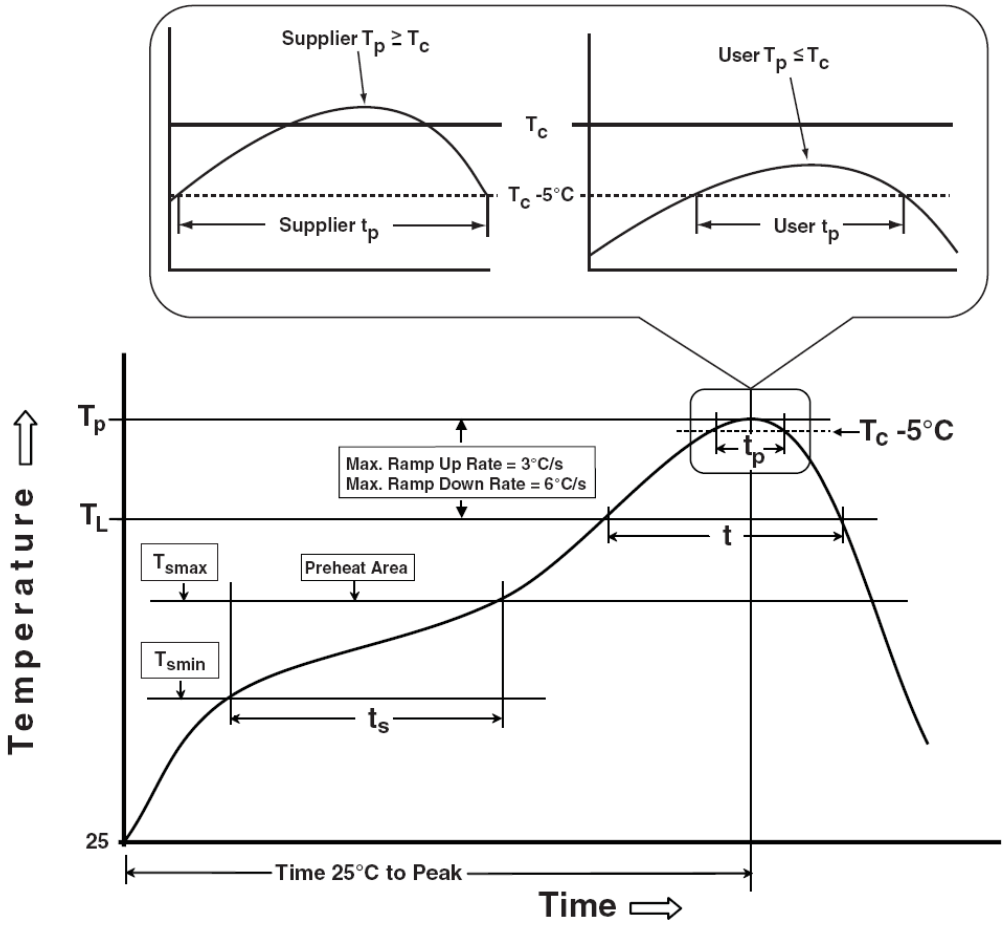
Package Type	Unit	Quantity
DFN3x3-10	Tape & Reel	3000

Taping Direction Information

DFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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