BW6562A High PFC LED Driver

Features

- **Single stage fly-back controller with PFC**
- **Transition-mode operation**
- **Ultra-low start-up current**
- **Internal start-up timer**
- **Low operating supply current**
- **Low quiescent current**
- **Disable function on error amplifier (E/A) input**
- **Totem pole, push-pull output drive**
- **Adjustable output over-voltage protection**
- **Under-voltage lockout with hysteresis**
- **1% Precision internal reference voltage**

Typical Applications

- **Fly-back power converters**
- **PFC pre-regulators to meet IEC61000-3-2**
- **Hi-end AC-DC adapter/charger**
- **Electronic single stage LED driver**
- **Electronic Ballast**

Product Description

The BW6562A is a cost effective high performance transition-mode (TM) power factor correction (PFC) controller IC optimized for high PFC LED driver, battery chargers and pre-regulator applications. The BW6562A integrates an internal start-up timer, a highly linear multiplier with Total Harmonics Distortion (THD) optimizer for near unity power factor, a Zero Current Detector (ZCD) to ensure transition-mode operation and a current sensing comparator with built-in leading edge blanking. With ZCD control, power MOSFET is always turned on with zero inductor current. Consequently, transition-mode control achieves lower switching loss and reduced noise. The BW6562A offers great protection coverage including system accurate adjustable over-voltage protection (OVP), input under-voltage lockout (UVLO), multiplier output clamp and GD output clamp for external power MOSFET protection. The totem pole output stage is capable of delivering sink/source drive current of +800mA/-600mA.
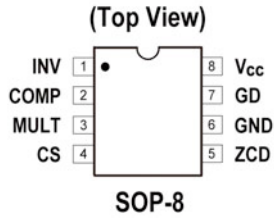
The BW6562A is available in SOP-8 package.

Typical Application Circuit
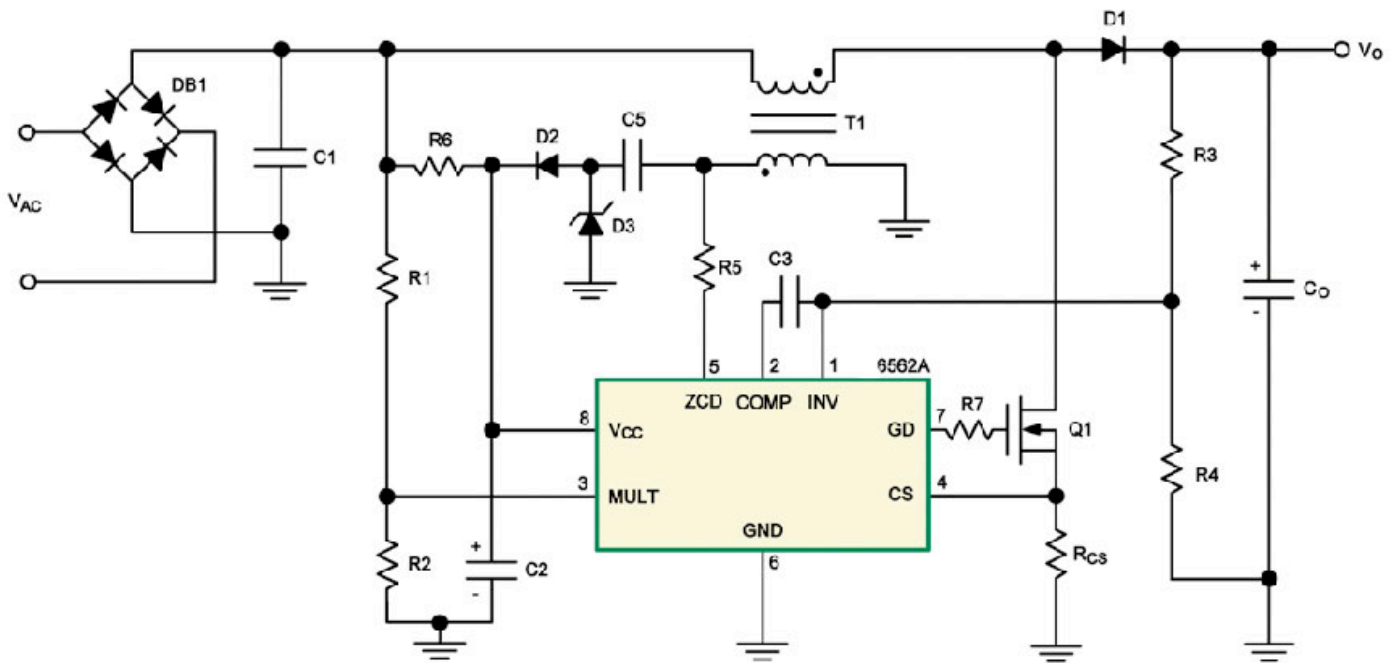
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Pin Assignments and Ordering Information

(Top View)

```
        ┌──┐
INV  [1] •      [8]  Vcc
COMP [2]        [7]  GD
MULT [3]        [6]  GND
CS   [4]        [5]  ZCD
```

SOP-8

Device	Packaging	Quantity of Tape & Reel
BW6562A MST	SOP-8	3000

Pin Descriptions

Pin No.	Pin Name	Function
1	INV	**Inverting input pin of the error amplifier.**
		The information on the output voltage of the PFC controller is fed into this pin through a resistor divider. The pin can also be used as chip enable/disable control pin.
2	COMP	**Output pin of the error amplifier.**
		A compensation network is placed between this pin and INV to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	**Main input to the multiplier.**
		This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	**Current sense input pin to the internal PWM comparator.**
		The current flowing in the MOSFET is sensed through a resistor; the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to switch on or off the external MOSFET. The pin is equipped with 200ns leading-edge blanking for improved noise immunity.
5	ZCD	**Zero current detection pin.**
		Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	**Ground pin.**
		Current return for both the signal part of the IC and the gate driver.
7	GD	**Gate driver output pin.**
		The totem pole output stage is able to drive power MOSFET's with a peak current of 600mA source and 800mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high V_{CC}.
8	V_{CC}	**System power input pin.**
		Supply voltage of both the signal part of the IC and the gate driver. Upper limit is extended to a maximum of 32V to provide a more headroom for supply voltage changes. This pin has an internal 34V (min.) Zener diode to protect the IC itself from over-voltage transients.

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Absolute Maximum Ratings [(Note 1)]

Symbol	Parameter	Ratings	Unit
V_{CC}	IC supply voltage	-0.3 ~ +40	V
I_{GD}	Output totem pole peak current	-600 (source) / +800 (sink)	mA
* [(Note 2)]	Analog inputs & outputs	-0.3 ~ +8.0	V
I_{ZCD}	Zero current detector maximum current	±10	mA
	Continuous power dissipation (T_A = +25°C) 8 Pin SOP (de-rating 6.3mW/°C above +25°C)	0.63	W
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 ~ +150	°C
θ_{JA}	Junction-to-ambient thermal resistance	165	°C/W

Note：

1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
2. * : Pin 1 (INV), pin 2 (COMP), pin 3 (MULT), pin 4 (CS)

Recommended Operating Conditions

Symbol	Parametar	Min.	Max.	Unit
V_{CC}	DC input supply voltage range, V_{CC} to GND	10.5	32	V
V_{INV}	INV input pin voltage range relative to GND	2.455	2.545	V
V_{MULT}	MULT input pin voltage range relative to GND	0	3	V
V_{CS}	CS input pin voltage range relative to GND	0	1.2	V
T_A	Ambient temperature range [(Note 3)]	-40	+85	°C

Note :

3. Maximum ambient temperature range is limited by allowable power dissipation.

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Electrical Characteristics

(Over recommended operating conditions unless otherwise specified. $V_{CC} = 12V$, $T_J = -25°C \sim +125°C$, $C_O = 1nF$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage						
Operating range	V_{CC}	10.5		32	V	After turn-on
Turn-on threshold	$V_{CC(ON)}$	11.7	12.5	13.3	V	
Turn-off threshold	$V_{CC(OFF)}$	8.7	9.0	9.3	V	
Hysteresis	ΔV_{CC}	3.0		4.0	V	
Zener voltage	V_Z	34		38	V	$I_{CC} = 20mA$
Supply current						
Start-up current	I_{START}		30	60	µA	Before turn-on, $V_{CC} = 11V$
Quiescent current	I_Q		2.50	3.75	mA	After turn on
Operating supply current	I_{CC}		3.5	5.0	mA	70kHz
Quiescent current	$I_{Q(OVP)}$		1.7	2.2	mA	During OVP, or $V_{INV} \leq 150mV$
Error amplifier						
Voltage feedback input threshold	V_{INV}	2.455	2.500	2.545	V	$10.5V < V_{CC} < 32V$
Line regulation	ΔV_{LINE}		2	5	mV	$V_{CC} = 10.5V \sim 32V$
Input bias current	I_{INV}			-1	µA	$V_{INV} = 0V \sim 3V$
Voltage gain	G_V	60	80		dB	Open loop
Gain-bandwidth product	GB		1		MHz	
Source current	$I_{COMP(SOURCE)}$	-2.0	-3.5	-5.0	mA	$V_{COMP} = 4V$, $V_{INV} = 2.4V$
Sink current	$I_{COMP(SINK)}$	2.4	4.5		mA	$V_{COMP} = 4V$, $V_{INV} = 2.6V$
Upper clamp voltage	$V_{COMP(UP)}$	5.3	5.7	6.0	V	$I_{SOURCE} = 0.5mA$
Lower clamp voltage	$V_{COMP(LOW)}$	2.10	2.25	2.40	V	$I_{SINK} = 0.5mA$
Disable threshold	$V_{INV(DIS)}$	150	200	250	mV	
Re-start threshold	$V_{INV(EN)}$	380	450	520	mV	
Multiplier input						
Input bias current	I_{MULT}			-1	µA	$V_{MULT} = 0V \sim 4V$
Linear operation range	V_{MULT}	0 ~ 3			V	
Output max. slope	$\Delta V_{CS} / \Delta V_{MULT}$	1.0	1.1		V/V	$V_{MULT} = 0V \sim 1V$, $V_{COMP} = $ Upper clamp
Gain [(Note 4)]	K	0.32	0.38	0.44	V	$V_{MULT} = 1V$, $V_{COMP} = 4V$
Zero current detector						
Upper clamp voltage	V_{ZCDH}	5.0	5.7	6.5	V	$I_{ZCD} = 2.5mA$
Lower clamp voltage	V_{ZCDL}	-0.3	0	0.3	V	$I_{ZCD} = -2.5mA$
Arming voltage [(Note 5)]	V_{ZCDA}		1.4		V	Positive-going edge

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Electrical Characteristics (continued)

(Over recommended operating conditions unless otherwise specified. $V_{CC} = 12V$, $T_J = -25°C \sim +125°C$, $C_O = 1nF$)

| Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Triggering voltage [Note 5]	V_{ZCDT}		0.7		V	Negative-going edge
Input bias current	I_{ZCDB}		2		µA	$V_{ZCD} = 1.0V \sim 4.5V$
Source current capability	$I_{ZCD(SOURCE)}$	-2.5			mA	
Sink current capability	$I_{ZCD(SINK)}$	2.5			mA	
Output over-voltage						
Dynamic OVP triggering current	I_{OVP}		27		µA	
Hysteresis [Note 5]	ΔI_{OVP}		20		µA	
Static OVP threshold	$V_{OVP(TH)}$	2.10	2.25	2.40	V	
Current sense comparator						
Input bias current	I_{CS}			-1	µA	$V_{CS} = 0V$
Leading edge blanking	t_{LEB}	100	200	300	ns	
Delay to output	$t_{D(H-L)}$		175		ns	
Current sense clamp	V_{CS}	1.00	1.08	1.16	V	$V_{COMP} = $ Upper clamp, $V_{MULT} = 1.5V$
Current sense offset	$V_{CS(OS\_0V)}$		25		mV	$V_{MULT} = 0V$
	$V_{CS(OS\_2.5V)}$		5			$V_{MULT} = 2.5V$
Starter						
Start timer period	t_{START}	75	190	300	µs	
GATE driver						
Output low voltage	V_{OL}		0.6	1.2	V	$I_{SINK} = 100mA$
Output high voltage	V_{OH}	9.8	10.3		V	$I_{SOURCE} = 5mA$
Peak source current	$I_{SOURCE(PK)}$	-0.6			A	
Peak sink current	$I_{SINK(PK)}$	0.8			A	
Voltage fall time	t_{FALL}		30	70	ns	
Voltage rise time	t_{RISE}		60	110	ns	
Output clamp voltage	$V_{O(CLAMP)}$	10	12	15	V	$I_{SOURCE} = 5mA$, $V_{CC} = 20V$
UVLO saturation	$V_{UVLO(SAT)}$			1.1	V	$V_{CC} = 0V \sim V_{CC(ON)}$, $I_{SINK} = 2mA$

Note：
4. The multiplier output is given by :
$$V_{CS} = K \times V_{MULT} \times (V_{COMP} - 2.5)$$
5. Parameters guaranteed by design, functionality tested in production.

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Functional Block Diagram
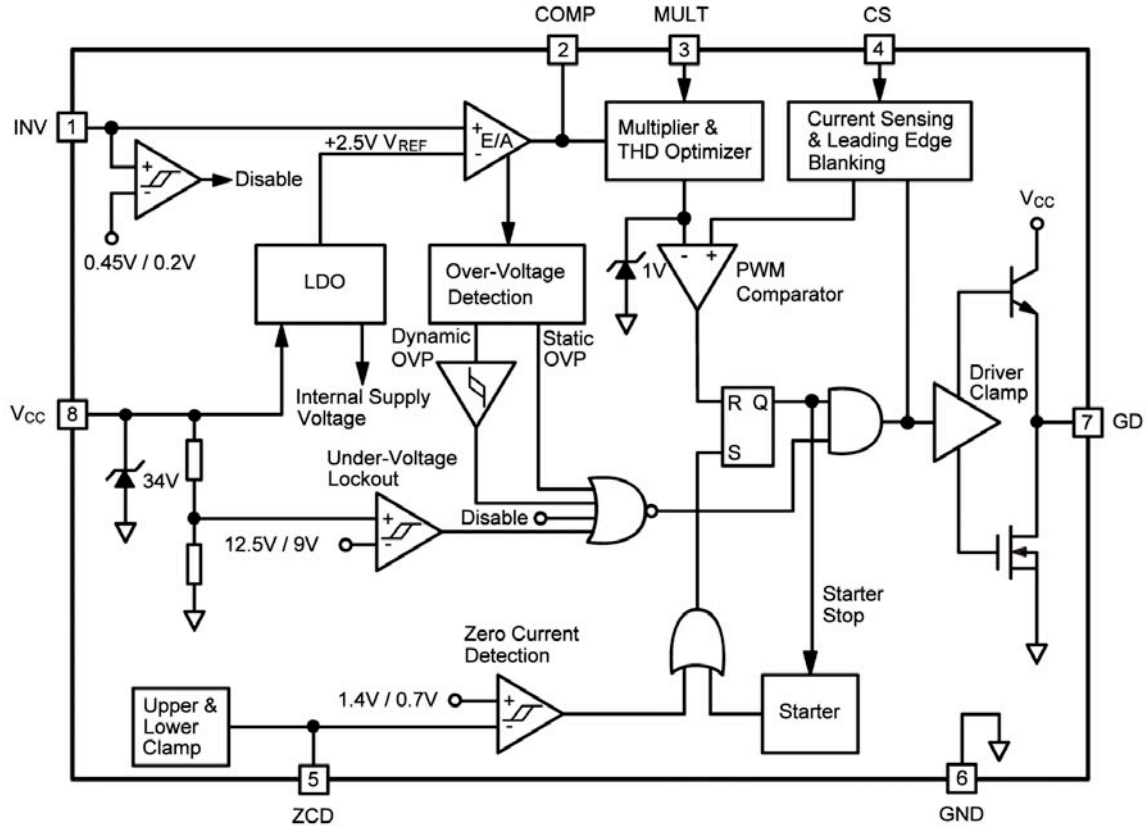
Application Information

Operation Overview

The BW6562A is an excellent transition-mode power factor correction controller for AC-DC switching mode power supply applications. It meets the IEC61000-3-2 requirement and is intended for the use in those applications that demand low power harmonics distortion. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Power Factor Correction and THD

The BW6562A features a one linear multiplier with THD optimizer for near unity power factor. To explain PFC and THD relation. First, average power is defined by

$$P_{AV} = V_{RMS} \times I_{RMS} \times \cos(\theta) \tag{1}$$

$$PF \equiv \frac{P_{AV}}{S} \tag{7}$$

$$= \frac{V_{RMS} \times i_{s1} \times \cos(\theta)}{V_{RMS} \times I_{RMS}} = \frac{V_{RMS} \cdot i_{s1} \cdot \cos(\theta)}{V_{RMS} \cdot I_{RMS}} \tag{8}$$

$$= \frac{i_{s1}}{I_{RMS}} \cos(\theta) \tag{9}$$

To consider current harmonics effect, I_{RMS} is given by

$$I_{RMS} = \sqrt{I_{S1}^2 + \sum_{N=2}^{\infty} I_{SN}^2} \tag{10}$$

where I_{SN} is RMS value of n-th input harmonics current. So, effective value of input distortion current is defined by

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where θ is phase shift between input voltage and current. Effective value of input voltage and current are defined by as follows :

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T v_s^2(t)\,dt} \qquad (2)$$

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i_s^2(t)\,dt} \qquad (3)$$

where $v_s(t)$ is instantaneous value of input voltage,

  $i_s(t)$ is instantaneous value of input current,

  T is the cycle.

Therefore, P_{AV} is written as :

$$P_{AV} = avg\,[\,v(t)\times i(t)\,] \qquad (4)$$

$$= \frac{1}{T}\int_0^T v_s(t)\ i_s(t)\,dt \frac{1}{T}\int_0^T v_s(t)\cdot i_s(t)\,dt \qquad (5)$$

And apparent power is defined by

$$S = V_{RMS}\times I_{RMS} \qquad (6)$$

where I_{RMS} is the root mean square (RMS) value of i_{RMS}. Therefore, based on the above equations, obtained power factor (PF) is defined by the ratio of average power and apparent power :

The major cause of this THD distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue, the circuit section designed in the BW6562A forces the PFC regulator to process more energy near the line voltage zero-crossings, as compared to that commanded by the control loop. This results in both, minimizing the time interval when energy transfer is lacking, and fully discharging the high-frequency filter capacitor after the bridge.

The BW6562A is designed with a special circuit that reduces the conduction dead-angle occurring to the AC

$$I_{TH} = \sqrt{I_{RMS}^2 - I_{S1}^2}\sqrt{I_{RMS}^2 - I_{s1}^2} \qquad (11)$$

$$= \sqrt{\sum_{n=2}^{\infty} I_{sn}^2} \qquad (12)$$

To quantify degree of current waveform distortion, THD is written by□

$$THD = \frac{I_{th}}{I_{s1}} \qquad (13)$$

$$= \frac{\sqrt{\sum_{N=2}^{\infty} I_{SN}^2}}{I_{S1}}\frac{\sqrt{\sum_{n=2}^{\infty} I_{sn}^2}}{I_{s1}} \qquad (14)$$

So,

$$PF = \frac{1}{\sqrt{1+THD^2}}\cos(\theta) \qquad (15)$$

If the current and voltage are in phase, then $\theta = 0$, which will lead to $\cos(\theta) = 1$, and the PF will be simplified as

$$PF = \frac{1}{\sqrt{1+THD^2}} \qquad (16)$$

Based on the equation 16, if THD is very small, then it will get near unity power factor.

is shown in Typical Application Circuit on page 1. During the start-up transient, the V_{CC} is lower than the UVLO threshold voltage ($V_{CC(ON)}$) thus there is no gate pulse produced from the BW6562A to drive power MOSFET. Therefore, the current through R6 will provide the start-up current and to charge the capacitor C2. Whenever the V_{CC} voltage is high enough to turn on the BW6562A and further to deliver the gate drive signal. Once the BW6562A is in normal operation, the supply current is switched to and provided from the auxiliary winding of the PFC choke (transformer). Lower start-up current requirement on the PFC controller will help to increase the value of R6 and then reduce the power consumption on R6. By using CMOS process and the special circuit design, the maximum start-up current of the BW6562A is only 60µA. If a higher resistance value of R6 is chosen, it usually takes more time to start-up. To carefully select the value of R6 and C2 will optimize the power consumption and start-up time.

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input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD of the current is considerably reduced. The result will be near unity power factor.

In essence, the circuit artificially increases the ON time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves towards the peak of the sinusoidal waveform.

Therefore, to maximize the benefit from the THD improvement circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, and kept just to satisfy the EMI filtering requirements.

Under-Voltage Lockout

An UVLO comparator is implemented in it to detect the voltage on the V_{CC} pin. It would assure the supply voltage enough to turn on the BW6562A PFC controller and further to drive the power MOSFET. A hysteresis is built in to prevent the shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 12.5V and 9V, respectively.

Start-up Current and Start-up Circuit

The typical start-up circuit to generate the BW6562A V_{CC}

The extra current ΔI_{R3} will flow through the compensation network and enter the error amplifier output via pin COMP. When it reaches about 37µA, the output voltage of the multiplier is forced to decrease which will reduce the energy drawn from the mains. This action behaves like braking will prevent the output voltage from exceeding the regulated value too much.

OVP and Non-Latched Disable on INV pin

To prevent the over voltage on the output capacitor from the fault condition, the BW6562A is implemented with a dynamic OVP function on INV pin. If the output voltage increases despite the braking and the current entering the INV pin is higher than the I_{OVP} threshold current 27µA, the OVP (Dynamic OVP) is triggered and the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET. This OVP condition is maintained until the INV pin current falls below 7µA to re-enable the internal starter and start switching again. The output change that is able to trigger the dynamic

Output Voltage Setting

The BW6562A monitors the output voltage signal at INV pin through a resistor divider pair R3 and R4. A trans-conductance amplifier is used instead of the conventional voltage amplifier. This trans-conductance amplifier (voltage controlled current source) also provides the additional OVP function. Neglecting ripple current, current flowing through R3, I_{R3}, will equal to current through R4, I_{R4}, As the non-inverting input of the error amplifier is biased inside the BW6562A at 2.5V, and output voltage is determined by the following relationship.

$$I_{R4} = I_{R3} = \frac{2.5}{R4} = \frac{V_O - 2.5}{R3} \qquad (17)$$

where R3 and R4 are top and bottom feedback resistor values (as shown in the Typical Application Circuit on page 1).

If any abrupt change of output voltage, $\Delta V_O > 0$, occurs due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the EA, the network connected between INV and COMP would introduces a time constant to achieve high PF. The current through R4 will remain equal to 2.5/R4 but I_{R3} will become :

$$I'_{R3} = \frac{V_O + \Delta V_O - 2.5}{R3} \qquad (18)$$

type protection. The INV pin also provides additional function as a non-latched IC disable. A voltage below 0.2V shuts down the IC and reduces its consumption below 1.7mA. To re-start the IC, the voltage on this pin must exceed 0.45V. The main usage of this function is a remote ON/OFF control input that can be driven by a PWM controller for power management purposes. However, it also offers a certain degree of additional safety since it will cause the IC to shutdown in case lower resistor of the output divider is shorted to ground or if the upper resistor is missing or fails open.

Zero Current Detection

The zero current detection block switches on the external MOSFET as the current through the boost inductor has gone to zero using an auxiliary winding coupled with the inductor. This feature allows transition-mode operation. If the voltage of the ZCD pin goes higher than 1.4V, the ZCD comparator waits until the voltage goes below 0.7V. If the voltage goes below

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OVP is calculate by

$$\Delta V_O = (27 - 7) \times R3 \tag{19}$$

An important advantage of this technique is that the over voltage level can be set independently from the regulated output voltage; the latter depends on the ratio of R3 to R4, the former on the individual value of R3. Another advantage is the precision because the tolerance of the detection current is about 12%, i.e. 12% tolerance on ΔV_O. Since ΔV_O << V_O, the tolerance on the absolute value will be proportionally reduced.

When the loading of PFC pre-regulator becomes very low, the output voltage tends to stay steadily above the nominal value, which is not the case that OVP is triggered by abrupt voltage increase. If this situation happens, the error amplifier output will saturate low, hence, when this is detected, the external power transistor is switched OFF, and the IC is put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the device will work in burst-mode, with a repetition rate that can be very low. When either OVP is activated, the quiescent consumption of the IC is reduced to minimum by the discharge of the V_{CC} capacitor and increase the hold-up capability of the IC supply.

The OVP function in the BW6562A is an auto-recovery

0.7V, the zero current detection turns on the MOSFET. The ZCD pin is protected internally by two clamps, 5.7V upper clamp and 0V lower clamp. The 190μs timer generates a MOSFET turn on signal if the driver output has been low for more than 190μs from the falling edge of the driver output.

Current Sensing and Leading Edge Blanking

The typical current mode of PFC controller feedbacks the current signals to close the control loop and achieve regulation. The BW6562A detects the primary MOSFET current from the CS pin; this is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1.08V. From above, the MOSFET peak current can be obtained from below.

$$I_{PK} = \frac{1.08}{R_{CS}} \tag{20}$$

A 200ns leading edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 200ns and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the RC filter.

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB

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layout. It is strongly recommended to adopt a smaller RC filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Multiplier

The internal multiplier takes two inputs, one from a portion of the instantaneous rectified line voltage (via pin 3 MULT) and the other from the output of the E/A (via pin 2 COMP), to feed the PWM comparator to determine the exact instant when the MOSFET is to be switched off. The output of multiplier would be rectified sinusoid as similar as instantaneous rectified line voltage different only with scaling factor determined by output of E/A. The output is then fed into PWM comparator to compare with current sense clamp voltage V_{CS} (at 1.08V), to switch MOSFET off.

The formula governing all parameters is given by multiplier output :

$$V_{CS} = K \times V_{MULT} \times (V_{COMP} - 2.5) \tag{21}$$

where K is the multiplier gain. System designer needs to calculate R1 and R2, for different input mains circumstances. Figure 1 and 2 explain multiplier characteristics and V_{CS} clamps vs. T_J respectively.

Output Drive Stage

An output stage of a push-pull buffer, with typical +800mA/-600mA driving capability is incorporated to drive a power MOSFET directly. The output voltage is clamped at 12V to protect the MOSFET gate even when the V_{CC} voltage is higher than 12V.
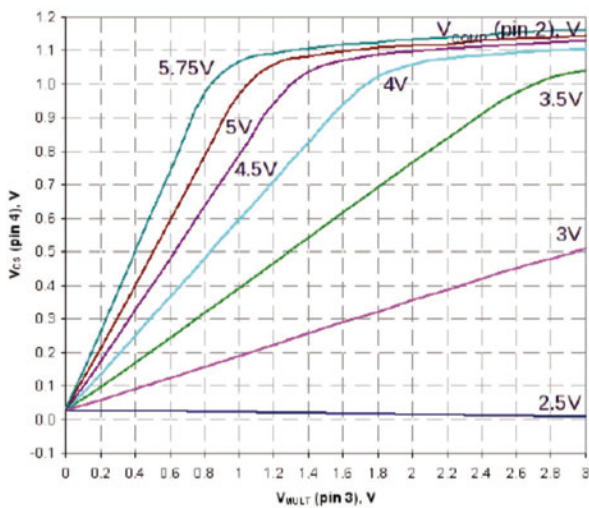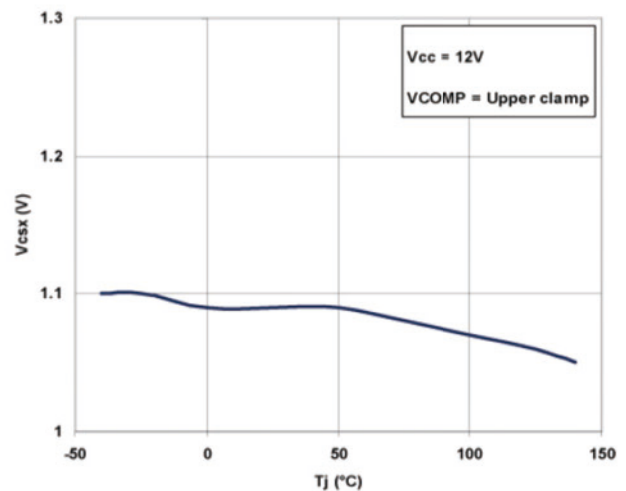
Figure 1. Multiplier Characteristics

Figure 2. V_{CS} clamps vs. T_J

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Example Applications
Single Stage LED Driver with PFC

One of major applications of the BW6562A is to provide a single stage power module with high PF for LED lighting. The following circuit, Figure 4, shows a simplified fly-back AC-DC converter with both constant current (CC) and constant voltage (CV) feedback from output side, to prevent overload and also provide an over-voltage protection facility.

This solution uses an isolated feedback with an opto-coupler and the SQ7103 (+2.5V voltage reference and dual Op-Amps), each one for voltage and current regulation respectively. As LED lighting application, the BW6562A offers the following advantages that make this solution an appropriate method against the traditionally PWM controller, where a good PF value is required :

●The input capacitance can be reduced to replace bulky and expensive high voltage electrolytic capacitor (as required by regular offline SMPS) by a small size, cheaper film capacitor

●Transition-mode ensures low turn-on losses in MOSFET and higher efficiency can be achieved.

●Lower parts count means lower material cost as well as lower assembly cost for limited space.

Few details information about this, please refer separate Application Note for details.

High PF Battery Charger

The single stage PFC can also be adopted as battery charger. Figure 5 presents an off-line universal mains battery charger that can drive up to 30W.

This solution also uses an isolated feedback with an opto-coupler and the BW7103. To use the BW6562A IC in a lead-acid battery charger circuit with high PFC, the DC output voltage and the maximum permissible DC output charging current needs to be decided on the basis of the specific battery to be charged. For the lead-acid batteries of different nominal voltages, the fixed constant-voltage, current limited, charging mode, the typical voltage level suggested by most lead-acid battery manufactures are as follows :

Nominal	Suggested Charging Voltage	Battery Discharged
6 V	6.9 V	5.25 V
12 V	13.8 V	10.50 V
24 V	27.6 V	21.00 V
48 V	55.2 V	42.00 V

The maximum lead-acid battery charging current is decided by the battery amp-hour capacity, represented as 'C'. The lead-acid battery manufacturers in general prefer a low battery charging current set at "C/20" Amp for slow-charging, for improved life of the battery. However, in case of 'fast-charging' and if permitted by the battery manufacturer, the maximum battery charging current can be set at "C/10" Amp. A charge-depleted battery will initially draw the maximum charging current. As the battery gradually gets charged, the charging current will gradually reduce.

The maximum "Current Limit" therefore helps avoid a battery getting over-heated during charging and thus avoid damage to the battery. It is advisable to avoid deep discharge of the lead-acid battery, to increase the usable battery life. The secondary side feedback network for the required CV-CC characteristics will therefore be tailored accordingly in the application circuit. The advanced battery chargers take into account the battery temperature while charging the battery and include appropriate compensation for the same, which is not in the scope of this document.

PFC Pre-Regulator

Major application of the BW6562A is to implement a wide-range mains input PFC pre-regulator, which will be acting the input stage for the cascaded isolation DC-DC converter, and can deliver above 350W in general. Typical application circuit diagram is showed on page 1. There are two methods; in general, to design pre-regulator stage, one is with fixed frequency while the other is with fixed on time.

The BW6562A can be implemented by fixed on time due to its simplicity and less expensive, while the fixed frequency technique is more complicated and beyond the scope of this application note. In fixed on time mode, the BW6562A is also working in transition mode where the inductor current will be turn on when zero crossing is detected. By using boost switching techniques, a PFC is

BW6562A High PFC LED Driver

shape the input current by drawing a quasi-sinusoidal current to be in-phase with the line voltage. A simplified circuit, shown in Figure 3, can explain the operation as follows :

Figure 3. ZCD Pin Synchronization without Auxiliary Winding
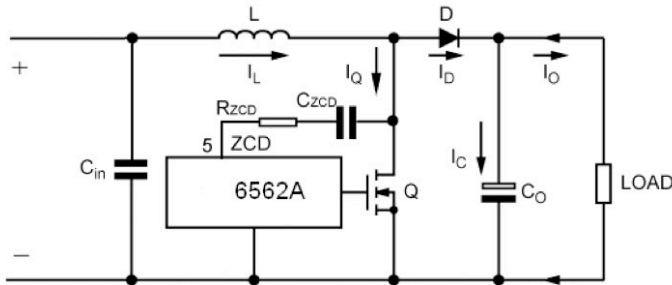
The AC mains voltage is rectified by a diode bridge and delivered to the boost converter which boosts the rectified input voltage to a higher regulated DC bus V_O.

The error amplifier compares a portion of the output voltage with an internal reference and generates a signal error proportional to the difference between them. The bandwidth of the internal error amplifier is set to be narrow within 20kHz, the output would be a DC value over a given half-cycle. Output of E/A fed into multiplier, multiplied by portion of the rectified mains voltage, will generate a scaled rectified sinusoid whose peak amplitude depends on the rectified mains peak voltage as well as the value of error signal.

The output of the multiplier is fed into the non-inverting pin of the internal PWM comparator. As the output from multiplier, a sinusoidal reference for PWM, equals to the voltage on the current sense CS pin (#4), the MOSFET will be turned off. As a consequence, the peak inductor current will be enveloped by a rectified sinusoid. After the MOSFET is turned off, the boost inductor discharges its stored energy to the load until zero current is detected and turns on MOSFET again.

In case there is no auxiliary winding on the boost inductor, a solution can be implemented by simply connecting the ZCD pin to the drain of the power MOSFET through an RC network as shown in Figure 3. In this way the high-frequency edges experienced by the drain will be transferred to the ZCD pin, hence arming and triggering the ZCD comparator.

Also in this case the resistance value must be properly chosen to limit the current sourced/sunk by the ZCD pin. In typical applications with output voltages around 400V, recommended values for these components as 22pF (or 33pF) for C_{ZCD} and 330kΩ for R_{ZCD}. With these values proper operation is ensured even with few volts difference between the regulated output voltage and the peak input voltage.

Figure 4. Single-Stage PFC, Constant Voltage and Constant Current

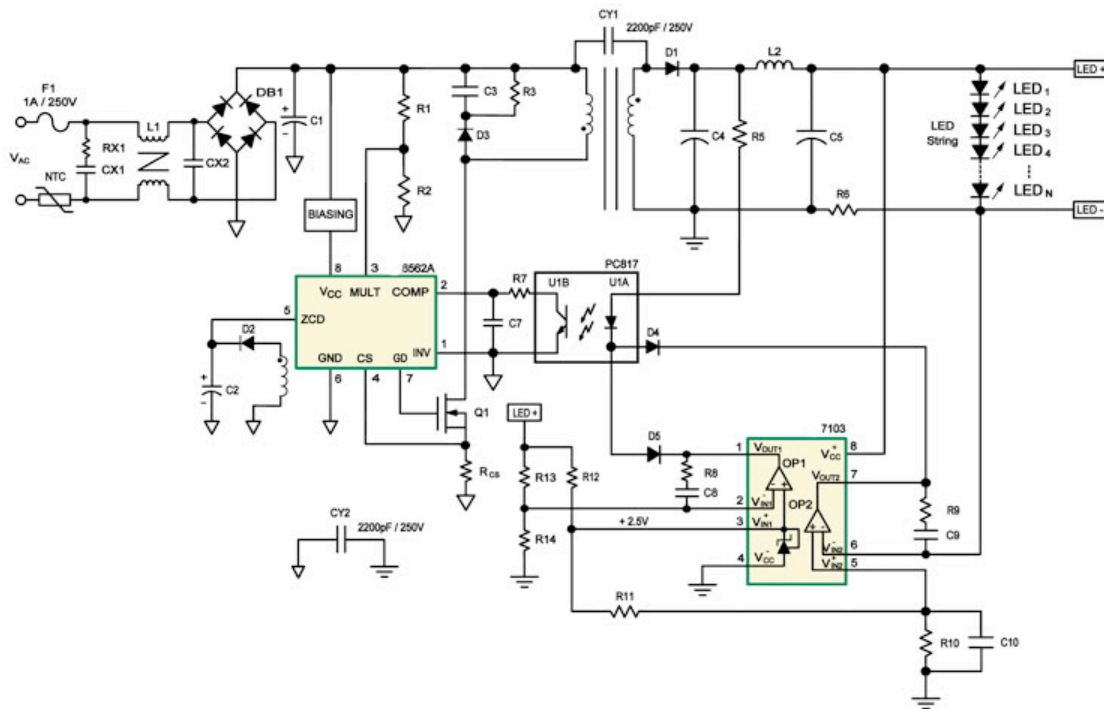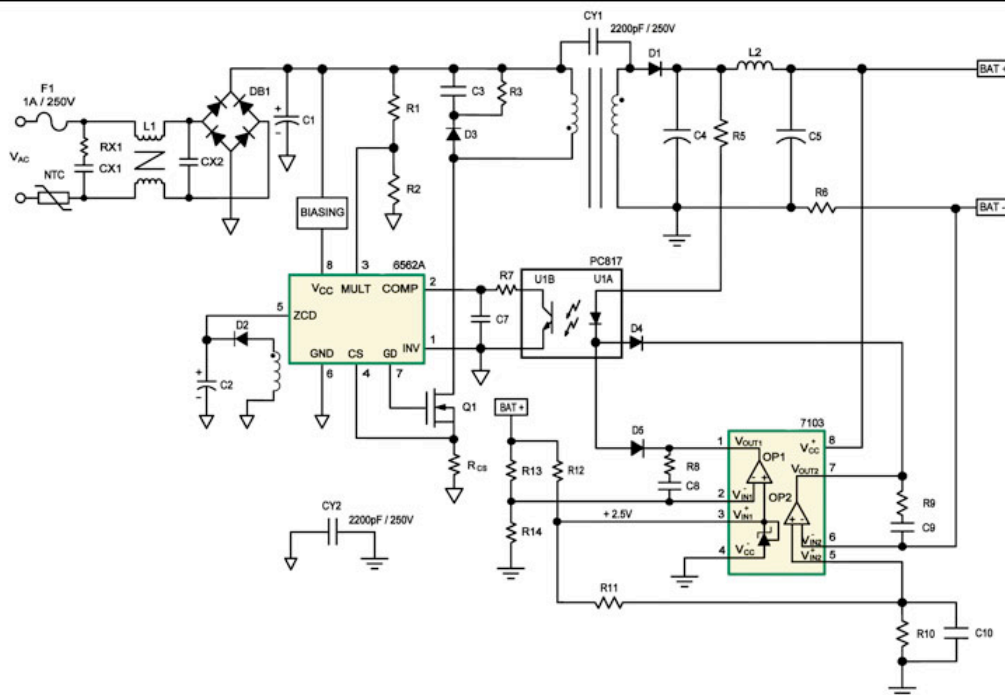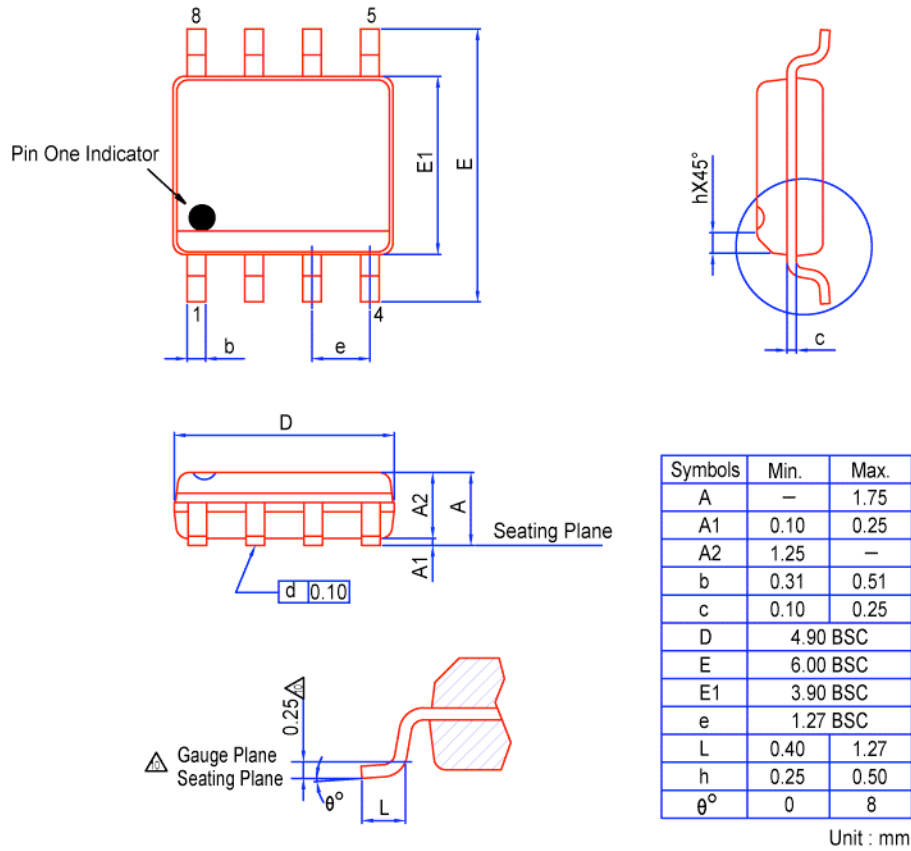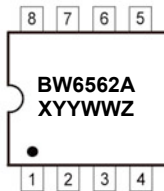**Figure 5. High Power Factor Battery Charger**

BW6562A High PFC LED Driver

Package Outline Dimensions

Package Type : SOP-8

Symbols	Min.	Max.
A	–	1.75
A1	0.10	0.25
A2	1.25	–
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

Unit : mm

Marking Information

SOP-8

BW6562A
XYYWWZ

X = A/T Site, YY = Year, WW = Working Week, Z = Device Version

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