SRAM

32K x 9 SRAM

FEATURES

- High speed: 15, 17, 20 and 25ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

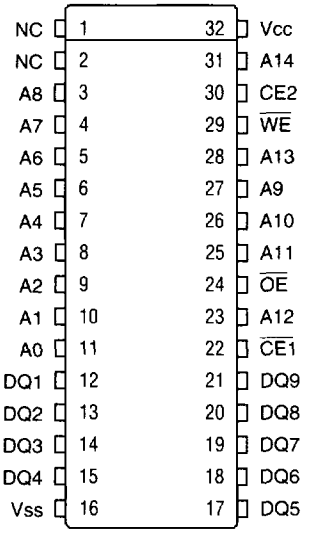
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic SOJ (300 mil) — DJ

  Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***
- 2V data retention — L
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(E-10)



GENERAL DESCRIPTION

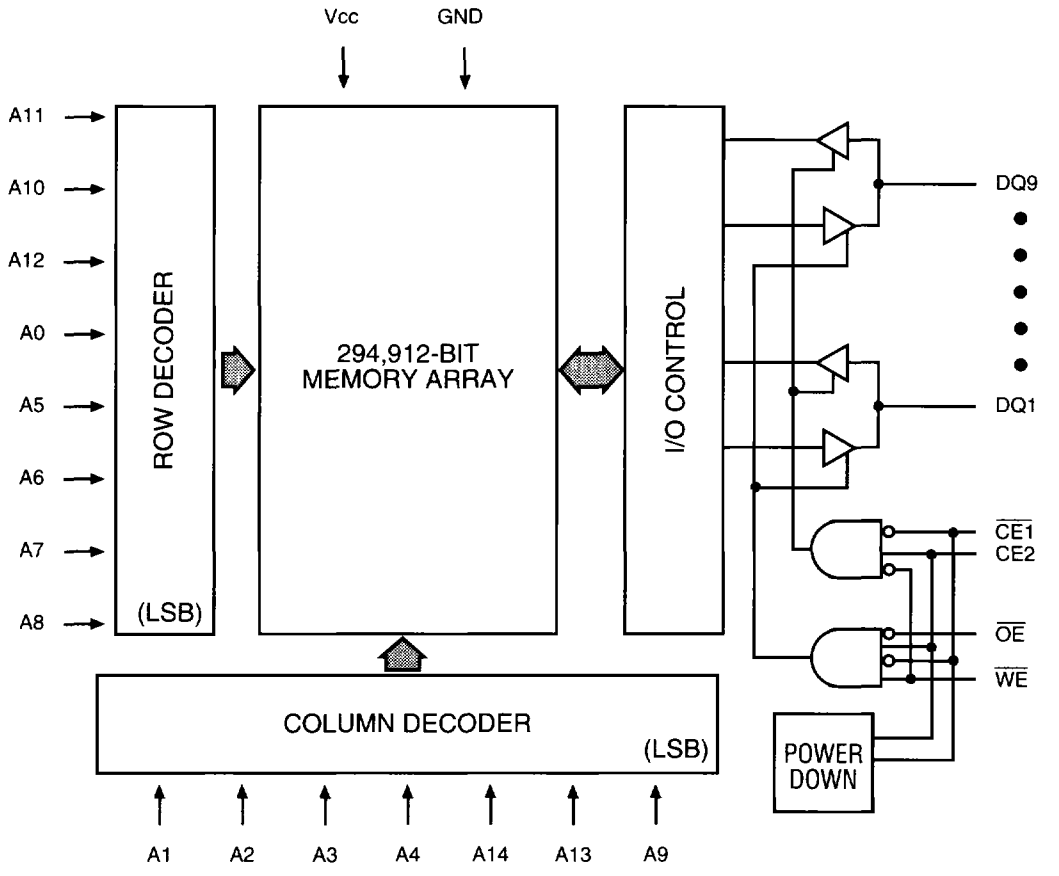
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. They are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and output enable ($\overline{OE}$) control signals. This enhancement can place the outputs in High-Z for additional flexibility in system design. The dual chip enables may be used to directly address multiple banks of SRAM without external logic.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW while CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH while $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1} \le V_{IL}$; CE2, $\ge V_{IH}$ f = MAX = $1/^tRC$ V_{CC} = MAX; Outputs Open	I_{CC}	75	145	130	120	110	mA	3, 14
Power Supply Current: Standby	$\overline{CE1} \ge V_{IH}$; CE2 $\le V_{IL}$ f = MAX = $1/^tRC$ V_{CC} = MAX; Outputs Open	I_{SB1}	11	35	35	30	30	mA	14
	$\overline{CE1} \ge V_{CC}$ - 0.2; V_{CC} = MAX CE2 and $V_{IL} \le V_{SS}$ + 0.2 $V_{IH} \ge V_{CC}$ - 0.2; f = 0	I_{SB2}	0.5	7	7	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	7	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$, V_{CC} = 5V ±10%)

DESCRIPTION		-15		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	t_{RC}	15		17		20		25		ns	
Address access time	t_{AA}		15		17		20		25	ns	
Chip Enable access time	t_{ACE}		15		17		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	4		4		4		4		ns	7
Chip disable to output in High-Z	t_{HZCE}		8		8		8		8	ns	6, 7
Chip Enable to power up time	t_{PU}	0		0		0		0		ns	
Chip disable to power down time	t_{PD}		15		17		20		25	ns	
Output Enable access time	t_{AOE}		8		8		8		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	
Output disable to out put in High-Z	t_{HZOE}		7		7		7		7	ns	6
WRITE Cycle											
WRITE cycle time	t_{WC}	15		17		20		25		ns	
Chip Enable to end of write	t_{CW}	10		13		15		20		ns	
Address valid to end of write	t_{AW}	10		13		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	10		13		15		20		ns	
WRITE pulse width	t_{WP2}	12		13		15		20		ns	
Data setup time	t_{DS}	7		8		10		10		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	4		4		4		4		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	7	0	8	0	10	0	10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

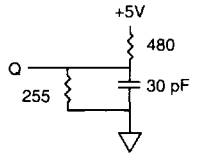


Fig. 1 OUTPUT LOAD EQUIVALENT

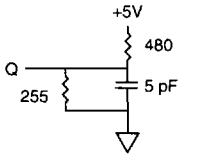


Fig. 2 OUTPUT LOAD EQUIVALENT

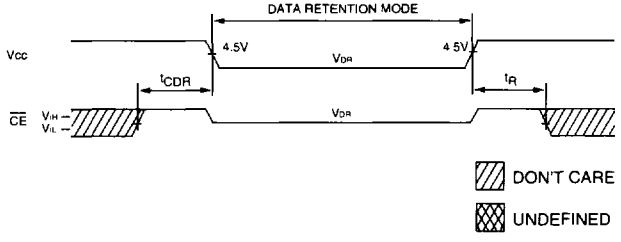
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is identical to $\overline{CE1}$ timing. The waveform is inverted.
13. Either $\overline{CE1}$, CE2 or $\overline{WE}$ can initiate or terminate WRITE cycles.
14. For automotive, industrial and extended temperature specifications, refer to page 1-175.
15. Typical values are measured at 5V, 25°C and 20ns cycle time.

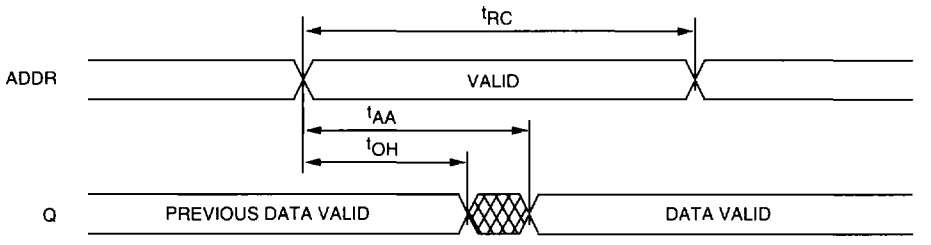
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		200	400	µA	
		Vcc = 3V			300	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

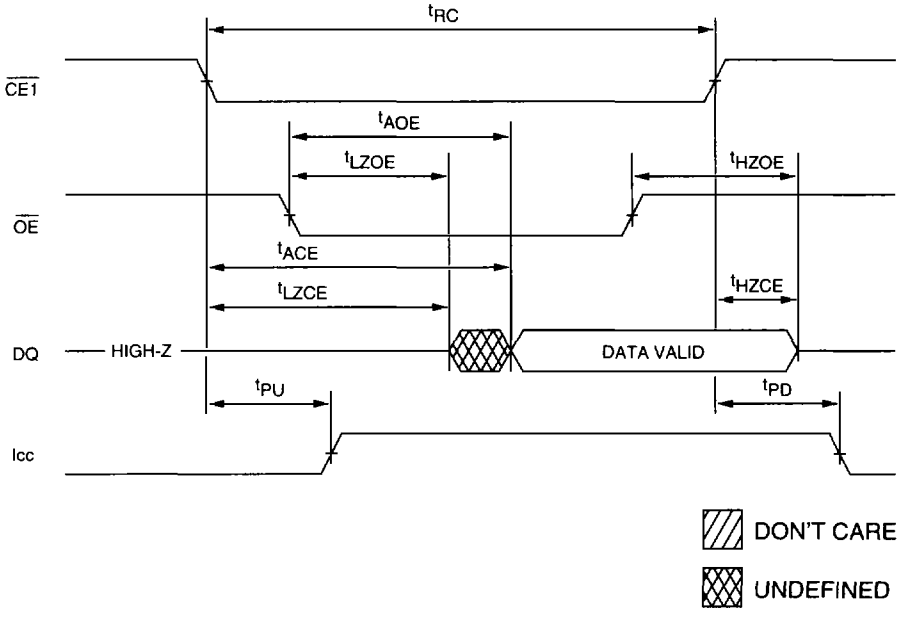
LOW Vcc DATA RETENTION WAVEFORM



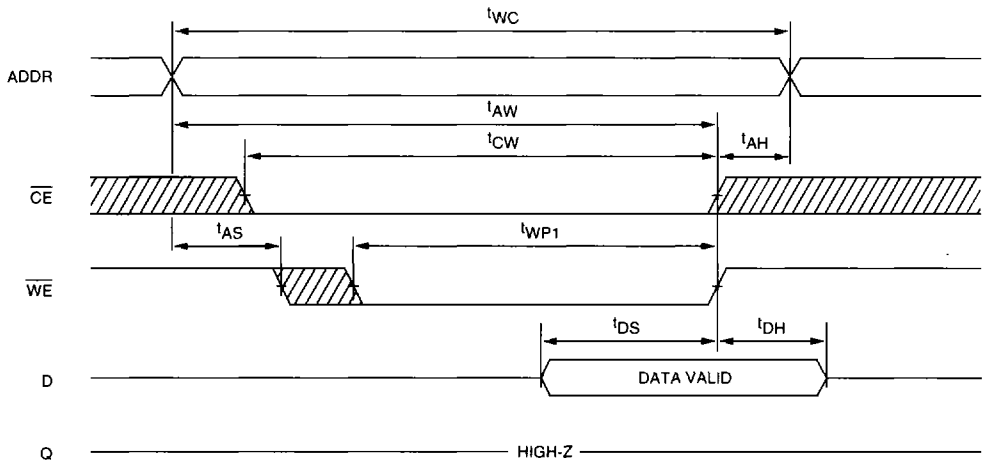
READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10, 12]

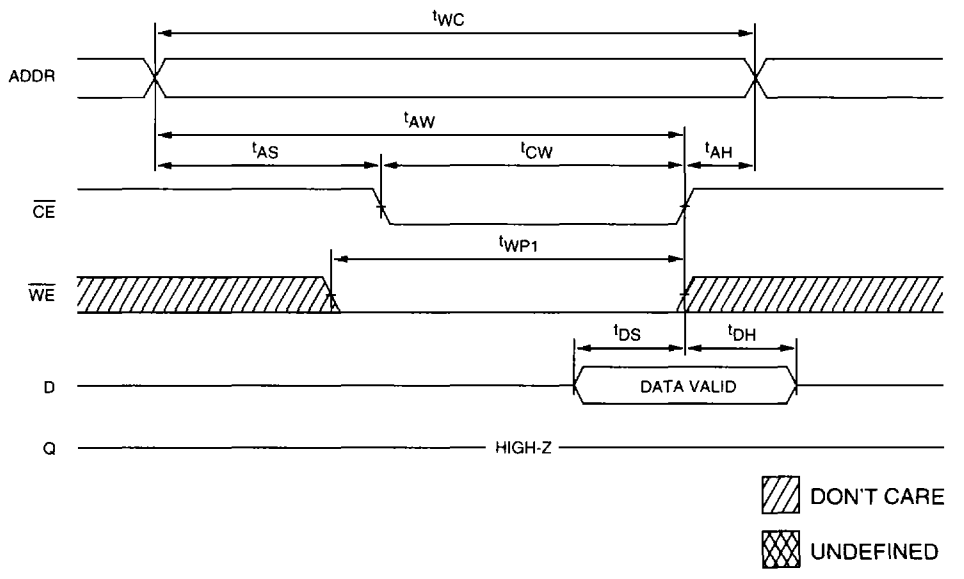


WRITE CYCLE NO. 1
(Write Enable Controlled) [12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



WRITE CYCLE NO. 3

(Write Enable Controlled) [7, 12, 13]