

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS STATIC RAM

Description

The TC55328AP/AJ is a 262,144 bit high speed CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55328AP/AJ features low power dissipation when the device is deselected using chip enable (\overline{CE}) and has an output enable input (\overline{OE}) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

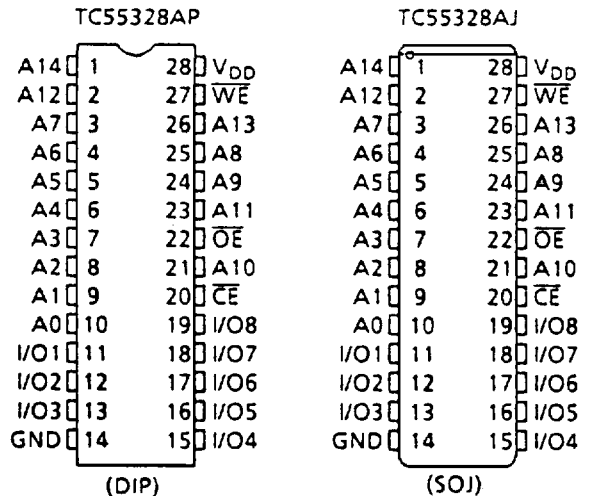
The TC55328AP/AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55328AP/AJ is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55328AP/AJ-15 15ns (max.)
 - TC55328AP/AJ-20 20ns (max.)
 - TC55328AP/AJ-25 25ns (max.)
 - TC55328AP/AJ-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC55328AP/AJ-15 140mA (max.)
 - TC55328AP/AJ-20 140mA (max.)
 - TC55328AP/AJ-25 140mA (max.)
 - TC55328AP/AJ-35 120mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55328AP: DIP28-P-300E
 - TC55328AJ: SOJ28-P-300A

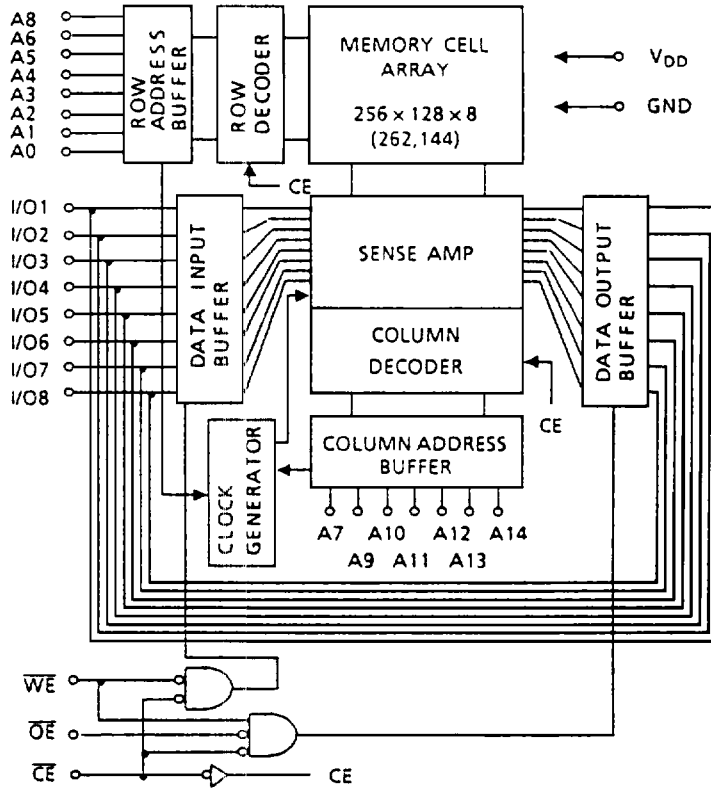
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 - I/O8	POWER
Read		L	L	H	Output	I_{DD0}
Write		L	*	L	Input	I_{DD0}
Output Disable		L	H	H	High Impedance	I_{DD0}
Standby		H	*	*	High Impedance	I_{DD5}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0 ~ 7.0	V
V_{IO}	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I_{LI}	Input Leakage Current	$V_{IN} = 0 - V_{DD}$	-	-	± 1	μA	
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = 0 - V_{DD}$	-	-	± 1	μA	
I_{OH}	Output High Voltage	$V_{OH} = 2.4\text{V}$	-4	-	-	mA	
I_{OL}	Output Low Voltage	$V_{OL} = 0.4\text{V}$	8	-	-	mA	
I_{DDO}	Operating Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-15	-	-	140	mA
			-20	-	-	140	
			-25	-	-	140	
			-35	-	-	120	
I_{DDS1}	Standby Current	$t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	-15	-	-	20	mA
			-20	-	-		
			-25	-	-		
			-35	-	-		
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	-	-	1		

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C⁽¹⁾, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55328AP/AJ-15		TC55328AP/AJ-20		TC55328AP/AJ-25		TC55328AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t _{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t _{CO}	\overline{CE} Access Time	–	15	–	20	–	25	–	35	
t _{OE}	\overline{OE} Access Time	–	8	–	10	–	12	–	15	
t _{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	
t _{COE}	Output Enable Time from \overline{CE}	5	–	5	–	5	–	5	–	
t _{COD}	Output Disable Time from \overline{CE}	–	8	–	8	–	10	–	15	
t _{OEE}	Output Enable Time from \overline{OE}	1	–	1	–	1	–	1	–	
t _{ODD}	Output Disable Time from \overline{OE}	–	8	–	8	–	10	–	15	

Write Cycle

SYMBOL	PARAMETER	TC55328AP/AJ-15		TC55328AP/AJ-20		TC55328AP/AJ-25		TC55328AP/AJ-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t _{WP}	Write Pulse Width	10	–	11	–	13	–	18	–	
t _{AW}	Address Valid to End of Write	12	–	13	–	15	–	20	–	
t _{CW}	Chip Enable to End of Write	12	–	13	–	15	–	20	–	
t _{AS}	Address Setup Time	0	–	0	–	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t _{DS}	Data Setup Time	8	–	10	–	12	–	15	–	
t _{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t _{OEW}	Output Enable Time from \overline{WE}	1	–	1	–	1	–	1	–	
t _{ODW}	Output Disable Time from \overline{WE}	–	8	–	8	–	10	–	15	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

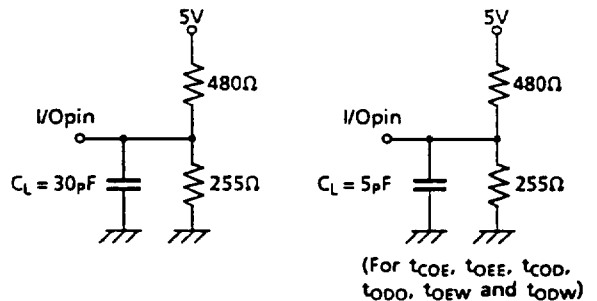
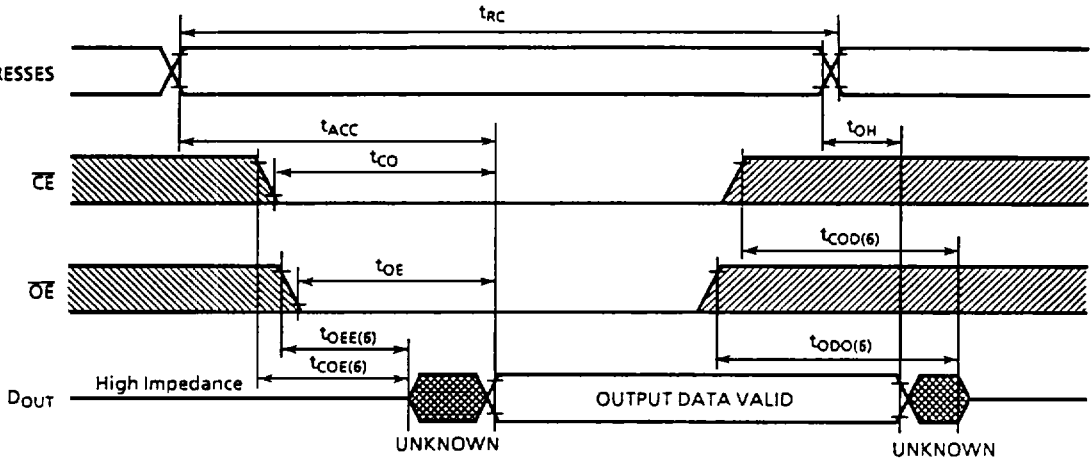


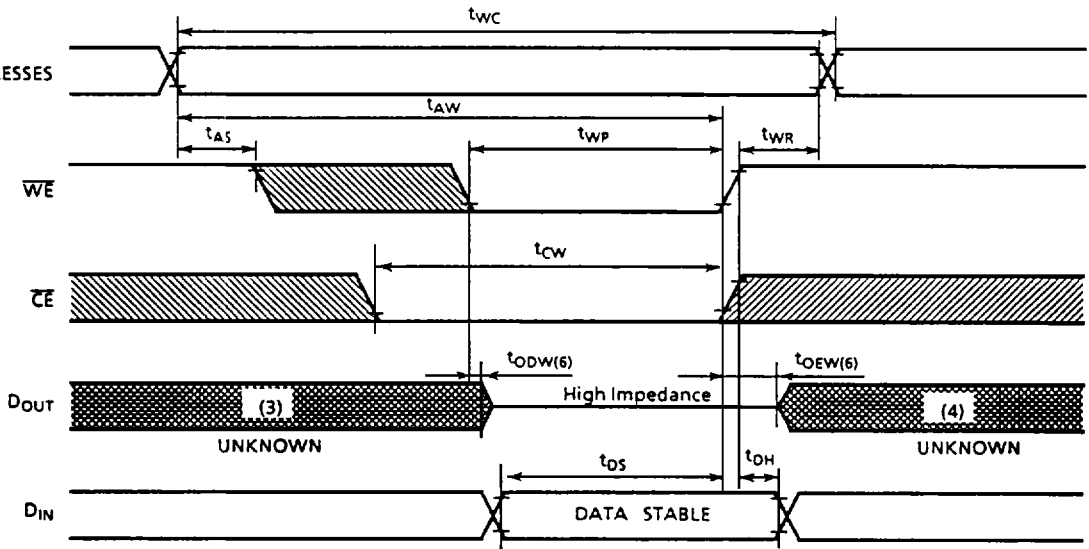
Figure 1.

Timing Waveforms

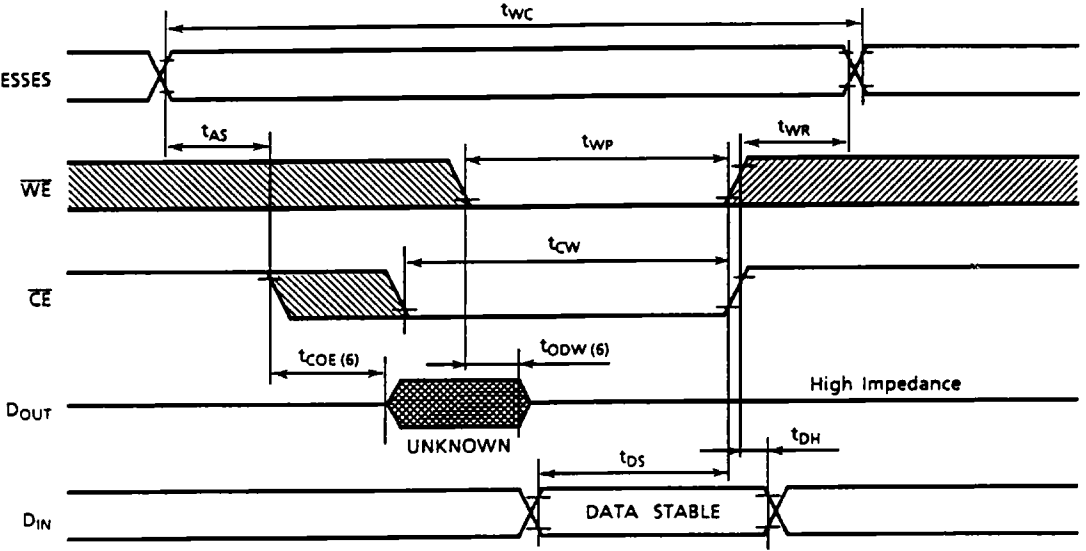
Read Cycle ⁽²⁾



Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)



Write Cycle 2⁽⁵⁾ (\overline{CE} Controlled Write)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 (B) t_{COD} , t_{OD0} , $t_{OD\overline{W}}$ Output Disable Time

