

**Document Title**

**1M x8 bit Super Low Power and Low Voltage Full CMOS Static RAM**

**Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	August 25, 1999	Preliminary

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# KM68FV8100 Family

## 1M x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 1M x8
- Power Supply Voltage: 3.0~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R, 48-FBGA-8.00x12.00

### GENERAL DESCRIPTION

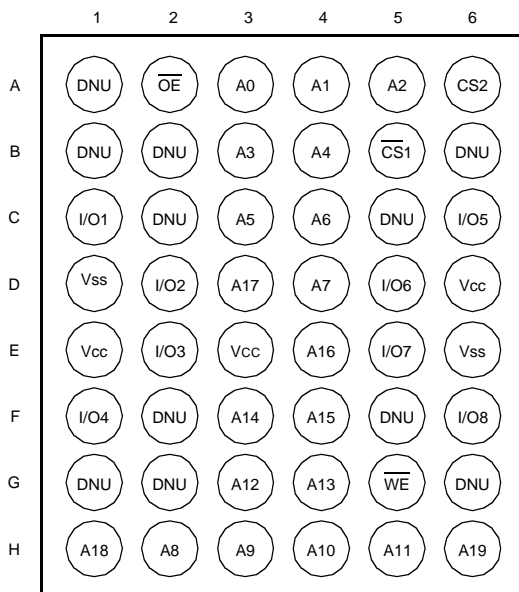
The KM68FV8100 families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

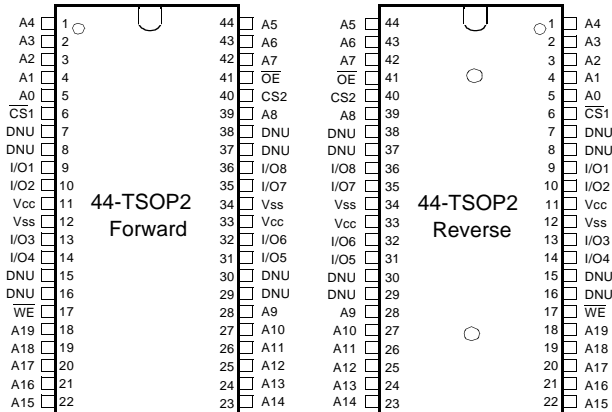
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC1</sub> , Max)	
KM68FV8100I	Industrial(-40~85°C)	3.0~3.6V	55 <sup>1)</sup> /70ns	0.5μA	3mA	44-TSOP2-400F/R 48-FBGA-8.00x12.00

1. The parameter is measured with 30pF test load.

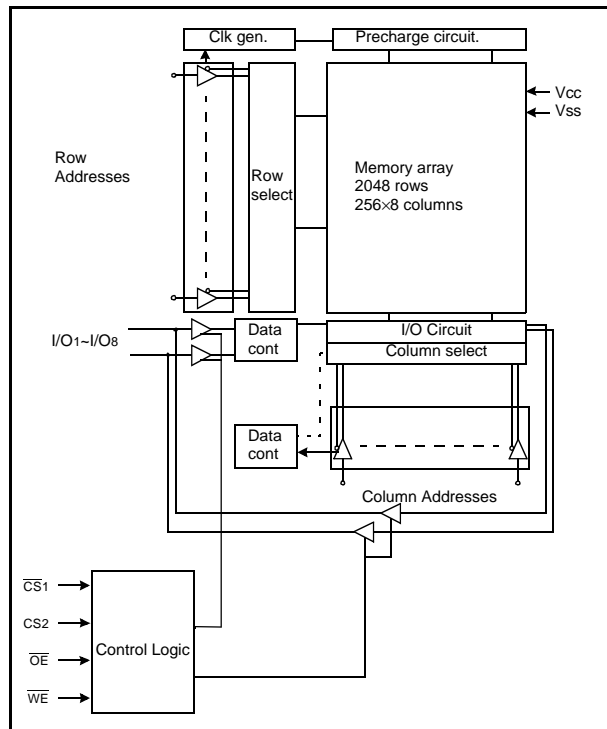
### PIN DESCRIPTION



48-FBGA: Top View (Ball Down)



### FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	A0~A19	Address Inputs
OE	Output Enable Input	Vcc	Power
WE	Write Enable Input	Vss	Ground
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

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## PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
KM68FV8100TI-5	44-TSOP2-F, 55ns, 3.3V
KM68FV8100TI-7	44-TSOP2-F, 70ns, 3.3V
KM68FV8100RI-5	44-TSOP2-R, 55ns, 3.3V
KM68FV8100RI-7	44-TSOP2-R, 70ns, 3.3V
KM68FV8100FI-5	48-FBGA, 55ns, 3.3V
KM68FV8100FI-7	48-FBGA, 70ns, 3.3V

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>1-8</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care. (Must be low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to 3.9	V
Voltage on V <sub>cc</sub> supply relative to V <sub>ss</sub>	V <sub>CC</sub>	-0.2 to 4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-55 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.6	V

Note:

1. T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

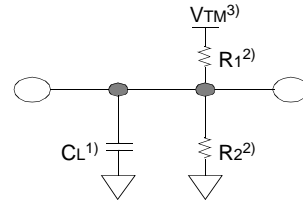
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , $\overline{WE}=V_{IH}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	2	mA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	3	mA
	I <sub>CC2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	40	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA			0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.2			V
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1 \geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V(CS <sub>1</sub> controlled) or CS <sub>2</sub> ≤0.2V(CS <sub>2</sub> controlled), Other inputs=0~V <sub>CC</sub>	-	0.5	30 <sup>1)</sup>	μA

1. Super low power product=10μA with special handling.

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load (see right):  $CL=100pF+1TTL$   
 $CL=30pF+1TTL$



1. Including scope and jig capacitance
2.  $R_1=3070\Omega$ ,  $R_2=3150\Omega$
3.  $V_{TM}=2.8V$

## AC CHARACTERISTICS ( $V_{CC}=3.0\sim 3.6V$ , $T_A=-40$ to $85^\circ C$ )

Parameter List	Symbol	Speed Bins				Units	
		55ns		70ns			
		Min	Max	Min	Max		
Read	Read cycle time	tRC	55	-	70	-	ns
	Address access time	tAA	-	55	-	70	ns
	Chip select to output	tCO1, tCO2	-	55	-	70	ns
	Output enable to valid output	tOE	-	25	-	35	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	20	0	25	ns
	$\overline{OE}$ disable to high-Z output	tOHZ	0	20	0	25	ns
Output hold from address change	tOH	10	-	10	-	ns	
Write	Write cycle time	tWC	55	-	70	-	ns
	Chip select to end of write	tcw1, tcw2	45	-	60	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	ns
	Write pulse width	tWP	40	-	50	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	ns
	Data to write time overlap	tdW	20	-	25	-	ns
	Data hold from write time	tdH	0	-	0	-	ns
End write to output low-Z	tOW	5	-	5	-	ns	

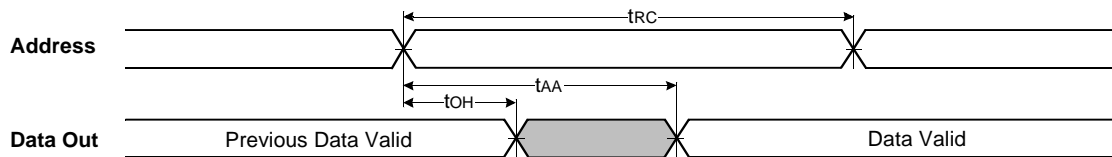
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	1.5	-	3.6	V
Data retention current	IDR	$V_{CC}=1.5V$ , $\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	-	0.5	6 <sup>(2)</sup>	$\mu A$
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ms
Recovery time	trDR		tRC	-	-	

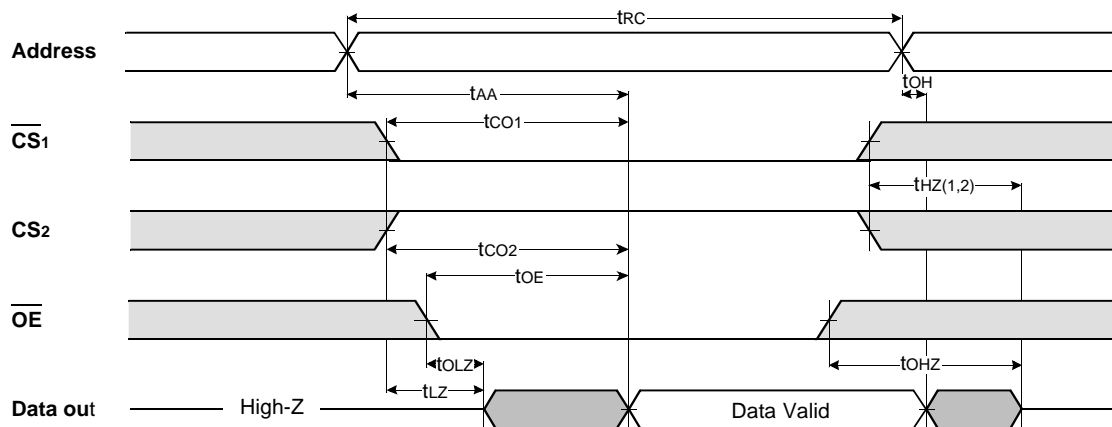
1.  $\overline{CS}_1 \geq V_{CC}-0.2V$ ,  $\overline{CS}_2 \geq V_{CC}-0.2V$  ( $\overline{CS}_1$  controlled) or  $\overline{CS}_2 \geq V_{CC}-0.2V$  ( $\overline{CS}_2$  controlled).
2. Super low power product=4 $\mu A$  with special handling.

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )



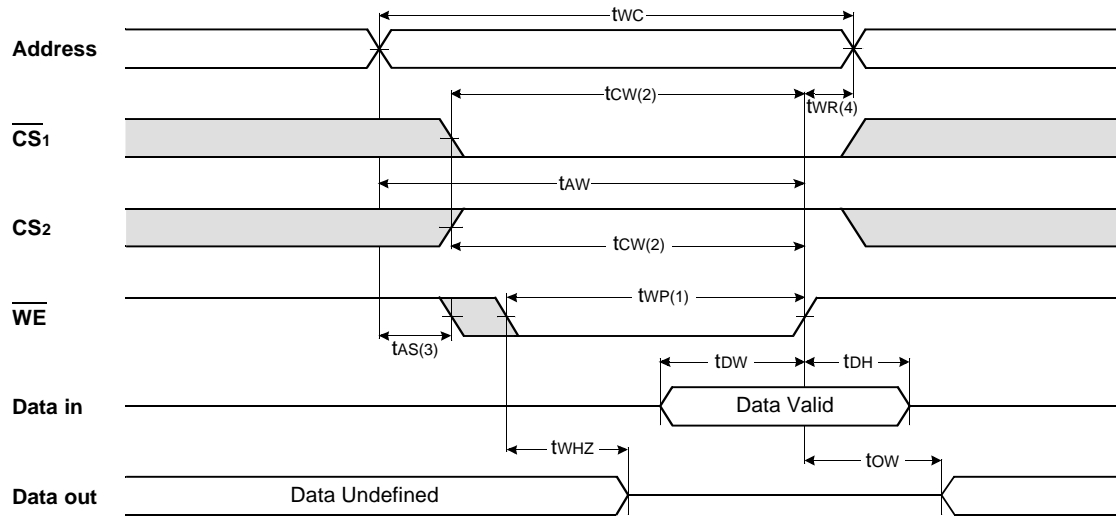
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



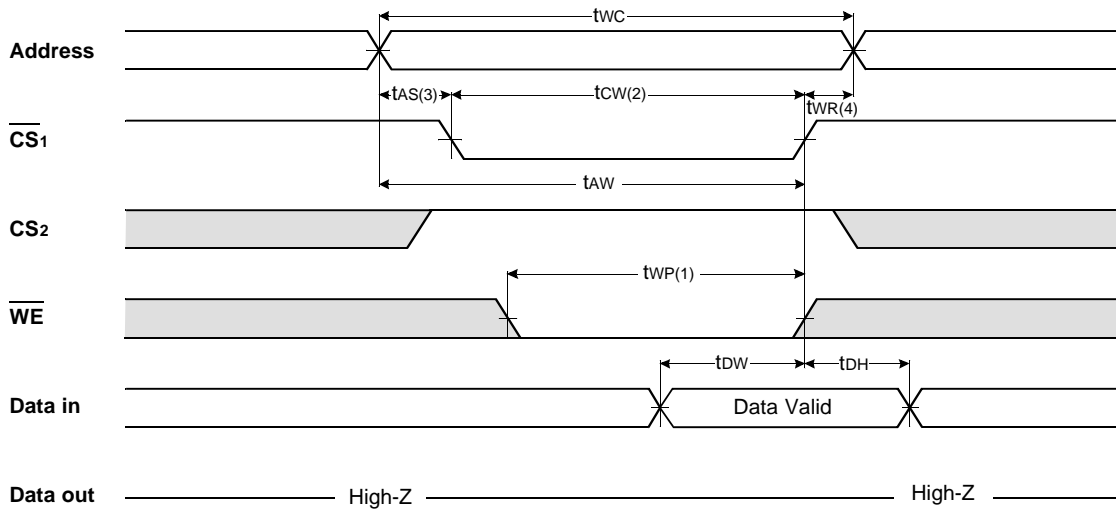
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

### TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$ Controlled)



### TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$ Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

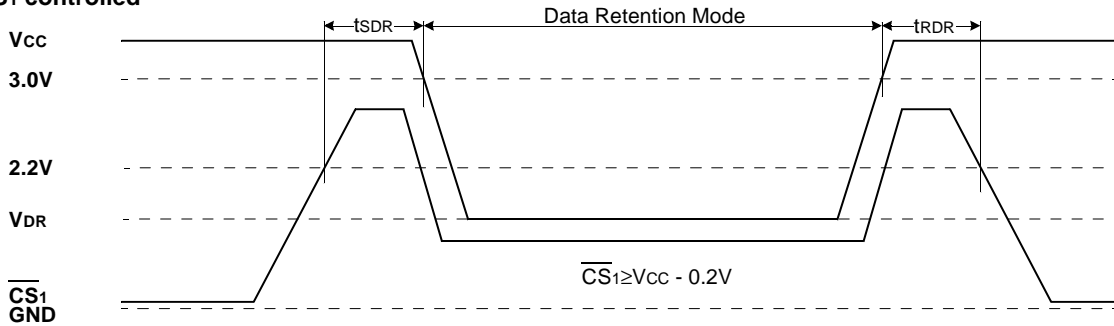


### NOTES (WRITE CYCLE)

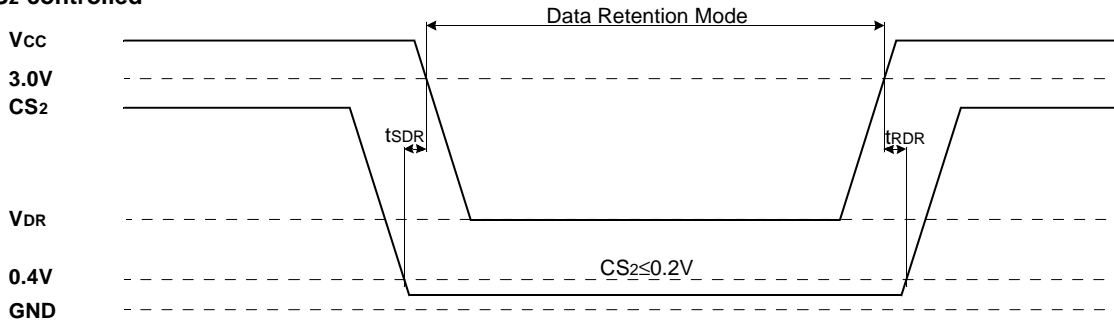
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $CS_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR2}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### CS<sub>1</sub> controlled



### CS<sub>2</sub> controlled

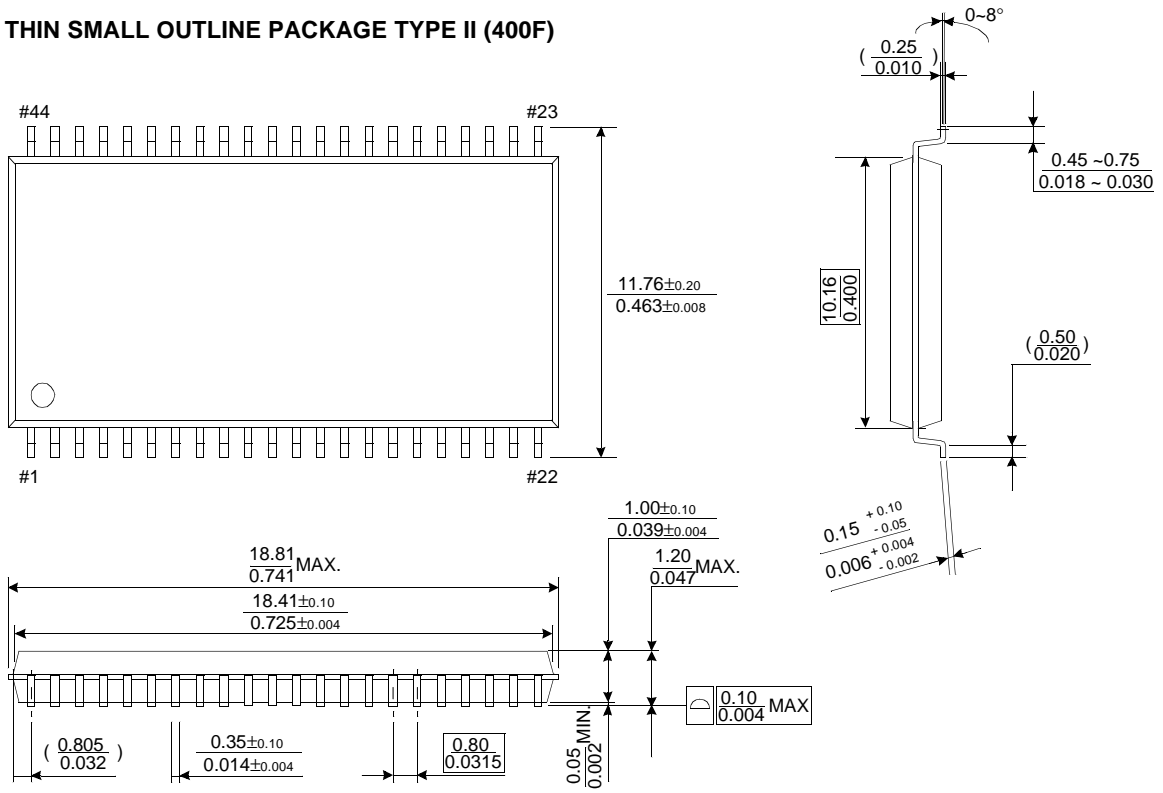




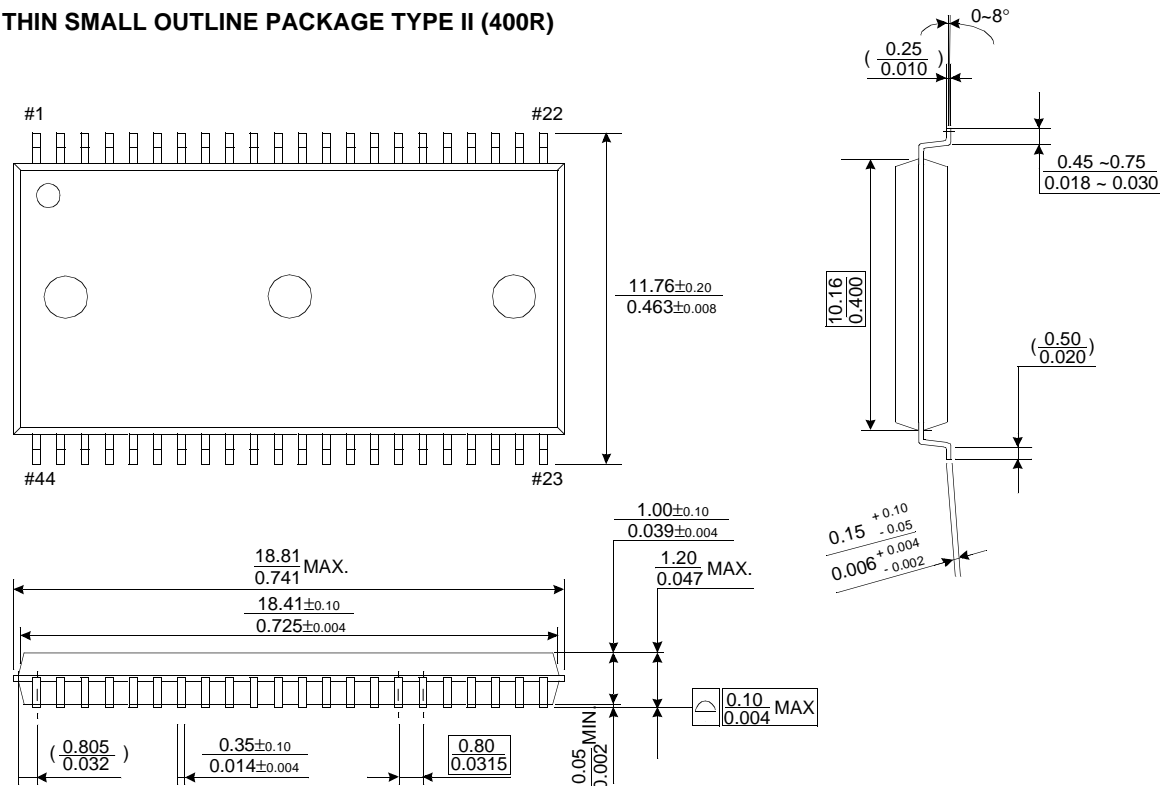
## PACKAGE DIMENSIONS

Unit: millimeter(inch)

### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



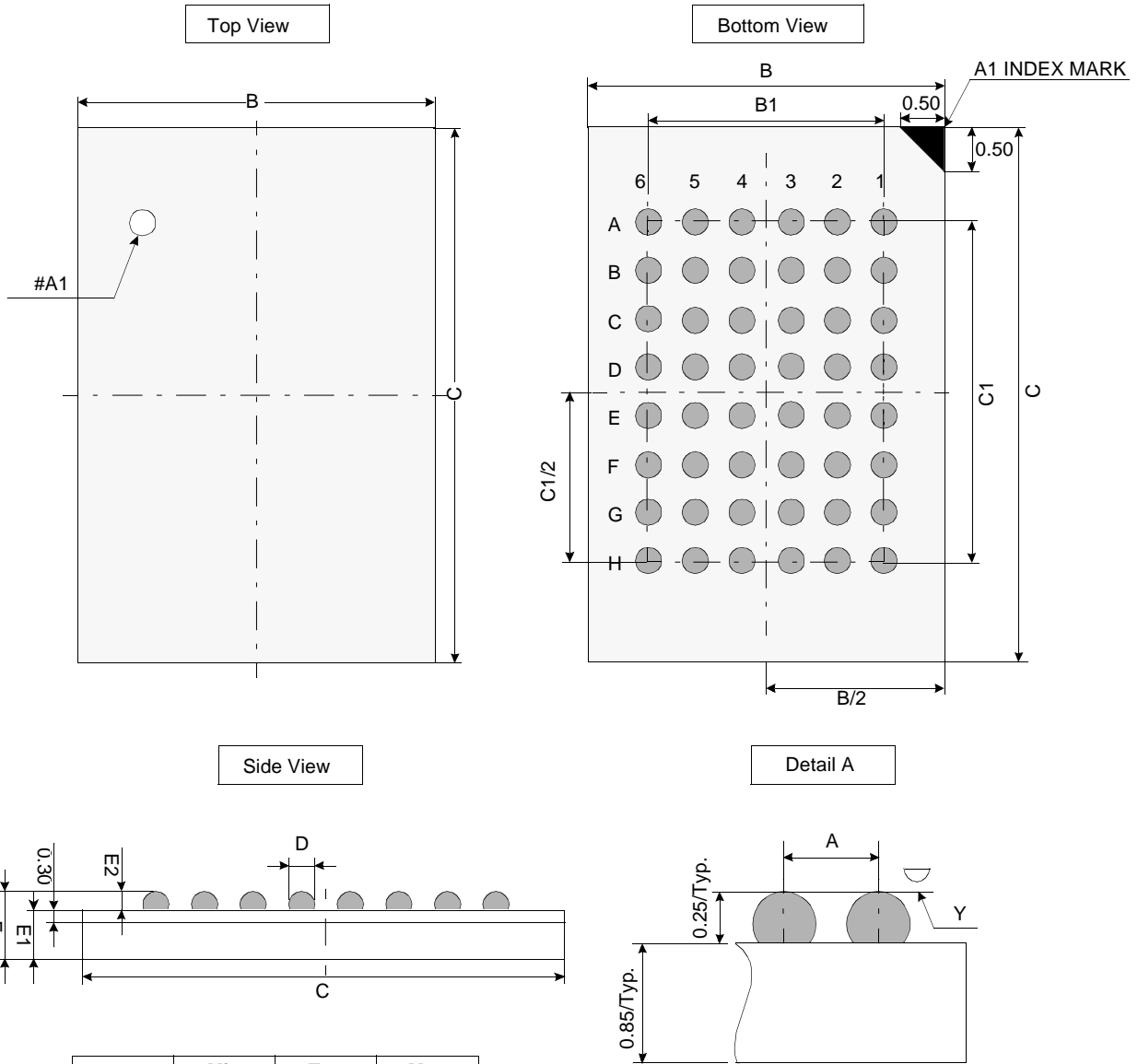
### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)



## PACKAGE DIMENSION

Unit: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	7.90	8.00	8.10
B1	-	3.75	-
C	11.90	12.00	12.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

### Notes.

1. Bump counts: 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)