

MN4516B/MN4516BS



4-Bit Binay Up/Down Counter

■ Outline


The MN4516B/S is a synchronous 4-bit binary up/down counter. When the level of the set input was set to "L" and the level of the load input was set to "H", the input data of $P_0 \sim P_3$ is preset in the counter.

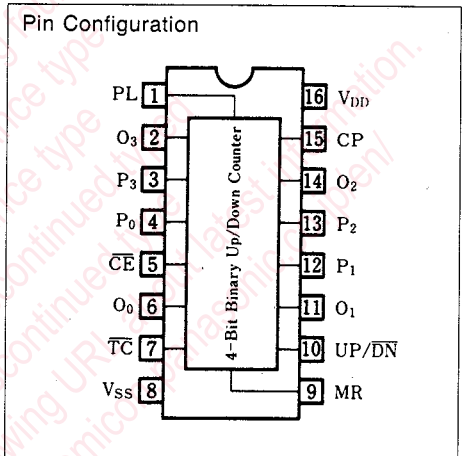
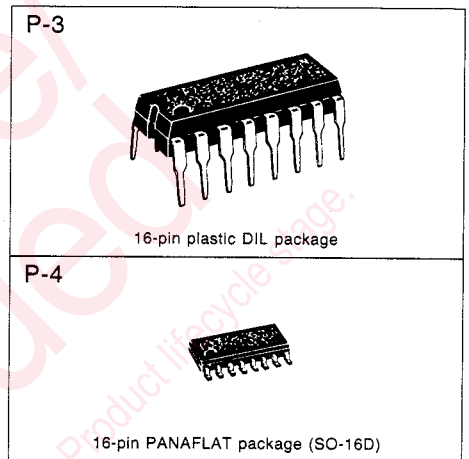
The MN4516B/S is equivalent to Motorola's MC14093B and RCA's DC4516B.

■ Truth Table

MR	PL	UP/DN	\overline{CE}	CP	Operation Mode
L	H	×	×	×	Parallel Load
L	L	×	H	×	No Change
L	L	L	L		Count Down
L	L	H	L		Count Up
H	×	×	×	×	Reset

Pin description

- CP : Clock input ()
- UP/DN : Up/down input
- PL : Load input
- \overline{CE} : Enable input (carry input)
- MR : Reset input
- $P_0 \sim P_3$: Data input (4 bits)
- $O_0 \sim O_3$: Counter output (4 bits)
- TC : Carry output



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.5~+18	V
Input voltage	V _I	-0.5~V _{DD} +0.5*	V
Output pin voltage	V _O	-0.5~V _{DD} +0.5*	V
Peak input · output pin current	±I _I	max. 10	mA
Power dissipation (per package)	Ta=-40~+60°C	P _D	max. 400 Decrease to 200mW at the rate of 8mW/°C
	Ta=+60~+80°C		
Power dissipation (per output pin)	P _D	max. 100	mW
Operating ambient temperature	T _{opr}	-40~+85	°C
Storage temperature	T _{stg}	-65~+150	°C

* V_{DD}+0.5V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V _{DD} (V)	Symbol	Condition	Ta=-40°C		Ta=25°C		Ta=85°C		Unit
				min.	max.	min.	max.	min.	max.	
Static supply current	5	I _{DD}	V _I =V _{SS} or V _{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output voltage low level	5	V _{OL}	V _I =V _{SS} or V _{DD} I _O <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V _{OH}	V _I =V _{SS} or V _{DD} I _O <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V _{IL}	I _O <1μA	V _O =0.5V or 4.5V	—	1.5	—	1.5	—	V
	10			V _O =1V or 9V	—	3	—	3	—	
	15			V _O =1.5V or 13.5V	—	4	—	4	—	
Input voltage high level	5	V _{IH}	I _O <1μA	V _O =0.5V or 4.5V	3.5	—	3.5	—	3.5	V
	10			V _O =1V or 9V	7	—	7	—	7	
	15			V _O =1.5V or 13.5V	11	—	11	—	11	
Output current low level	5	I _{OL}	V _O =0.4V, V _I =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V _O =0.5V, V _I =0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V _O =1.5V, V _I =0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	-I _{OH}	V _O =4.6V, V _I =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V _O =9.5V, V _I =0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V _O =13.5V, V _I =0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	-I _{OH}	V _O =2.5V, V _I =0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	±I _I	V _I =0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

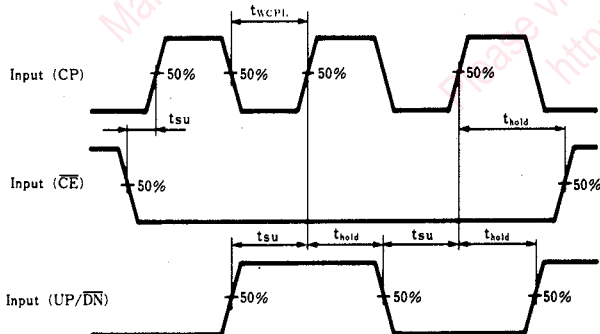
Item	V _{DD} (V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t _{PLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t _{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP→On (H→L)	5	t _{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation time CP→On (L→H)	5	t _{PLH}	—	155	465	ns
	10		—	65	195	
	15		—	45	135	
Propagation time CP→ \overline{TC} (H→L)	5	t _{PHL}	—	260	780	ns
	10		—	105	315	
	15		—	75	225	
Propagation time CP→TC (L→H)	5	t _{PLH}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation time PL→On (H→L)	5	t _{PHL}	—	125	375	ns
	10		—	55	165	
	15		—	40	120	
Propagation time PL→On (L→H)	5	t _{PLH}	—	170	510	ns
	10		—	70	210	
	15		—	50	150	
Propagation time PL→ \overline{TC} (H→L)	5	t _{PHL}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation time PL→ \overline{TC} (L→H)	5	t _{PLH}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation time \overline{CE} → \overline{TC} (H→L)	5	t _{PHL}	—	165	495	ns
	10		—	65	195	
	15		—	50	150	
Propagation time \overline{CE} →TC (L→H)	5	t _{PLH}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation time MR→On, \overline{TC} (H→L)	5	t _{PHL}	—	205	615	ns
	10		—	65	195	
	15		—	45	135	
Propagation time MR→ \overline{TC} (L→H)	5	t _{PLH}	—	225	675	ns
	10		—	75	225	
	15		—	50	150	
Minimum clock pulse width (Fig. 1)	5	t _{wCPL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	

■ Switching Characteristics (cont.)

Item	V _{DD} (V)	Symbol	min.	typ.	max.	Unit
Minimum PL pulse width (H) (Fig. 2)	5	t _{WPLH}	—	55	165	ns
	10		—	25	75	
	15		—	15	45	
Minimum reset pulse width (H) (Fig. 2)	5	t _{WMRH}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Reset recovery time (Fig. 2)	5	t _{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
PL recovery time (Fig. 2)	5	t _{RP}	—	75	225	ns
	10		—	25	75	
	15		—	15	45	
Set-up time (Fig. 2) P _n →PL	5	t _{su}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Set-up time (Fig. 1) UP/ \overline{DN} →CP	5	t _{su}	—	125	375	ns
	10		—	50	150	
	15		—	35	105	
Set-up time (Fig. 1) \overline{CE} →CP	5	t _{su}	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Hold time (Fig. 2) P _n →PL	5	t _{hold}	—	-40	10	ns
	10		—	-20	5	
	15		—	-20	0	
Hold time (Fig. 1) UP/ \overline{DN} →CP	5	t _{hold}	—	-90	35	ns
	10		—	-35	15	
	15		—	-25	15	
Hold time (Fig. 1) \overline{CE} →CP	5	t _{hold}	—	-40	20	ns
	10		—	-15	5	
	15		—	-10	5	
Maximum clock frequency	5	f _{max}	5	10	—	MHz
	10		12	24	—	
	15		17	34	—	
Input capacitance		C _i	—	—	7.5	pF

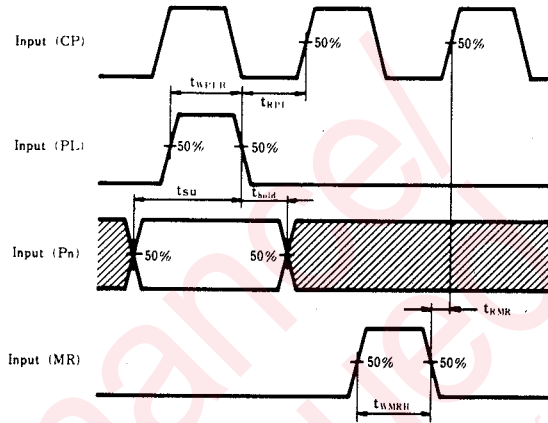
● Switching waveforms

Fig. 1 t_{WPLH}, t_{su} (UP/ \overline{DN} →CP· \overline{CE} →CP), t_{hold} (UP/ \overline{DN} →CP· \overline{CE} →CP)



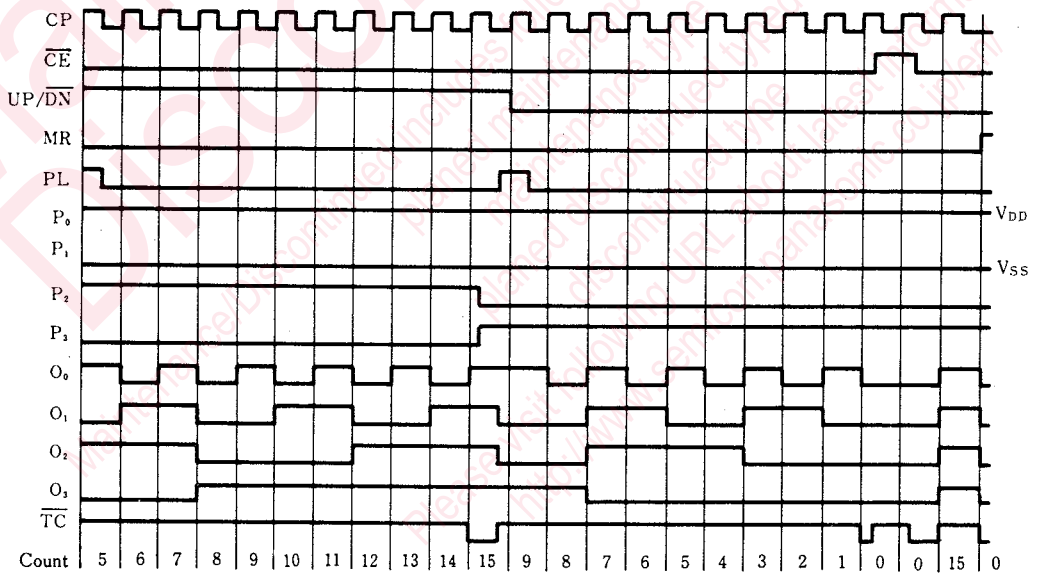
Waveforms showing minimum pulse width for CP, set-up and hold times for CE to CP and UP/ \overline{DN} to CP.

Fig. 2 t_{WPLH} , t_{RPL} , t_{RMR} , t_{WMRH} , t_{su} ($P_n \rightarrow PL$), t_{hold} ($P_n \rightarrow PL$)

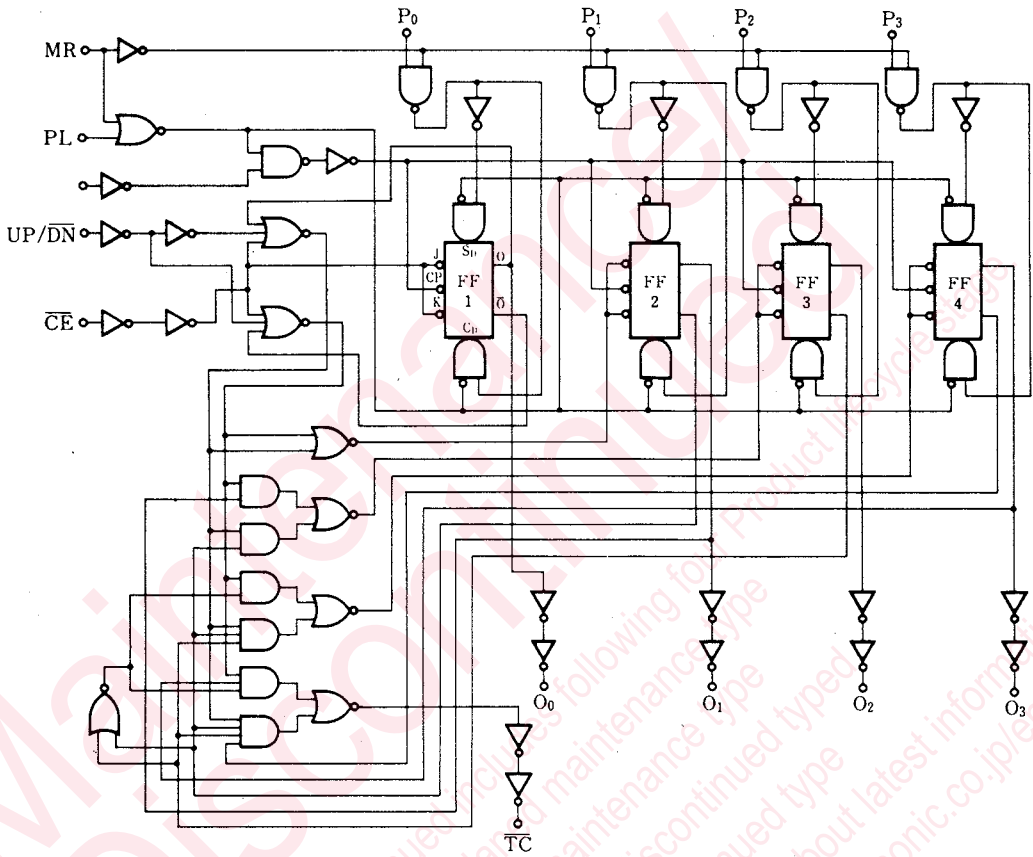


Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and, set-up and hold times for P_n to PL.

■ Timing Diagram



■ Logic Diagram



Maintenance/Discontinued type
 planned maintenance type
 planned discontinued type
 discontinued type
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