July 2013

# FAN54040 — FAN54047
# USB-OTG, 1.55 A, Li-Ion Switching Charger with Power Path and 2.3 A Production Test Support

## Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Power Path Circuit Ensures Fast System Startup with a Dead Battery when VBUS is Connected
- 1.55 A Maximum Charge Current
- Float Voltage Accuracy:
  - ±0.5% at 25°C
  - ±1% from 0 to 125°C
- ±5% Input and Charge Current Regulation Accuracy
- Temperature-Sense Input Prevents Auto-Charging for JEITA Compliance
- Thermal Regulation and Shutdown
- 4.2 V at 2.3 A Production Test Mode
- 5 V, 500 mA Boost Mode for USB OTG
- 28 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- Programmable through High-Speed $I^2C$ Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Float Voltage
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1 μH External Inductor
- Safety Timer with Reset Control
- Dynamic Input Voltage Control
- Very Low Battery Current when Charger Inactive

## Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

## Description

The FAN5404X family includes $I^2C$ controlled 1.55 A USB-compliant switch-mode chargers with power path operation and USB OTG boost operation. Integrated with the charger, the IC supports production test mode, which provides 4.2 V at up to 2.3 A to the system.

To facilitate fast system startup, the IC includes a power path circuit, which disconnects the battery from the system rail, ensuring that the system can power up quickly following a VBUS connection. The power path circuit ensures that the system rail stays up when the charger is plugged in, even if the battery is dead or shorted.

The charging parameters and operating modes are programmable through an $I^2C$ Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN5404X provides battery charging in three phases: conditioning, constant current, and constant voltage. The integrated circuit automatically restarts the charge cycle when the battery falls below a voltage threshold. If the input source is removed, the IC enters a high-impedance mode blocking battery current from leaking to the input. Charge status is reported back to the host through the $I^2C$ port.

Dynamic input voltage control prevents a weak adapter's voltage from collapsing, ensuring charging capability from such adapters.

The FAN5404X is available in a 25-bump, 0.4 mm pitch, WLCSP package.

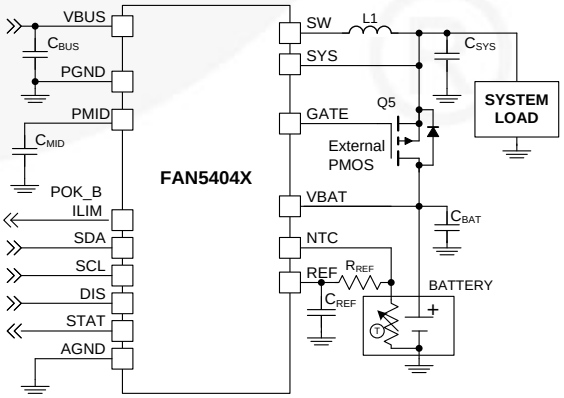



**Figure 1. Typical Application**

## Ordering Information

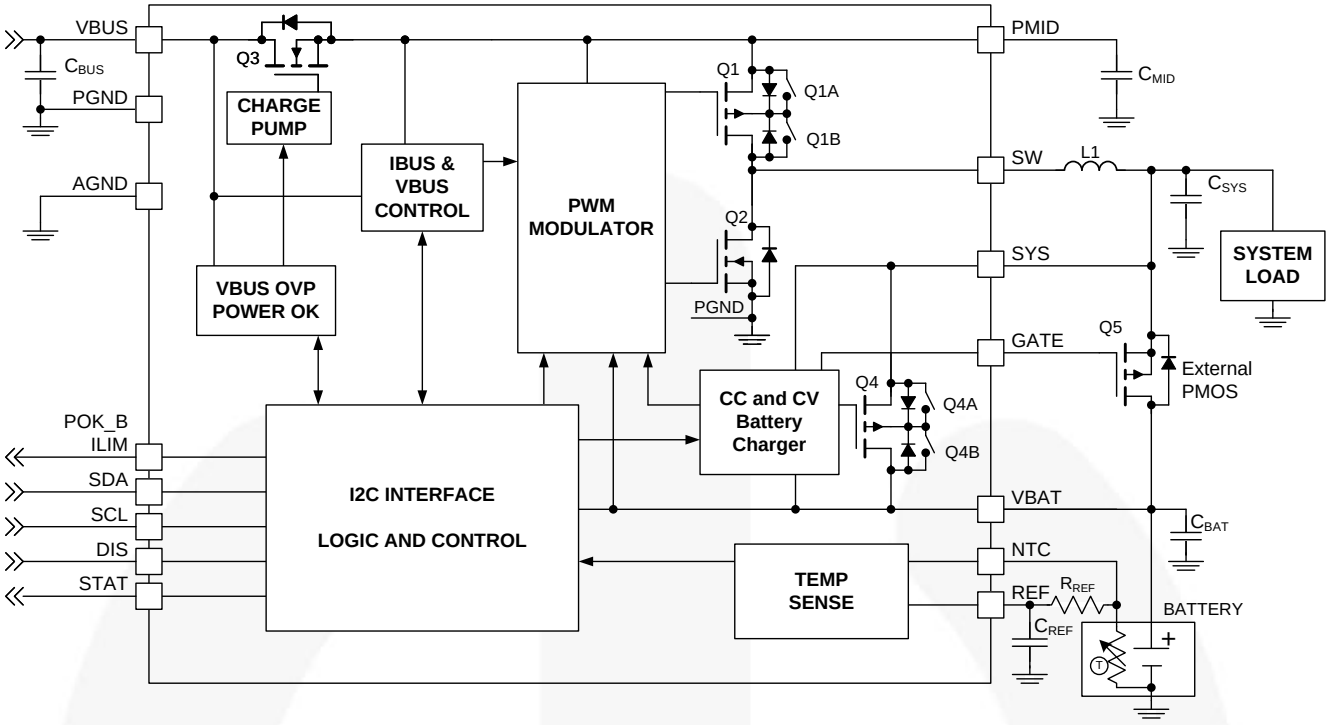
| Part Number | Temperature Range | Package | PN Bits: IC_INFO[5:3] | Packing Method |
|---|---|---|---|---|
| FAN54040UCX | -40 to 85°C | 25-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch | 000 | Tape and Reel |
| FAN54041UCX | | | 001 | |
| FAN54042UCX(1) | | | 010 | |
| FAN54045UCX(1) | | | 101 | |
| FAN54046UCX(1) | | | 110 | |
| FAN54047UCX | | | 110 | |

**Note:**
1. Contact Fairchild Sales for availability.

**Table 1. Feature Comparison Summary**

| Part Number | Slave Address | Automatic Charge | Battery Absent Behavior | E1 Pin |
|---|---|---|---|---|
| FAN54040 | 1101011 | Yes | Off | POK_B |
| FAN54041 | 1101011 | No | Off | POK_B |
| FAN54042 | 1101011 | Yes | On | POK_B |
| FAN54045 | 1101011 | No | Off | ILIM |
| FAN54046 | 1101011 | No | On | ILIM |
| FAN54047 | 1101011 | Yes | On | ILIM |

## Block Diagram




| PMID | Q1A | Q1B |
|---|---|---|
| Greater than $V_{BAT}$ | ON | OFF |
| Less than $V_{BAT}$ | OFF | ON |

| SYS | Q4A | Q4B |
|---|---|---|
| Greater than $V_{BAT}$ | ON | OFF |
| Less than $V_{BAT}$ | OFF | ON |

**Figure 2. IC and System Block Diagram**

**Table 2. Recommended External Components**

| Component | Description | Vendor | Parameter | Typ. | Unit |
|---|---|---|---|---|---|
| L1 | 1 µH, 20%, 2.2 A, 2016 | Taiyo Yuden MAKK2016T1R0M or Equivalent | L | 1.0 | µH |
| | | | DCR (Series R) | 75 | mΩ |
| $C_{BAT}$, $C_{SYS}$ | 10 µF, 20%, 6.3 V, X5R, 0603 | Murata: GRM188R60J106M TDK: C1608X5R0J106M | C | 10 | µF |
| $C_{MID}$ | 4.7 µF, 10%, 6.3 V, X5R, 0603 | Murata: GRM188R60J475K TDK: C1608X5R0J475K | C(2) | 4.7 | µF |
| $C_{BUS}$, | 1.0 µF, 10%, 25 V, X5R, 0603 | Murata GRM188R61E105K TDK:C1608X5R1E105M | C | 1.0 | µF |
| Q5 | PMOS,12 V, 16 mΩ, MLP2x2 | Fairchild FDMA905P | $R_{DS(ON)}$ | 16 | mΩ |
| $C_{REF}$ | 1 µF, 10%, 6.3 V, X5R, 0402 | | C | 1.0 | µF |

**Note:**

2. 6.3 V rating is sufficient for $C_{MID}$ since PMID is protected from over-voltage surges on VBUS by Q3.

## Pin Configuration

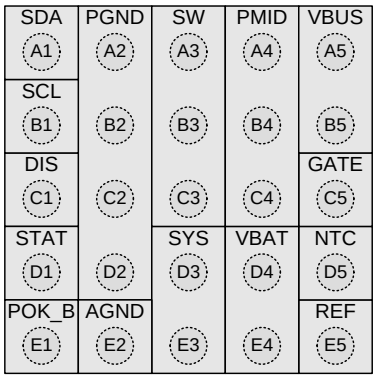



**Figure 3. Top View**

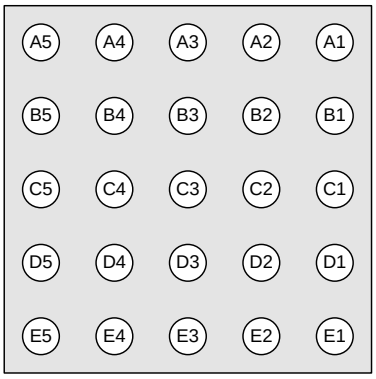



**Figure 4. Bottom View**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| A1 | SDA | **I²C Interface Serial Data**. This pin should not be left floating. |
| B1 | SCL | **I²C Interface Serial Clock**. This pin should not be left floating. |
| C1 | DIS | **Disable**. If this pin is held HIGH, Q1 and Q3 are turned off, creating a HIGH Z condition at VBUS and the PWM converter is disabled. |
| D1 | STAT | **Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in progress; can be used to signal the host processor when a fault condition occurs. |
| E1 | POK_B | **Power OK (FAN54040-2)**. Open-drain output that pulls LOW when VBUS is plugged in and the battery has risen above $V_{LOWV}$. This signal is used to signal the host processor that it can begin to draw significant current. |
| E1 | ILIM | **Input Current Limit (FAN54045-7)**. Controls input current limit in Auto-Charge Mode. When LOW, input current is limited to 100 mA maximum. When HIGH, input current is limited to 500 mA. In 32-Second Mode, the input current limit is set by the $I_{BUSLIM}$ bits. |
| A2 – D2 | PGND | **Power Ground**. Power return for gate drive and power transistors. The connection from this pin to the bottom of $C_{MID}$ should be as short as possible. |
| E2 | AGND | **Analog Ground**. All IC signals are referenced to this node. |
| A3 – C3 | SW | **Switching Node**. Connect to output inductor. |
| D3 – E3 | SYS | **System Supply**. Output voltage of the switching charger and input to the power path controller. Bypass SYS to PGND with a 10 µF capacitor. |
| A4 – C4 | PMID | **Power Input Voltage**. Power input to the charger regulator, bypass point for the input current sense. Bypass with a minimum of a 4.7 µF, 6.3 V capacitor to PGND. |
| D4 – E4 | VBAT | **Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 µF capacitor to PGND. VBAT is a power path connection. |
| A5 – B5 | VBUS | **Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1 µF capacitor to PGND. |
| C5 | GATE | **External MOSFET Gate**. This pin controls the gate of an external P-channel MOSFET transistor used to augment the internal ideal diode. The source of the P-channel MOSFET should be connected to SYS and the drain should be connected to VBAT. |
| D5 | NTC | **Thermistor input**. The IC compares this node with taps on a resistor divider from REF to inhibit auto-charging when the battery temperature is outside of permitted fast-charge limits. |
| E5 | REF | **Reference Voltage**. REF is a 1.8 V regulated output. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{BUS}$ | Voltage on VBUS Pin | Continuous | | -0.3 | 28.0 | V |
| | | Pulsed, 100 ms Maximum Non-Repetitive | | -1.0 | | |
| $V_I$ | Voltage on PMID Voltage Pin | | | –0.3 | 7.0 | V |
| | Voltage on SW, SYS, VBAT, STAT, DIS Pins | | | –0.3 | 7.0 | |
| $V_O$ | Voltage on Other Pins | | | –0.3 | 6.5[3] | V |
| $\frac{dV_{BUS}}{dt}$ | Maximum $V_{BUS}$ Slope Above 5.5 V when Boost or Charger Active | | | | 4 | V/µs |
| ESD | Electrostatic Discharge Protection Level[4] | Human Body Model per JESD22-A114 | | 2000 | | V |
| | | Charged Device Model per JESD22-C101 | | 500 | | |
| | IEC 61000-4-2 System ESD | USB Connector Pins ($V_{BUS}$ to GND) | Air Gap | 15 | | kV |
| | | | Contact | 8 | | |
| $T_J$ | Junction Temperature | | | –40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | | –65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | | +260 | °C |

**Note:**

3. Lesser of 6.5 V or $V_I$ + 0.3 V.
4. Guaranteed if $C_{BUS}$ ≥1µF and $C_{MID}$ ≥ 4.7µF.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BUS}$ | Supply Voltage | | 4 | 6 | V |
| $V_{BAT(MAX)}$ | Maximum Battery Voltage when Boost enabled | | | 4.5 | V |
| $-\frac{dV_{BUS}}{dt}$ | Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leq 4.7$ µF, *see VBUS Short While Charging* | $T_A \leq 60°C$ | | 4 | V/µs |
| | | $T_A \geq 60°C$ | | 2 | |
| $T_A$ | Ambient Temperature | | –30 | +85 | °C |
| $T_J$ | Junction Temperature *(see Thermal Regulation and Protection section)* | | –30 | +120 | °C |

## Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature $T_A$. *For measured data, see Table 18.*

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance *(see also Figure 18)* | 50 | °C/W |
| $\theta_{JB}$ | Junction-to-PCB Thermal Resistance | 20 | °C/W |

## Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$; $V_{BUS}$=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for $T_J$=25°C.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | | |
| $I_{VBUS}$ | VBUS Current | $V_{BUS} > V_{BUS(min)}$, PWM Switching | | | 10 | | mA |
| | | $V_{BUS} > V_{BUS(min)}$; $V_{BAT} > V_{OREG}$ $I_{BUSLIM}$=100 mA | | | 2.5 | | mA |
| | | 0°C < $T_J$ < 85°C, HZ_MODE=1 $V_{BAT} < V_{LOWV}$, 32S Mode, $I_{REG}$=0 | | | | 280 | µA |
| $I_{BAT\_HZ}$ | Battery Discharge Current in High-Impedance Mode | DIS=1, or HZ_MODE=1, $V_{BUS}$=0, 5 V or Floating, $V_{BAT}$=4.2 V | | | <1 | 10 | µA |
| $I_{BUS\_HZ}$ | Battery Leakage Current to $V_{BUS}$ in High-Impedance Mode | DIS=1, or HZ_MODE=1, $V_{BUS}$ Shorted to Ground, $V_{BAT}$=4.2 V | | -5.0 | -0.2 | | µA |
| **Charger Voltage Regulation** | | | | | | | |
| $V_{OREG}$ | Charge Voltage Range | | | 3.5 | | 4.4 | V |
| | Charge Voltage Accuracy | $T_A$=25°C | | –0.5 | | +0.5 | % |
| | | $T_J$=0 to 125°C | | –1 | | +1 | % |
| **Charging Current Regulation** | | | | | | | |
| $I_{OCHRG}$ | Output Charge Current Range | $V_{LOWV} < V_{BAT} < V_{OREG}$ | IO_LEVEL=0 | 550 | | 1550 | mA |
| | | | IO_LEVEL=1 | 290 | 340 | 390 | mA |
| | Charge Current Accuracy | IO_LEVEL=0 | | –5 | | +5 | % |
| **Weak Battery Detection** | | | | | | | |
| $V_{LOWV}$ | Weak Battery Threshold Range | | | 3.4 | | 3.7 | V |
| | Weak Battery Threshold Accuracy | | | –5 | | +5 | % |
| | Weak Battery Deglitch Time | Rising Voltage, 2 mV Overdrive | | | 30 | | ms |
| **Logic Levels : DIS, SDA, SCL** | | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | | | 1.05 | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | | | | 0.4 | V |
| $I_{IN}$ | Input Bias Current | Input Tied to GND or $V_{BUS}$ | | | 0.01 | 1.00 | µA |
| **Charge Termination Detection** | | | | | | | |
| $I_{(TERM)}$ | Termination Current Range | $V_{BAT} > V_{OREG} – V_{RCH}$, $V_{BUS} > V_{SLP}$ | | 50 | | 400 | mA |
| | Termination Current Accuracy | $I_{TERM}$ Setting ≤ 100 mA | | –15 | | +15 | % |
| | | $I_{TERM}$ Setting ≥ 200 mA | | –5 | | +5 | |
| | Termination Current Deglitch Time | | | | 30 | | ms |
| **Power Path (Q4) Control** | | | | | | | |
| $I_{LIN}$ | Power Path Max. Charge Current | | IO_LEVEL=1 | 290 | 340 | 390 | mA |
| | | $I_{BUSLIM}$ > 01, $I_{OCHARGE}$ ≤ 02 | IO_LEVEL=0 | 400 | 450 | 510 | mA |
| | | $I_{BUSLIM}$ > 01, $I_{OCHARGE}$ > 02 | IO_LEVEL=0 | 650 | 725 | 800 | mA |
| $V_{THSYS}$ | VBAT to SYS Threshold for Q4 and Gate Transition While Charging | (SYS-VBAT) Falling | | –6 | –5 | –3 | mV |
| | | (SYS-VBAT) Rising | | -1 | +1 | 2 | mV |
| **Production Test Mode** | | | | | | | |
| $V_{BAT(PTM)}$ | Production Test Output Voltage | 1 mA < $I_{BAT}$ < 2 A, $V_{BUS}$=5.5 V | | 4.116 | 4.200 | 4.284 | V |
| $I_{BAT(PTM)}$ | Production Test Output Current | 20% Duty with Max. Period 10 ms | | 2.3 | | | A |

*Continued on the following page…*

## Electrical Specifications (Continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$; $V_{BUS}$=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for $T_J$=25°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Input Power Source Detection** | | | | | | |
| T1 | T1 (0°C) Temperature Threshold | | 71.9 | 73.9 | 75.9 | % of $V_{REF}$ |
| T2 | T1 (10°C) Temperature Threshold | | 62.6 | 64.6 | 66.6 | |
| T3 | T1 (45°C) Temperature Threshold | | 31.9 | 32.9 | 34.9 | |
| T4 | T1 (60°C) Temperature Threshold | | 21.3 | 23.3 | 25.3 | |
| **Input Power Source Detection** | | | | | | |
| $V_{IN(MIN)1}$ | VBUS Input Voltage Rising | To Initiate and Pass VBUS Validation | | 4.29 | 4.42 | V |
| $V_{IN(MIN)2}$ | Minimum VBUS during Charge | During Charging | | 3.71 | 3.94 | V |
| $t_{VBUS\_VALID}$ | VBUS Validation Time | | | 30 | | ms |
| **$V_{BUS}$ Control Loop** | | | | | | |
| $V_{BUSLIM}$ | VBUS Loop Setpoint Accuracy | | –3 | | +3 | % |
| **Input Current Limit** | | | | | | |
| $I_{BUSLIM}$ | Charger Input Current Limit Threshold | $I_{BUSLIM}$ Set to 100 mA | 88 | 93 | 98 | mA |
| | | $I_{BUSLIM}$ Set to 500 mA | 450 | 475 | 500 | |
| **$V_{REF}$ Bias Generator** | | | | | | |
| $V_{REF}$ | Bias Regulator Voltage | $V_{BUS} > V_{IN(MIN)}$ | | 1.8 | | V |
| | Short-Circuit Current Limit | | | 2.5 | | mA |
| **Battery Recharge Threshold** | | | | | | |
| $V_{RCH}$ | Recharge Threshold | Below $V_{(OREG)}$ | 100 | 120 | 150 | mV |
| | Deglitch Time | $V_{BAT}$ Falling Below $V_{RCH}$ Threshold | | 130 | | ms |
| **STAT, POK_B Output** | | | | | | |
| $V_{STAT(OL)}$ | STAT Output Low | $I_{STAT}$=10 mA | | | 0.4 | V |
| $I_{STAT(OH)}$ | STAT High Leakage Current | $V_{STAT}$=5 V | | | 1 | µA |
| **Battery Detection** | | | | | | |
| $I_{DETECT}$ | Battery Detection Current before Charge Done (Sink Current)[5] | Begins after Termination Detected and $V_{BAT} \le V_{OREG} - V_{RCH}$ | | –0.8 | | mA |
| $t_{DETECT}$ | Battery Detection Time | | | 262 | | ms |
| **Sleep Comparator** | | | | | | |
| $V_{SLP}$ | Sleep-Mode Entry Threshold, $V_{BUS} - V_{BAT}$ | 2.3 V ≤ $V_{BAT}$ ≤ $V_{OREG}$, $V_{BUS}$ Falling | 0 | 0.04 | 0.10 | V |
| **Power Switches** *(see Figure 2)* | | | | | | |
| $R_{DS(ON)}$ | Q3 On Resistance (VBUS to PMID) | $I_{IN(LIMIT)}$=500 mA | | 180 | 250 | mΩ |
| | Q1 On Resistance (PMID to SW) | | | 130 | 225 | |
| | Q2 On Resistance (SW to GND) | | | 150 | 225 | |
| | Q4 On Resistance (SYS to VBAT) | $V_{BAT}$=4.2 V | | 70 | 100 | mΩ |
| $I_{SYNC}$ | Synchronous to Non-Synchronous Current Cut-Off Threshold[6] | Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit | | 140 | | mA |

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## Electrical Specifications (Continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$; $V_{BUS}$=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for $T_J$=25°C.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Charger PWM Modulator** | | | | | | | |
| $f_{SW}$ | Oscillator Frequency | | | 2.7 | 3.0 | 3.3 | MHz |
| $D_{MAX}$ | Maximum Duty Cycle | | | | | 100 | % |
| $D_{MIN}$ | Minimum Duty Cycle | | | | 0 | | % |
| **Boost Mode Operation (OPA_MODE=1, HZ_MODE=0)** | | | | | | | |
| $V_{BOOST}$ | Boost Output Voltage at VBUS | 2.5 V < $V_{BAT}$ < 4.5 V, $I_{LOAD}$ from 0 to 200 mA | | 4.80 | 5.07 | 5.20 | V |
| | | 3.0 V < $V_{BAT}$ < 4.5 V, $I_{LOAD}$ from 0 to 500 mA | | 4.77 | 5.07 | 5.20 | |
| $I_{BAT(BOOST)}$ | Boost Mode Quiescent Current | PFM Mode, $V_{BAT}$=3.6 V, $I_{LOAD}$=0 | | | 250 | 350 | µA |
| $I_{LIMPK(BST)}$ | Q2 Peak Current Limit | | | 1350 | 1550 | 1950 | mA |
| $UVLO_{BST}$ | Minimum Battery Voltage for Boost Operation | While Boost Active | | | 2.32 | | V |
| | | To Start Boost Regulator | | | 2.48 | 2.70 | |
| **VBUS Load Resistance** | | | | | | | |
| $R_{VBUS}$ | VBUS to PGND Resistance | Normal Operation | | | 500 | | kΩ |
| | | VBUS Validation | | | 100 | | Ω |
| **Protection and Timers** | | | | | | | |
| $VBUS_{OVP}$ | VBUS Over-Voltage Shutdown | $V_{BUS}$ Rising | | 6.09 | 6.29 | 6.49 | V |
| | Hysteresis | $V_{BUS}$ Falling | | | 100 | | mV |
| $I_{LIMPK(CHG)}$ | Q1 Cycle-by-Cycle Peak Current Limit | Charge Mode | | | 3 | | A |
| $V_{SHORT}$ | Battery Short-Circuit Threshold | $V_{BAT}$ Rising | | 1.95 | 2.00 | 2.05 | V |
| | Hysteresis | | | | 100 | | mV |
| $I_{SHORT}$ | Linear Charging Current | $V_{BAT}$ < $V_{SHORT}$ | Power Path | | 13 | | mA |
| | | | Linear | | 30 | | |
| $T_{SHUTDWN}$ | Thermal Shutdown Threshold[7] | $T_J$ Rising | | | 145 | | °C |
| | Hysteresis[7] | $T_J$ Falling | | | 25 | | |
| $T_{CF}$ | Thermal Regulation Threshold[7] | Charge Current Reduction Begins | | | 120 | | °C |
| $t_{INT}$ | Detection Interval | | | | 2.1 | | s |
| $t_{32S}$ | 32-Second Timer[8] | Charger Enabled | | 20.5 | 25.2 | 28.0 | s |
| | | Charger Disabled | | 18.0 | 25.2 | 34.0 | |
| $t_{15MIN}$ | 15-Minute Timer | 15-Minute Mode (FAN54040, FAN54042, FAN54046, FAN54047) | | 12.0 | 13.5 | 15.0 | min |
| $\Delta t_{LF}$ | Low-Frequency Timer Accuracy | Charger Inactive | | –25 | | 25 | % |

**Notes:**

5. Negative current is current flowing from the battery to VBUS (discharging the battery).
6. Q2 always turns on for 60 ns, then turns off if current is below $I_{SYNC}$.
7. Guaranteed by design; not tested in production.
8. This tolerance (%) applies to all timers on the IC, including soft-start and deglitching timers.

## $I^2C$ Timing Specifications

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | Standard Mode | | | 100 | kHz |
| | | Fast Mode | | | 400 | |
| | | Fast Mode Plus | | | 1000 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | | 3400 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | | 1700 | |
| $t_{BUF}$ | BUS-free Time between STOP and START Conditions | Standard Mode | | 4.7 | | µs |
| | | Fast Mode | | 1.3 | | |
| | | Fast Mode Plus | | 0.5 | | |
| $t_{HD;STA}$ | START or Repeated START Hold Time | Standard Mode | | 4 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| $t_{LOW}$ | SCL LOW Period | Standard Mode | | 4.7 | | µs |
| | | Fast Mode | | 1.3 | | µs |
| | | Fast Mode Plus | | 0.5 | | µs |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 160 | | ns |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 320 | | ns |
| $t_{HIGH}$ | SCL HIGH Period | Standard Mode | | 4 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 60 | | ns |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 120 | | ns |
| $t_{SU;STA}$ | Repeated START Setup Time | Standard Mode | | 4.7 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| $t_{SU;DAT}$ | Data Setup Time | Standard Mode | | 250 | | ns |
| | | Fast Mode | | 100 | | |
| | | Fast Mode Plus | | 50 | | |
| | | High-Speed Mode | | 10 | | |
| $t_{HD;DAT}$ | Data Hold Time | Standard Mode | 0 | | 3.45 | µs |
| | | Fast Mode | 0 | | 900 | ns |
| | | Fast Mode Plus | 0 | | 450 | ns |
| | | High-Speed Mode, $C_B \leq 100$ pF | 0 | | 70 | ns |
| | | High-Speed Mode, $C_B \leq 400$ pF | 0 | | 150 | ns |
| $t_{RCL}$ | SCL Rise Time | Standard Mode | $20+0.1C_B$ | | 1000 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 160 | |

*Continued on the following page…*

## $I^2C$ Timing Specifications (Continued)

Guaranteed by design.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{FCL}$ | SCL Fall Time | Standard Mode | | $20+0.1C_B$ | 300 | ns |
| | | Fast Mode | | $20+0.1C_B$ | 300 | |
| | | Fast Mode Plus | | $20+0.1C_B$ | 120 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 40 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 80 | |
| $t_{RCL1}$ | Rise Time of SCL after a Repeated START Condition and after ACK Bit | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 80 | ns |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 160 | |
| $t_{RDA}$ | SDA Rise Time | Standard Mode | | $20+0.1C_B$ | 1000 | ns |
| | | Fast Mode | | $20+0.1C_B$ | 300 | |
| | | Fast Mode Plus | | $20+0.1C_B$ | 120 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 160 | |
| $t_{FDA}$ | SDA Fall Time | Standard Mode | | $20+0.1C_B$ | 300 | ns |
| | | Fast Mode | | $20+0.1C_B$ | 300 | |
| | | Fast Mode Plus | | $20+0.1C_B$ | 120 | |
| | | High-Speed Mode, $C_B \leq 100$ pF | | 10 | 80 | |
| | | High-Speed Mode, $C_B \leq 400$ pF | | 20 | 160 | |
| $t_{SU;STO}$ | Stop Condition Setup Time | Standard Mode | | 4 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 120 | | ns |
| | | High-Speed Mode | | 160 | | ns |
| $C_B$ | Capacitive Load for SDA and SCL | | | | 400 | pF |

## Timing Diagrams

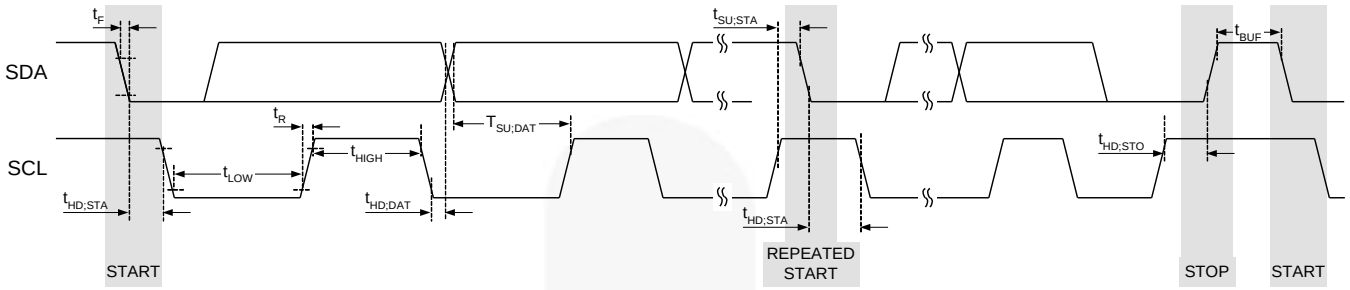
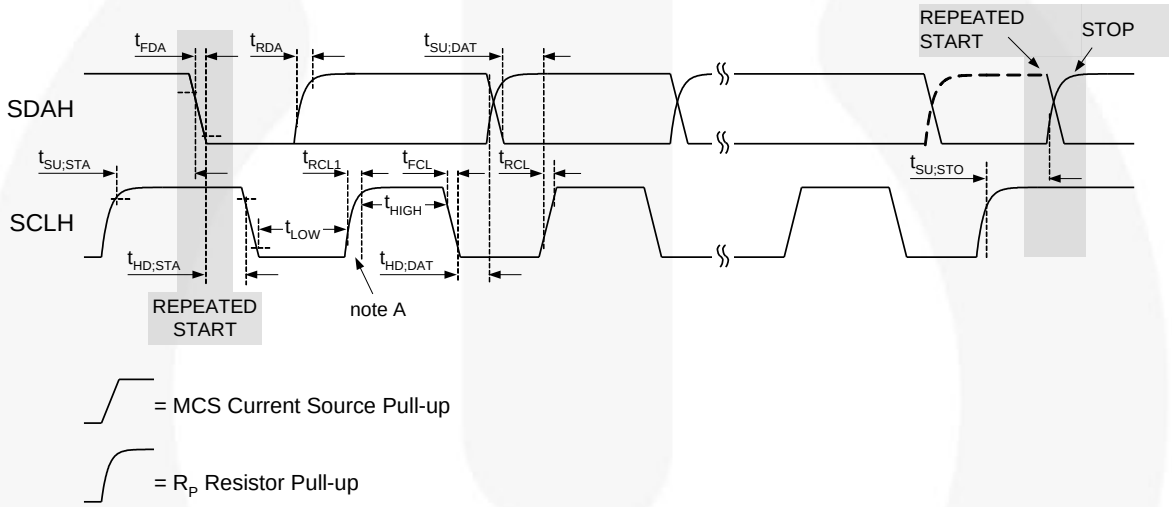



**Figure 5. I²C Interface Timing for Fast and Slow Modes**




Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

**Figure 6. I²C Interface Timing for High-Speed Mode**

## Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}$=4.2 V, $V_{BUS}$=5.0 V, and $T_A$=25°C.

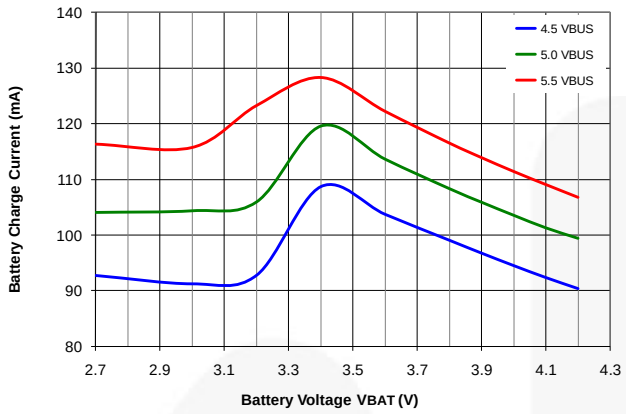



**Figure 7. Battery Charge Current vs. $V_{BUS}$ with $I_{BUSLIM}$=100 mA**

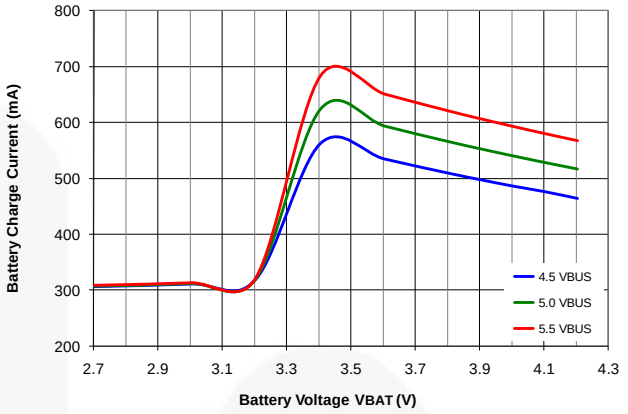



**Figure 8. Battery Charge Current vs. $V_{BUS}$ with $I_{BUSLIM}$=500 mA**

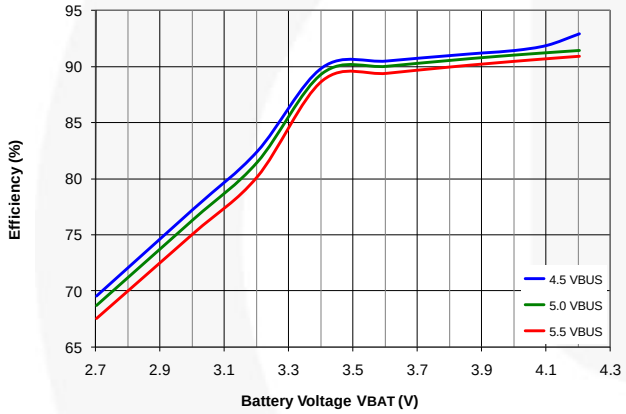



**Figure 9. Efficiency vs. $V_{BUS}$, $I_{BUSLIM}$=500 mA, $I_{SYS}$=0**

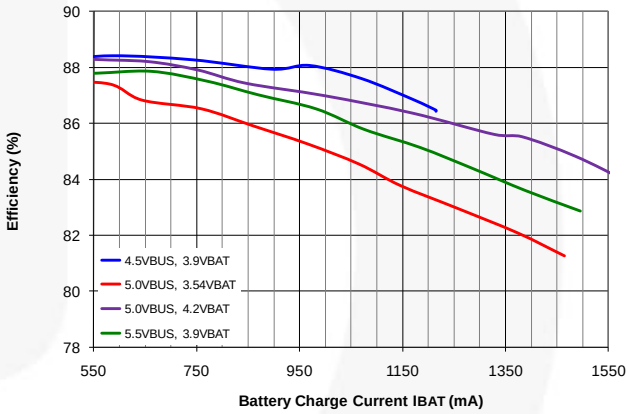



**Figure 10. Efficiency vs. Charging Current, $I_{BUSLIM}$=No Limit**

## Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}$=4.2 V, $V_{BUS}$=5.0 V, and $T_A$=25°C.

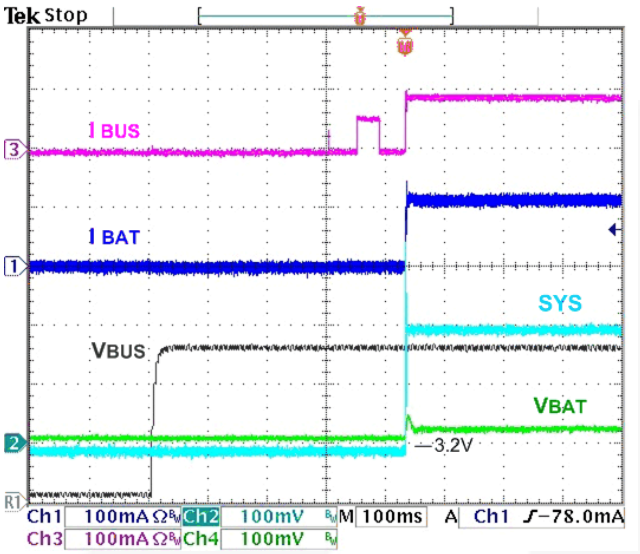



**Figure 11. Charger Startup at $V_{BUS}$ Plug-In, 100 mA $I_{BUSLIM}$, 3.2 $V_{BAT}$, 100 Ω SYS Load**

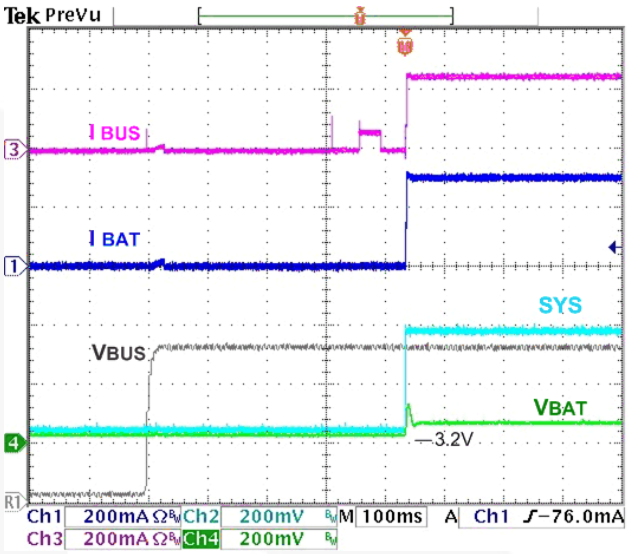



**Figure 12. Charger Startup at $V_{BUS}$ Plug-In, 500 mA $I_{INBUSLIM}$, 3.2 $V_{BAT}$, 100 Ω SYS Load**

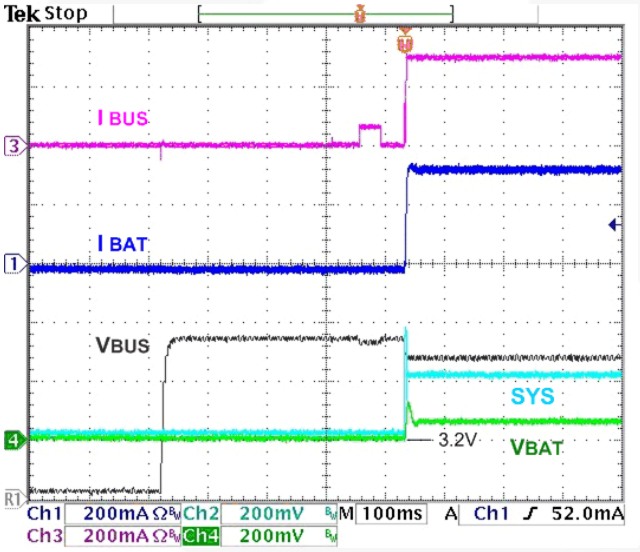



**Figure 13. Charger Startup at $V_{BUS}$ Plug-In Using 300 mA Current Limited Source, 500 mA $I_{BUSLIM}$, 3.2 $V_{BAT}$, 50 Ω SYS Load**

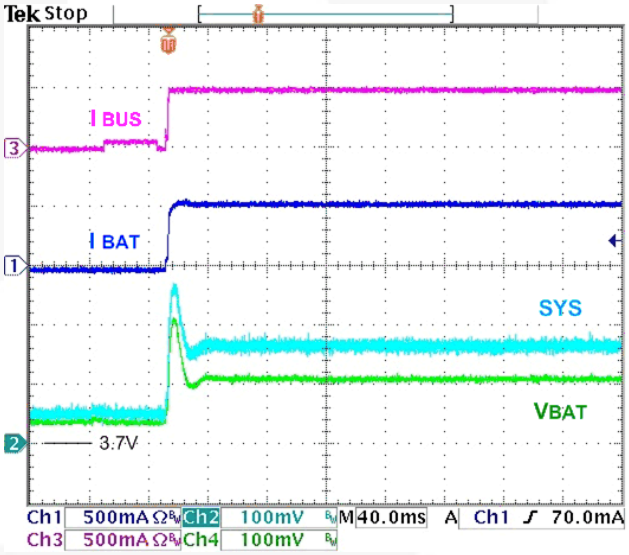



**Figure 14. Charger Startup with HZ Bit Reset, 500 mA $I_{BUSLIM}$, 950 mA $I_{CHARGE}$, 50 Ω SYS Load**

## Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}$=4.2 V, $V_{BUS}$=5.0 V, and $T_A$=25°C.

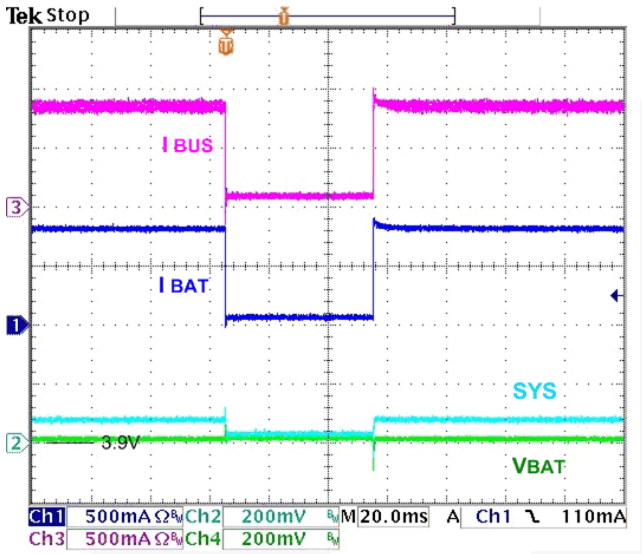



**Figure 15. Battery Removal / Insertion while Charging, TE=0, 3.9 $V_{BAT}$, $I_{CHRG}$=950 mA, $I_{BUSLIM}$=No Limit, 50 Ω SYS Load**

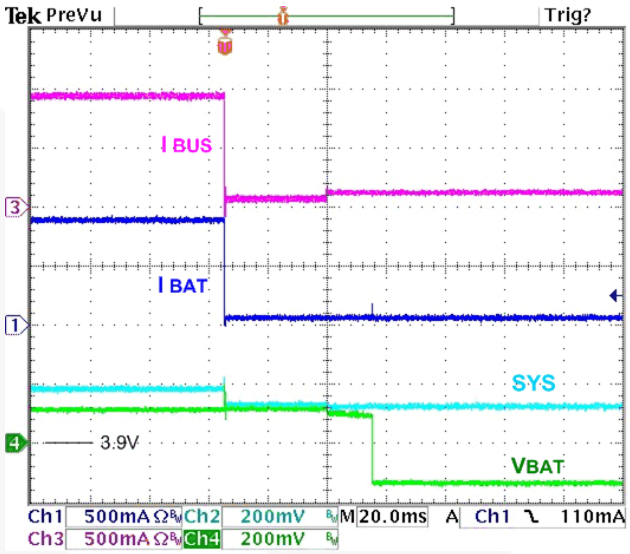



**Figure 16. Battery Removal / Insertion when Charging, TE=1, 3.9 $V_{BAT}$, $I_{CHRG}$=950 mA, $I_{BUSLIM}$=No Limit, 50 Ω SYS Load**

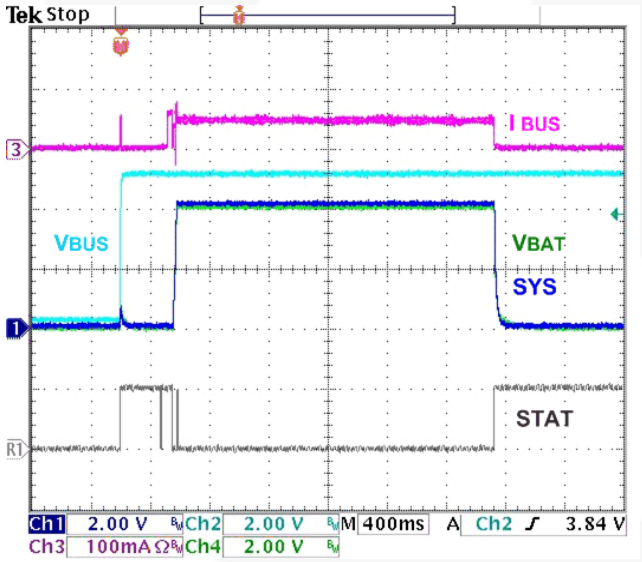



**Figure 17. No Battery at $V_{BUS}$ Power-Up, FAN54040, 100 Ω SYS Load, 1 kΩ $V_{BAT}$ Load**

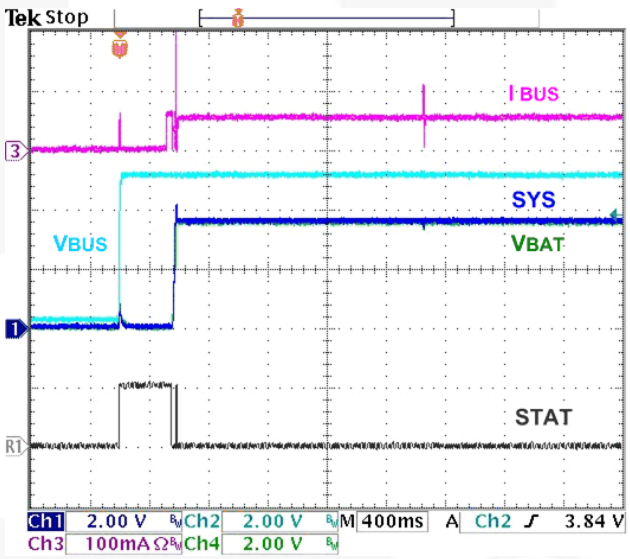



**Figure 18. No Battery at $V_{BUS}$ Power-Up, FAN54042, 100 Ω SYS Load, 1 kΩ $V_{BAT}$ Load**

## Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, $V_{OREG}$=4.2 V, $V_{BUS}$=5.0 V, and $T_A$=25°C.

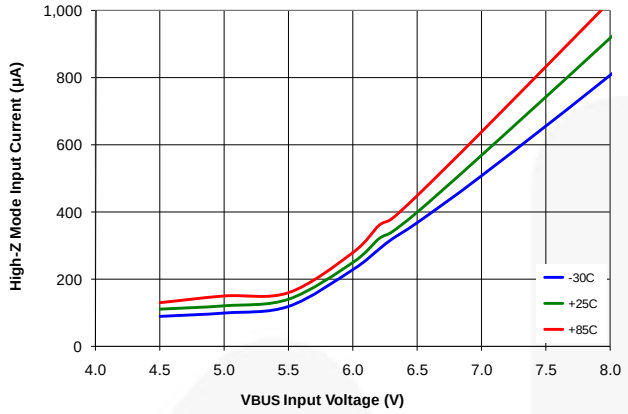



**Figure 19. HZ Mode VBUS Current vs. Temperature, 3.7 $V_{BAT}$**

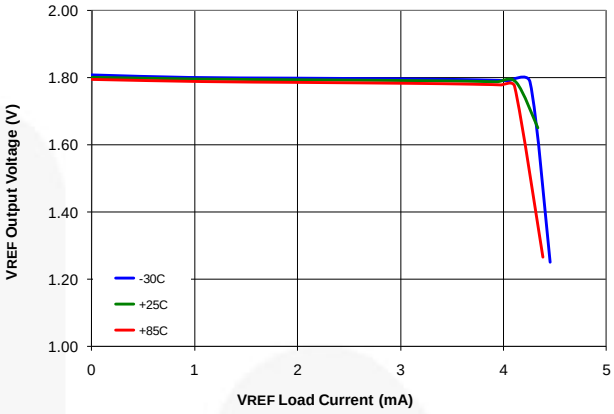



**Figure 20. $V_{REF}$ vs. Load Current, Over-Temperature, 5.0 $V_{BUS}$**

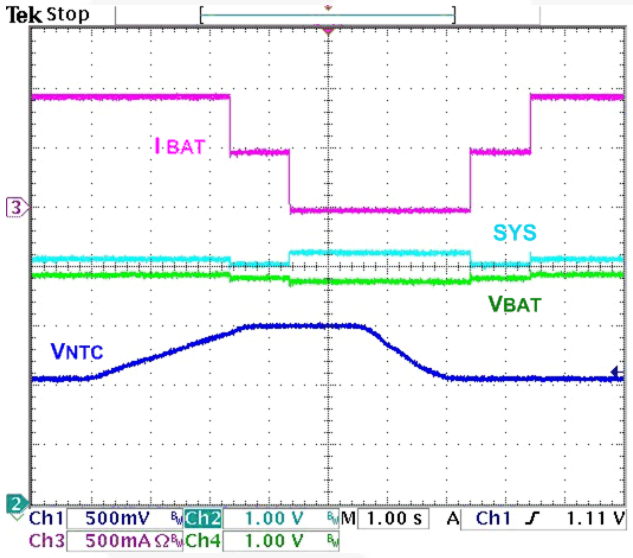



**Figure 21. Charging vs. Temperature (NTC), +30°C to -10°C 3.7 $V_{BAT}$, $I_{CHRG}$=950 mA, No $I_{BUSLIM}$, 100 Ω SYS Load**

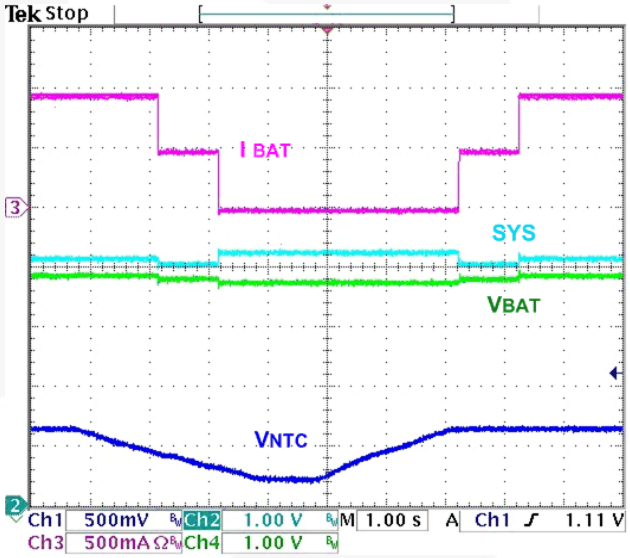



**Figure 22 Charging vs. Temperature (NTC), +30°C to +70°C 3.7 $V_{BAT}$, $I_{CHRG}$=950 mA, No $I_{BUSLIM}$, 100 Ω SYS Load**

## GSM Typical Characteristics

A 2.0 A GSM pulse applied at VBAT with 5 µs rise / fall time. Simultaneous to GSM pulse, 50 Ω additional load applied at SYS.

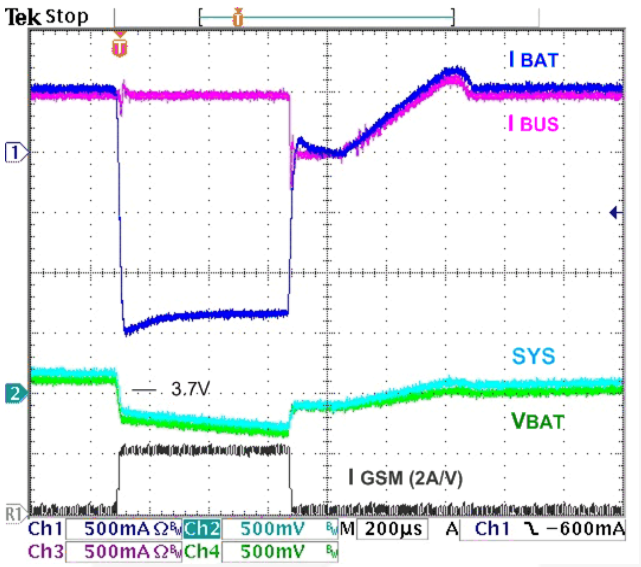



**Figure 23. 2.0 A GSM Pulse Response, $I_{BUSLIM}$=500 mA Control, $I_{CHRG}$=950 mA, 3.7 $V_{BAT}$, OREG=4.2 V**

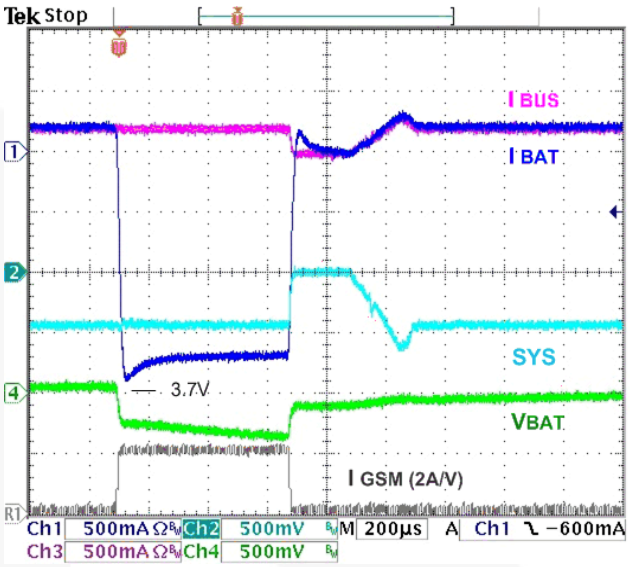



**Figure 24. 2.0 A GSM Pulse Response, $I_{BUSLIM}$=500 mA, $I_{CHRG}$=950 mA, 3.7 $V_{BAT}$, OREG=4.2 V, 200 mA Source Current Limit**

## Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, $V_{BAT}$=3.6 V, $T_A$=25°C.

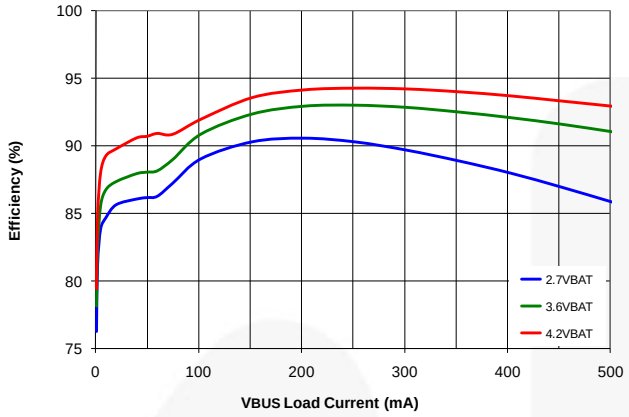



**Figure 25. Efficiency vs. $I_{BUS}$ Over $V_{BAT}$**

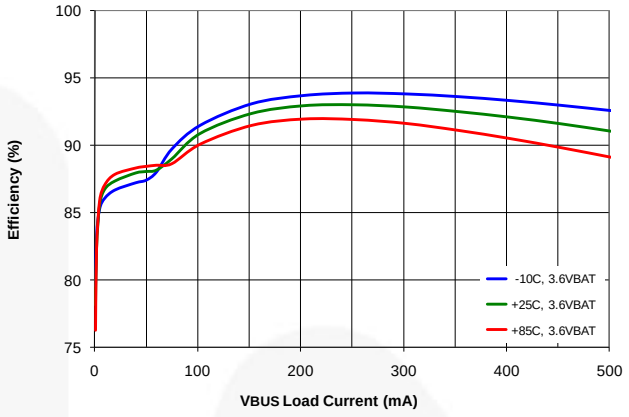



**Figure 26. Efficiency vs. $I_{BUS}$ Over-Temperature, 3.6 $V_{BAT}$**

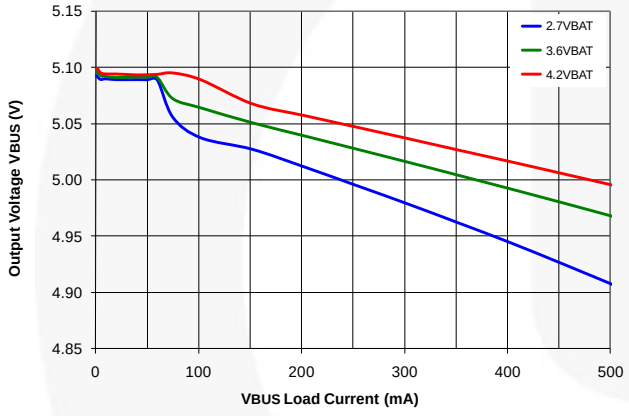



**Figure 27. Regulation vs. $I_{BUS}$ Over $V_{BAT}$**

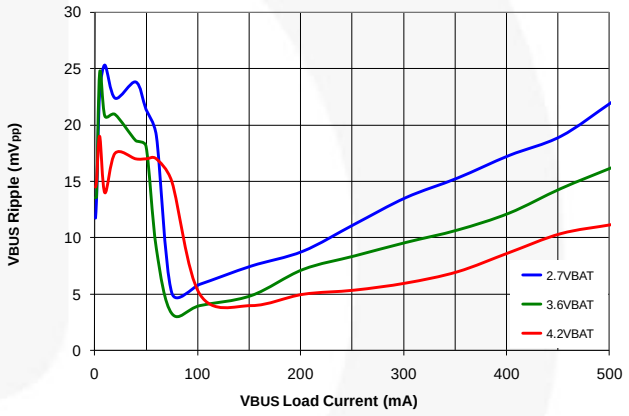



**Figure 28. Output Ripple vs. $I_{BUS}$ Over $V_{BAT}$**

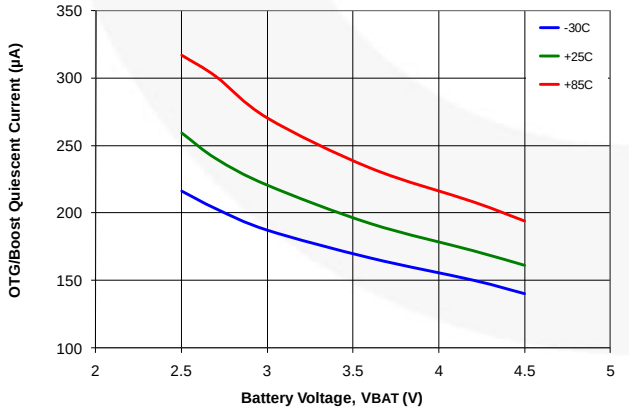



**Figure 29. Quiescent Current ($I_Q$) vs. $V_{BAT}$ Over-Temperature**

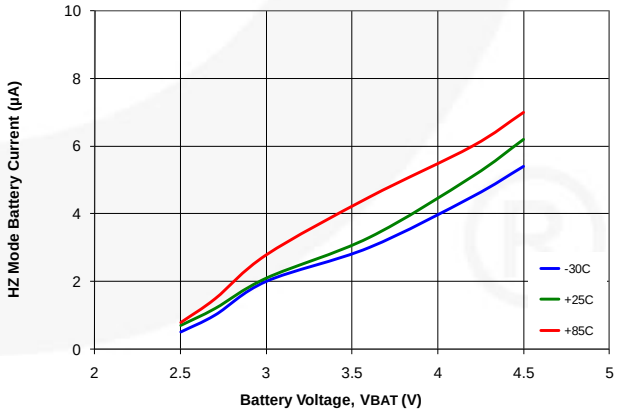



**Figure 30. Battery Discharge Current vs. $V_{BAT}$, HZ / Sleep Mode**

## Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, $V_{BAT}$=3.6 V, $T_A$=25°C.

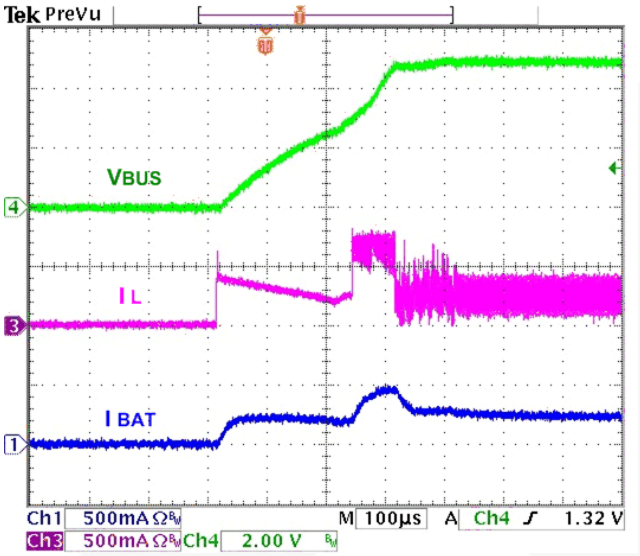



**Figure 31. OTG Startup, 50 Ω Load, 3.6 $V_{BAT}$ External / Additional 10 µf on VBUS**

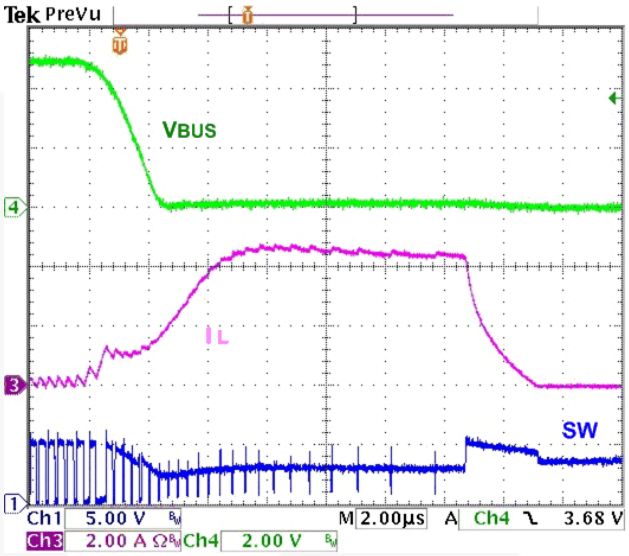



**Figure 32. OTG $V_{BUS}$ Overload Response**

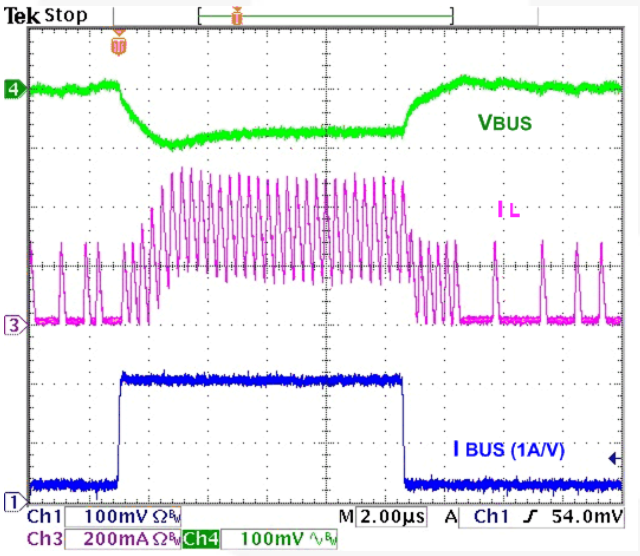



**Figure 33. Load Transient, 20-200-20 mA $I_{BUS}$, $t_{RISE/FALL}$=100 ns**

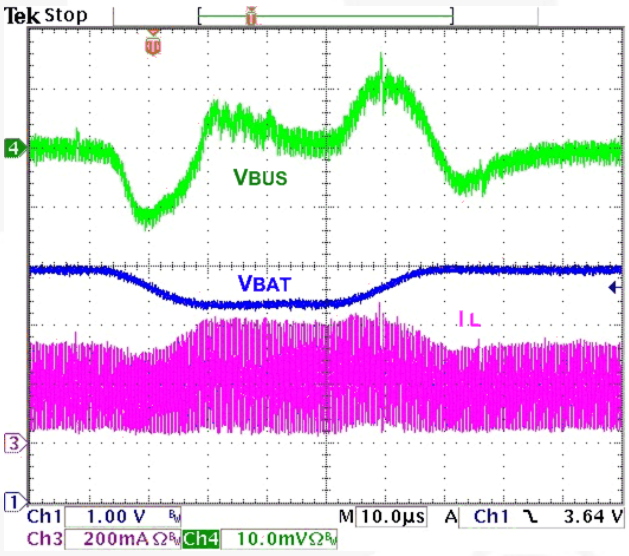



**Figure 34. Line Transient, 50 Ω Load, 3.9-3.3-3.9 $V_{BAT}$, $t_{RISE/FALL}$=10 µs**

## Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

FAN5404X combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The FAN5404X employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN5404X has four operating modes:

1. Charge Mode:
   Charges a single-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator, using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.
4. Production Test Mode
   This mode provides 4.2 V output on VBAT and supplies a load current of up to 2.3 A.

## Charge Mode

In Charge Mode, FAN5404X employs six regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the $I^2C$ interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an internal sense MOSFET.
3. VBUS Voltage: This loop is designed to prevent the input supply from being dragged below $V_{BUSLIM}$ (typically 4.5 V) when the input power source is current limited. An example of this would be a travel charger. This loop cuts back the current when $V_{BUS}$ approaches $V_{BUSLIM}$, allowing the input source to run in current limit.
4. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current through Q4 drops below the $I_{TERM}$ threshold.
5. Power Path: When $V_{BAT}$ is below $V_{BATMIN}$, Q4 operates as a linear current source and modulates its current to ensure that the voltage on SYS stays above 3.4 V.
6. Temperature: If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature is below 120°C.

## Battery Charging Curve

If the battery voltage is below $V_{SHORT}$, a linear current source pre-charges the battery until $V_{BAT}$ reaches $V_{SHORT}$. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The FAN5404X is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, $I_{BUSLIM}$ or the programmed charging current limits the amount of current available to charge the battery and power the system. The effect of $I_{BUSLIM}$ on $I_{CHARGE}$ can be seen in Figure 36.

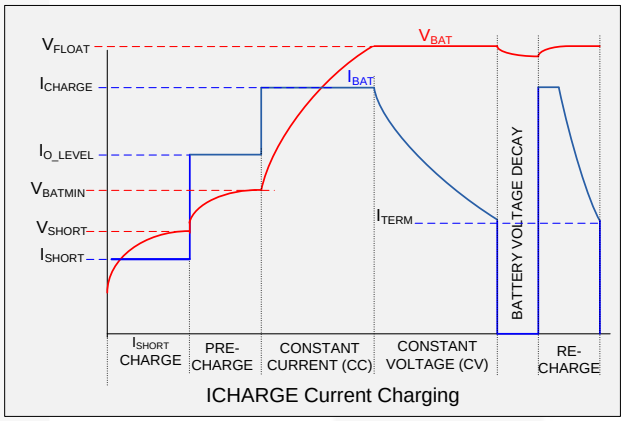



**Figure 35. Charge Curve, $I_{CHARGE}$ Not Limited by $I_{INLIM}$**

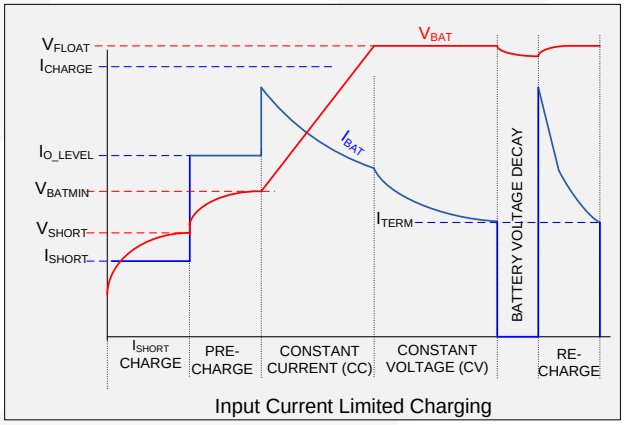



**Figure 36. Charge Curve, $I_{BUSLIM}$ Limits $I_{CHARGE}$**

Assuming that $V_{OREG}$ is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to $V_{OREG}$ declines and the charger enters the voltage regulation phase of charging. When the current declines to the programmed $I_{TERM}$ value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG1[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments, as shown in Table 4.

The following charging parameters can be programmed by the host through $I^2C$:

**Table 3. Programmable Charging Parameters**

| Parameter | Name | Register |
|---|---|---|
| Output Voltage Regulation | $V_{OREG}$ | REG2[7:2] |
| Battery Charging Current Limit | $I_{OCHRG}$ | REG4[6:3] |
| Input Current Limit | $I_{INLIM}$ | REG1[7:6] |
| Charge Termination Limit | $I_{TERM}$ | REG4[2:0] |
| Weak Battery Voltage | $V_{LOWV}$ | REG1[5:4] |

**Table 4. OREG Bits (OREG[7:2]) vs. Charger $V_{OUT}$ ($V_{OREG}$) Float Voltage**

| Decimal | Hex | VOREG | Decimal | Hex | VOREG |
|---|---|---|---|---|---|
| 0 | 00 | 3.50 | 24 | 18 | 3.98 |
| 1 | 01 | 3.52 | 25 | 19 | 4.00 |
| **2** | **02** | **3.54** | 26 | 1A | 4.02 |
| 3 | 03 | 3.56 | 27 | 1B | 4.04 |
| 4 | 04 | 3.58 | 28 | 1C | 4.06 |
| 5 | 05 | 3.60 | 29 | 1D | 4.08 |
| 6 | 06 | 3.62 | 30 | 1E | 4.10 |
| 7 | 07 | 3.64 | 31 | 1F | 4.12 |
| 8 | 08 | 3.66 | 32 | 20 | 4.14 |
| 9 | 09 | 3.68 | 33 | 21 | 4.16 |
| 10 | 0A | 3.70 | 34 | 22 | 4.18 |
| 11 | 0B | 3.72 | 35 | 23 | 4.20 |
| 12 | 0C | 3.74 | 36 | 24 | 4.22 |
| 13 | 0D | 3.76 | 37 | 25 | 4.24 |
| 14 | 0E | 3.78 | 38 | 26 | 4.26 |
| 15 | 0F | 3.80 | 39 | 27 | 4.28 |
| 16 | 10 | 3.82 | 40 | 28 | 4.30 |
| 17 | 11 | 3.84 | 41 | 29 | 4.32 |
| 18 | 12 | 3.86 | 42 | 2A | 4.34 |
| 19 | 13 | 3.88 | 43 | 2B | 4.36 |
| 20 | 14 | 3.90 | 44 | 2C | 4.38 |
| 21 | 15 | 3.92 | 45 | 2D | 4.40 |
| 22 | 16 | 3.94 | 46 | 2E | 4.42 |
| 23 | 17 | 3.96 | 47 - 63 | 2F-3F | 4.44 |

**Note:**

9. Default settings are denoted by **bold** typeface.

Provided DIS, CE# and HZ_MODE are LOW, a new charge cycle begins when one of the following occurs:

1. The battery voltage falls below $V_{OREG}$ - $V_{RCH}$ after charge termination has occurred.
2. Any $I^2C$ write occurs causing the T32 s timer to run.

Products that include the auto-charge feature also begin charging if:

**3.** VBUS Power-on-Reset (POR) occurs and the battery voltage is below the weak battery threshold ($V_{LOWV}$).

## Charge Current Limit ($I_{OCHARGE}$)

**Table 5. $I_{OCHARGE}$ Current as Function of $I_{OCHARGE}$ Bits (REG4 [6:3])**

| DEC | BIN | HEX | $I_{OCHARGE}$ (mA) |
|---|---|---|---|
| **0** | **0000** | **0** | **550** |
| 1 | 0001 | 1 | 650 |
| 2 | 0010 | 2 | 750 |
| 3 | 0011 | 3 | 850 |
| 4 | 0100 | 4 | 950 |
| 5 | 0101 | 5 | 1,050 |
| 6 | 0110 | 6 | 1,150 |
| 7 | 0111 | 7 | 1,250 |
| 8 | 1000 | 8 | 1,350 |
| 9 | 1001 | 9 | 1,450 |
| 10-15 | 1010-1111 | A-F | 1,550 |

When the IO_LEVEL bit is set (default), the $I_{OCHARGE}$ bits are ignored and charge current is set to 340 mA.

## PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a negative current limit that turns off Q2 at 140 mA to prevent current flow from the battery.

## Termination Current Limit

Current charge termination is enabled when TE (REG1[3])=1. Typical termination current values are given in Table 6.

**Table 6. Termination Current as Function of ITERM Bits (REG4[2:0]) or PC_IT Bits (REG7[2:0]**

| ITERM Bits or PC_IT Bits | Termination Current (mA) |
|---|---|
| 0 | 50 |
| **1** | **100** |
| 2 | 150 |
| 3 | 200 |
| 4 | 250 |
| 5 | 300 |
| 6 | 350 |
| 7 | 400 |

When the charge current falls below $I_{TERM;}$ PWM charging stops, but the STAT pin remains LOW. The STAT pin then goes HIGH and the STATUS bits change to CHARGE DONE (10), provided the battery and charger are still connected.

A post-charging feature, “top-off” charging, is available to continue the battery charging to a lower charge current to maximize battery capacity. The PC_EN bit must be set to 1 before the battery charging current reaches the termination current $I_{TERM}$ for normal charging. The post-charging termination current is set by the PC_IT[2:0] bits, as shown in Table 6. If PC_EN is set to 1; right after the normal charging is ended as described above, post charging is started with PC_ON monitor bit set to 1. Once the current reaches the

threshold for post-charging completion, PWM charging stops and PC_ON bit changes back to 0.

During post-charging, the STAT pin is HIGH, indicating that the charge current is below the $I_{TERM}$ level. To exit post-charging, one of the following must occur: a $V_{BUS}$ POR, the POK_B cycled when $V_{BAT}$ <3.0 V, or the CE# or HZ_Mode bit cycled.

## Safety Timer

At the beginning of charging, the IC starts a 15-minute timer ($t_{15MIN}$ ). When this timer times out, charging is terminated. Writing to any register through $I^2C$ stops and resets the $t_{15MIN}$ timer, which in turn starts a 32-second timer ($t_{32S}$). Setting the TMR_RST bit (REG0[7]) resets the $t_{32S}$ timer. If the $t_{32S}$ timer times out; charging is terminated, the registers are set to their default values, and charging resumes using the default values with the $t_{15MIN}$ timer running.

Normal charging is controlled by the host with the $t_{32S}$ timer running to ensure that the host is alive. Charging with the $t_{15MIN}$ timer running is used for charging unattended by the host. If the $t_{15MIN}$ timer expires, the IC turns off the charger and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This sequence prevents overcharge if the host fails to reset the $t_{32S}$ timer.

## $V_{BUS}$ POR / Non-Compliant Charger Rejection

256 ms after VBUS is connected, the IC pulses the STAT pin and sets the VBUS_CON bit. Before starting to supply current, the IC applies a 110 Ω load from VBUS to GND. $V_{BUS}$ must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for $t_{VBUS\_VALID}$ (32 ms) before the IC initiates charging or supplies power to SYS. The $V_{BUS}$ validation sequence always occurs before significant current is drawn from VBUS (for example, after a VBUS OVP fault or a $V_{RCH}$ recharge initiation). $t_{VBUS\_VALID}$ ensures that unfiltered 50/60 Hz chargers and other non-compliant chargers are rejected.

## USB-Friendly Boot Sequence

At $V_{BUS}$ POR, when the battery voltage is above the weak battery threshold ($V_{LOWV}$); the IC operates in accordance with its $I^2C$ register settings. If $V_{BAT}$ < $V_{LOWV}$ and $t_{32s}$ is not running, the IC sets all registers to their default values and begins to deliver power to SYS.

FAN54040, FAN54042, and FAN54047 feature auto-charge, which allow these parts to deliver charge to the battery prior to receiving host commands.

FAN54041 does not automatically initiate charging at $V_{BUS}$ POR. Instead, it waits in IDLE state for the host to initiate charging through $I^2C$ commands. While in IDLE state, Q4 and Q5 are on. This allows the system to run through a separate power path without requiring an additional disconnection MOSFET.

## Power Path Operation

As long as $V_{BAT}$ < $V_{BATMIN}$, Q4 operates as a linear current source, (Power Path Mode) with its current limited to 340 mA. The IC then regulates SYS to 3.54 V and attempts to charge the battery with as much current as possible with the available $I_{BUSLIM}$ input current, without allowing SYS to drop below 3.4 V. This ensures that system power always receives first priority from a limited input supply. During this time, POK_B is HIGH. If $V_{BAT}$ < $V_{SHORT}$, Q4's current is further reduced to about 13 mA ($I_{SHORT}$) when $I_{BUSLIM}$ is set to 100 or 500 mA. For all other input current limits, $I_{SHORT}$ current is approximately 30 mA.

The POK_B signal can be used to keep the system in a low-power state, preventing excessive loading from the system while attempting to charge a depleted battery.

**Table 7. VBATMIN Thresholds to Exit Power Path Mode**

| $I_{BUSLIM}$ (mA) | $V_{BATMIN}$ (V) |
|---|---|
| 100 | 3.4 |
| 500 | 3.3 |
| 800 | 3.2 |
| No Limit | 3.2 |

After $V_{BAT}$ reaches $V_{BATMIN}$, Q4 closes and is used as a current-sense element to limit $I_{CHARGE}$ per the $I^2C$ register settings by limiting the PWM modulator's current (Full PWM Mode). During PWM Mode, if SYS drops more than 5 mV ($V_{THSYS}$) below $V_{BAT}$, Q4 and Q5 are turned on (GATE is pulled LOW). Once SYS voltage becomes higher than $V_{BAT}$, Q5 is turned off and Q4 again serves as the current-sense element to limit $I_{OCHARGE}$.

Q4 and Q5 are both turned on when the IC enters SLEEP Mode ($V_{BUS}$ < $V_{BAT}$).

POK_B pulls LOW once $V_{BAT}$ reaches $V_{LOWV}$, and remains LOW as long as the IC is in Full PWM Mode. The IC remains in Full PWM Mode as long as $V_{BAT}$ > 3.0 V, at which point, the IC enters Power Path Charging Mode.

## Startup with a Dead Battery

At $V_{BUS}$ POR, a 2 kΩ load is applied to VBAT for 256 ms to discharge any residual system capacitance in case the battery is absent or its discharge protection switch is open.

If $V_{BAT}$ < $V_{LOWV}$, all registers are reset to default values and the IC charges in T15Min Mode. If $V_{BAT}$ < $V_{SHORT}$, the SAFETY register is reset to its default value and the Battery Detection test below is performed.

### Battery Detection

If $V_{BAT}$ is below $V_{SHORT}$ when charging is enabled, the DBAT_B bit is reset and the IC (except FAN54045 and FAN54046) performs an addition battery detection test.

After $V_{BAT}$ rises above $V_{SHORT}$, PWM charging begins (when CE# = 0) with the float voltage ($V_{OREG}$) temporarily set to 4 V. If the battery voltage exceeds 3.7 V within 32 ms of the beginning of PWM charging, the battery is absent. If battery absence is detected:

1. STAT pulses, with FAULT bits set to 111, and the NOBAT bit is set.
2. For FAN54040 only; the $t_{15MIN}$ timer is disabled until $V_{BUS}$ is removed, IDLE state is entered, and POK_B remains HIGH.
3. The IC bypasses the protection switch close test below, since no battery is present.

The FAN54042 and FAN54047 continue to charge.

If $V_{BAT}$ remained below 3.7 V during the initial 32 ms period, Power Path Mode charging continues to ensure that the

battery's discharge protection switch has closed before exiting Power Path Mode:

1. If $V_{BAT}$ is less than 3.4 V, $V_{SYS}$ is set to 4 V, and Power Path charging continues until $V_{BAT}$ has exceeded 3.4 V for at least 128 ms. Charging continues until:
2. $V_{BAT}$ has dropped below 3.2 V for at least 32 ms. Once this occurs, $V_{SYS}$ returns to the OREG register setting (default 3.54 V).
3. $V_{BAT}$ has again risen above $V_{BATMIN}$ for at least 4 ms.

After these three events, PWM Mode is entered and the IC sets the DBAT_B bit. If the host sets the DBAT_B bit (Reg2[1]), events 1 and 2 above are skipped and PWM Mode is entered once $V_{BAT}$ rises above $V_{BATMIN}$.

In a typical application, as soon as the host processor has cleared its UVLO threshold (typically 3.3 V), the host's low level software would set the IBUSLIM and IOCHARGE registers to charge the battery more rapidly above $V_{BATMIN}$ as soon as the host determines that more than 100 mA is available through VBUS *(see Figure 37)*.

Once the host processor begins writing to the IC, charge parameters are set by the host, which must continually reset the $t_{32S}$ timer to continue charging using the programmed charging parameters.

If $t_{32S}$ times out; the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed, and charging continues with default charge parameters in T15MIN Mode for the FAN54040, FAN54042, and FAN54047.

### POK_B (*see Table 8*)

The POK_B pin and bit are intended to provide feedback to the baseband processor that the battery is strong enough to allow the device to fully function. Whenever the IC is operating in Power Path Mode, POK_B is HIGH. On exiting Power Path Mode, POK_B remains HIGH until $V_{BAT} > V_{LOWV}$. Reg1[5:4] sets the $V_{LOWV}$ threshold.

The STAT pin pulses any time the POK_B pin changes.

**Table 8. Q4, Q5, POK_B, and GATE Operation vs. Charging Mode**

| Q4 CC-CV Control | $V_{BUS}$ | $V_{BAT}$ | $V_{SYS}$ | Q4 | Q5 | GATE | POK_B |
|---|---|---|---|---|---|---|---|
| Power Path Mode: Maintain $V_{SYS} \geq 3.4$ V | Valid | $< V_{BATMIN}$ | $\leq 3.4$ | Linear | OFF | HIGH | HIGH |
| Power Path Mode: Limit $I_{CHARGE} \leq 340$ mA | Valid | $< V_{BATMIN}$ | > 3.4 | Linear | OFF | HIGH | HIGH |
| PWM Mode. Q4 Senses Current for $I_{CHARGE}$ | Valid | $> V_{BATMIN}$ and $< V_{LOWV}$ | X | ON | OFF | HIGH | HIGH |
| | | $> V_{LOWV}$ | | | | | LOW |
| OFF | $<V_{BAT}$ | X | X | ON | ON | LOW | HIGH |

**Note:**

10. POK_B remains LOW until Q4 returns to Power Path Mode. Q4 and Q5 are both ON if $V_{SYS} < V_{BAT}$ and CE# = 0. If CE# = 1 and $V_{SYS} < V_{BAT}$, Q5 is OFF and Q4 blocks current flow from VBAT to SYS.

**Table 9. Q4, Q5 Operation as a Function of Relationship between $V_{BUS}$ and $V_{BAT}$**

| PWM | Charger | CE# | $V_{BUS}$ | $V_{BAT}$ | Q4 | Q5 | GATE |
|---|---|---|---|---|---|---|---|
| ON | PWM Mode | 0 | Valid | $< V_{SYS}$, $>V_{BATMIN}$ | ON | OFF | HIGH |
| ON | PWM Mode | 0 | Valid | $> V_{SYS}$, $>V_{BATMIN}$ | ON | ON | LOW |
| ON | Disabled | 1 | Valid | X | OFF | OFF | HIGH |
| ON | Power Path Charging | 0 | Valid | $2\text{ V} < V_{BAT} < V_{BATMIN}$ | Linear | OFF | HIGH |
| OFF | 30 mA Linear Charging | X | Valid | $< 2\ V_{BAT}$ | ON | ON | LOW |
| OFF | OFF | X | X | X | ON | ON | LOW |

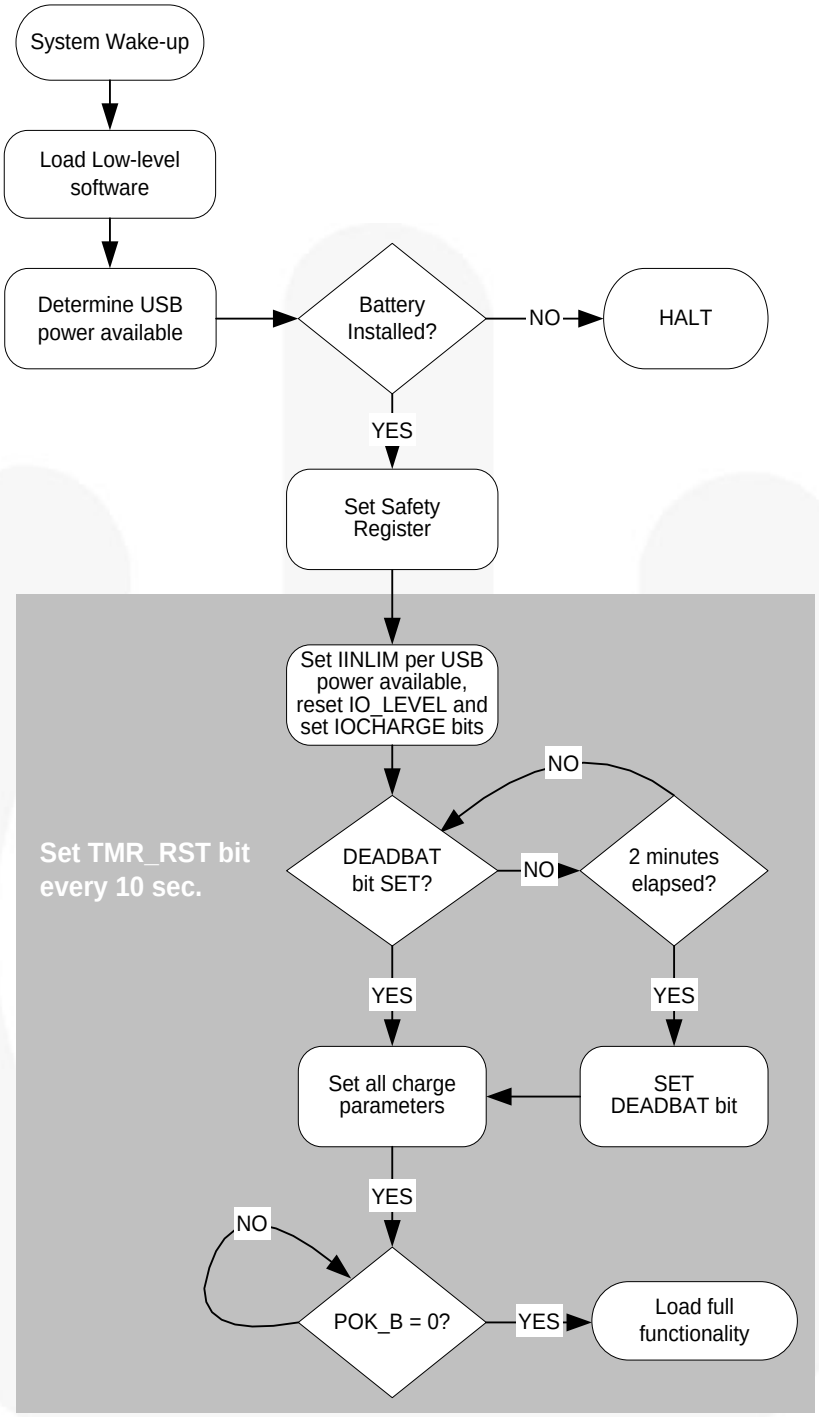



**Figure 37. Recommended Host Software Sequence when Booting with Dead Battery**

## Battery Temperature (NTC) Monitor

The FAN5404X reduces the maximum charge current and termination voltage if an NTC measuring battery temperature ($T_{BAT}$) indicates that it is outside the fast-charging limits (T2 to T3), as described in the JEITA specification[1]. There are four temperature thresholds that change battery charger operation: T1, T2, T3, and T4, shown in Table 10.

### Table 10. Battery Temperature Thresholds

For use with 10 kΩ NTC, β = 3380, and $R_{REF}$ = 10 kΩ.

| Threshold | Temperature | % of $V_{REF}$ |
|---|---|---|
| T1 | 0°C | 73.9 |
| T2 | 10°C | 64.6 |
| T3 | 45°C | 32.9 |
| T4 | 60°C | 23.3 |

### Table 11. Charge Parameters vs. $T_{BAT}$

| $T_{BAT}$ (°C) | $I_{CHARGE}$ | $V_{FLOAT}$ |
|---|---|---|
| Below T1 | Charging to VBAT Disabled | |
| Between T1 and T2 | $I_{OCHARGE}$ / $2^{(11)}$ | 4.0 V |
| Between T2 and T3 | $I_{OCHARGE}$ | $V_{OREG}$ |
| Between T3 and T4 | $I_{OCHARGE}$ / $2^{(11)}$ | 4.0 V |
| Above T4 | Charging to VBAT Disabled | |

**Note:**

11. If $I_{OCHARGE}$ is programmed to less than 650 mA, the charge current is limited to 340 mA.

Thermistors with other β values can be used, with some shift in the corresponding temperature threshold, as shown in Table 12.

### Table 12. Thermistor Temperature Thresholds

$R_{REF}$ = $R_{THRM}$ at 25°C

| Parameter | Various Thermistors | | | |
|---|---|---|---|---|
| $R_{THRM(25°C)}$ | 10 kΩ | 10 kΩ | 47 kΩ | 100 kΩ |
| β | 3380 | 3940 | 4050 | 4250 |
| T1 | 0°C | 3°C | 6 | 8 |
| T2 | 10°C | 12°C | 13 | 14 |
| T3 | 45°C | 42°C | 41 | 40 |
| T4 | 60°C | 55°C | 53 | 51 |

The host processor can disable temperature-driven control of charging parameters by writing 1 to the TEMP_DIS bit. Since TEMP_DIS is reset whenever the IC resets its registers, the temperature controls are enforced whenever the IC is auto-charging, since auto-charge is always preceeded by a reset of registers.

To disable the thermistor circuit, tie the NTC pin to GND. Before enabling the charger, the IC tests to see if NTC is shorted to GND. If NTC is shorted to GND, no thermistor readings occur and the NTC_OK and NTC1-NTC4 is reset.

The IC first measures the NTC immediately prior to entering any PWM charging state, then measures the NTC once per second, updating the result in NTC1-NTC4 bits (Reg 12H[3:0]).

### Table 13. NTC1-NTC4 Decoding

| $T_{BAT}$ (°C) | NTC4 | NTC3 | NTC2 | NTC1 |
|---|---|---|---|---|
| Above T4 | 1 | 1 | 1 | 1 |
| Between T3 and T4 | 0 | 1 | 1 | 1 |
| Between T2 and T3 | 0 | 0 | 1 | 1 |
| Between T1 and T2 | 0 | 0 | 0 | 1 |
| Below T1 | 0 | 0 | 0 | 0 |

[1] Japan Electronics and Information Technology Industries Association (JEITA) and Battery Association of Japan. “A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers,” April 28, 2007.

## Flow Charts

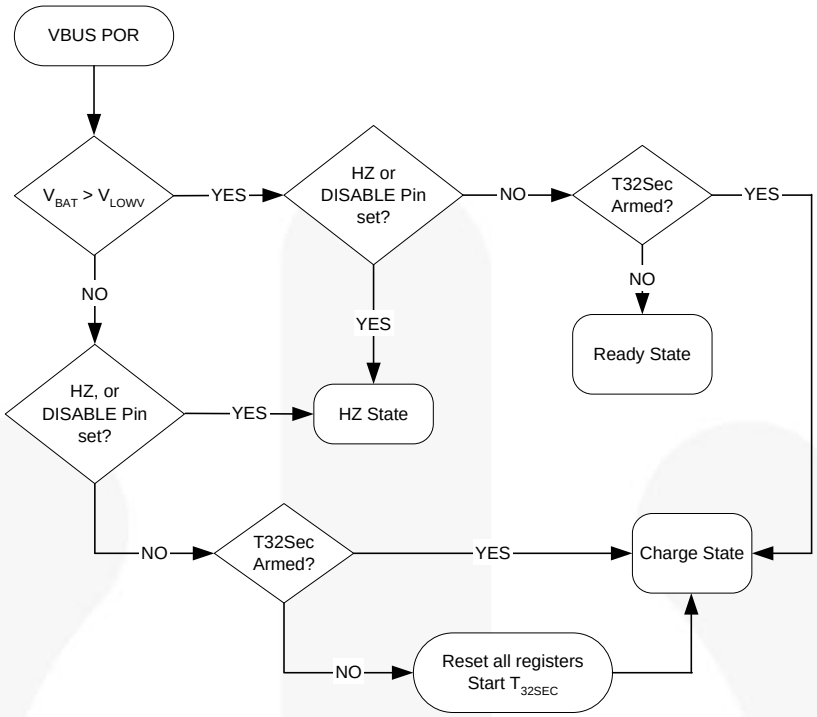



**Figure 38. Charger $V_{BUS}$ POR Flow Chart**

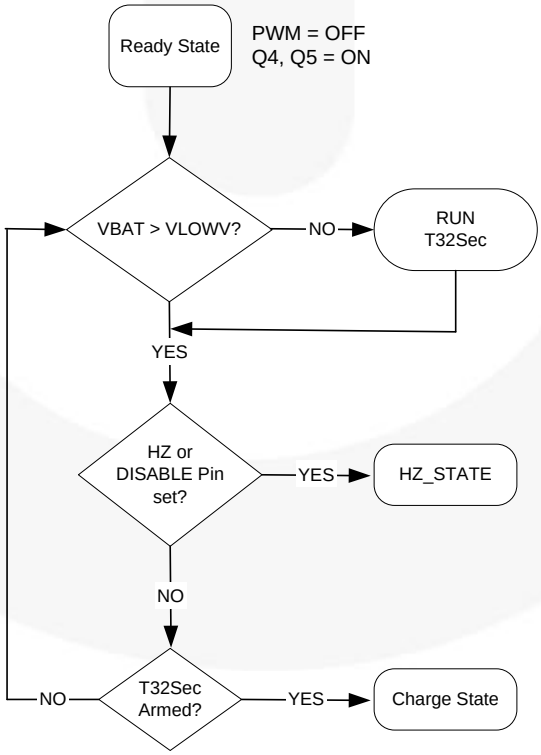



**Figure 39. Ready State Flow Chart**

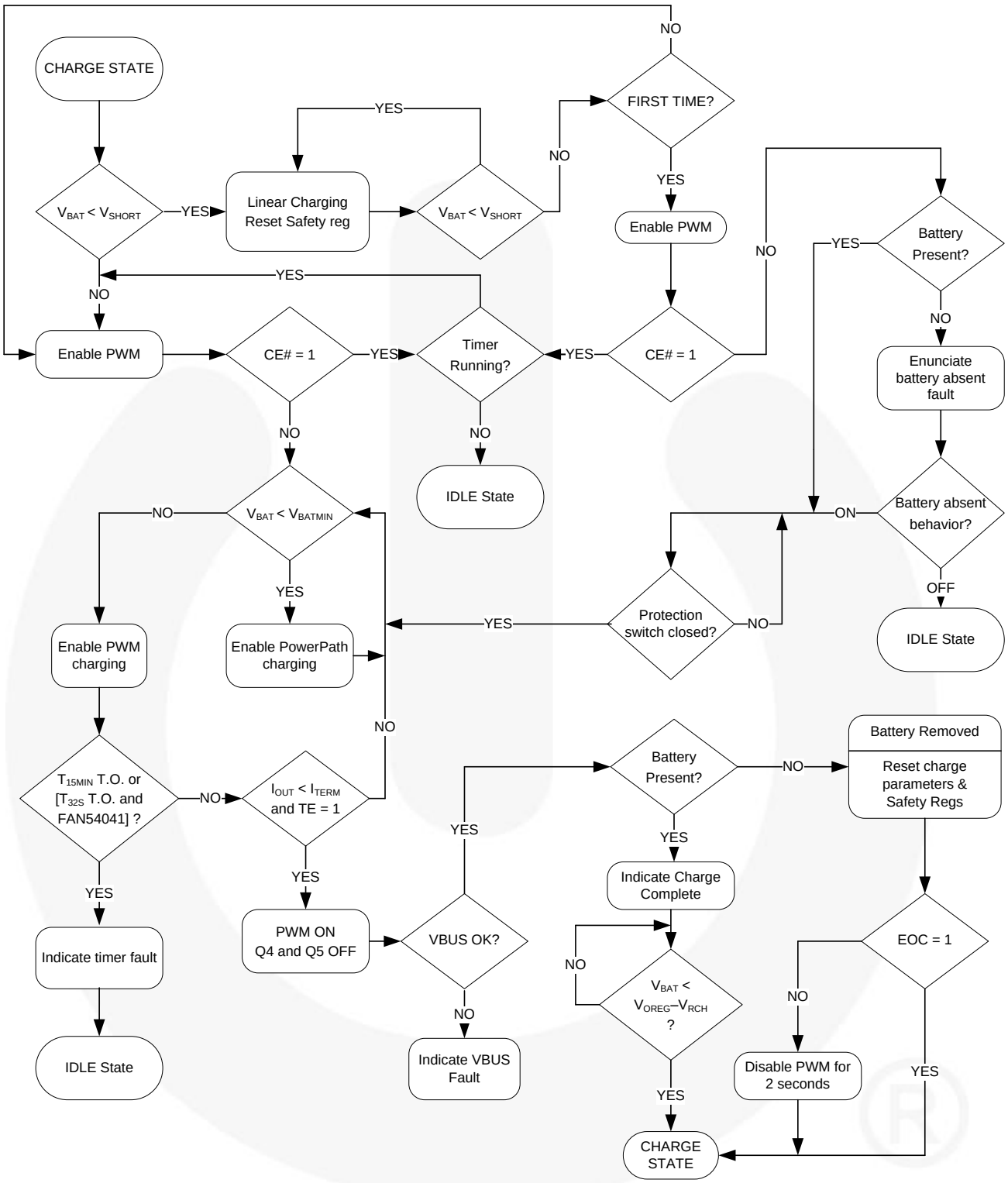



**Figure 40. Charge State Flow Chart**

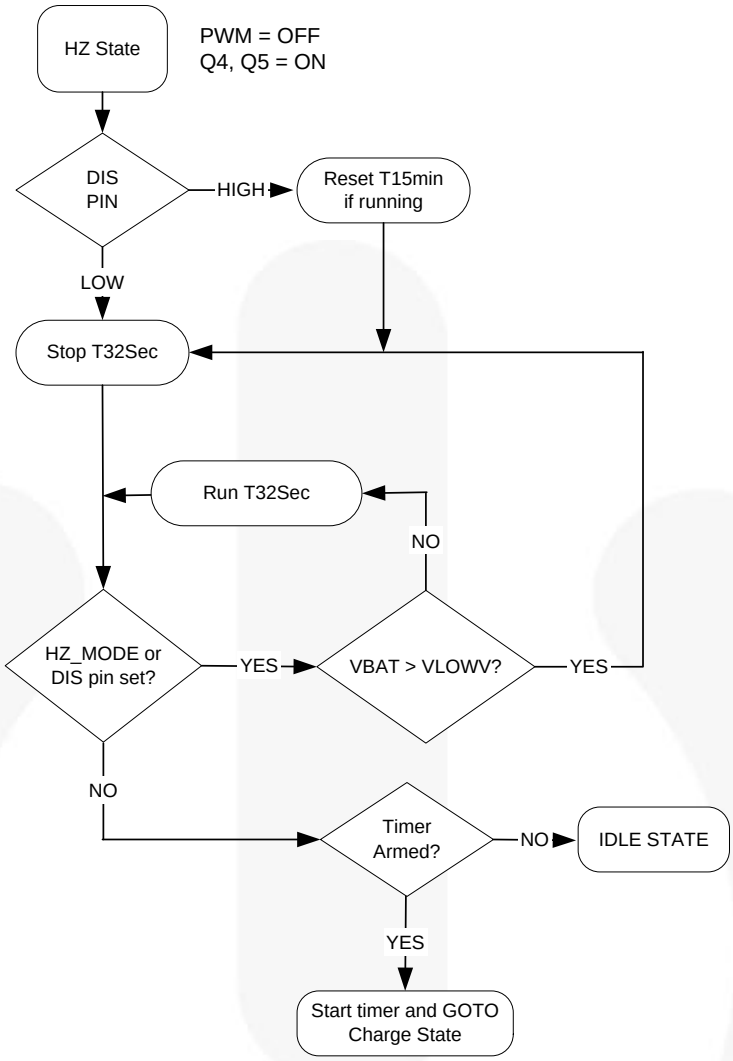



**Figure 41. HZ State**

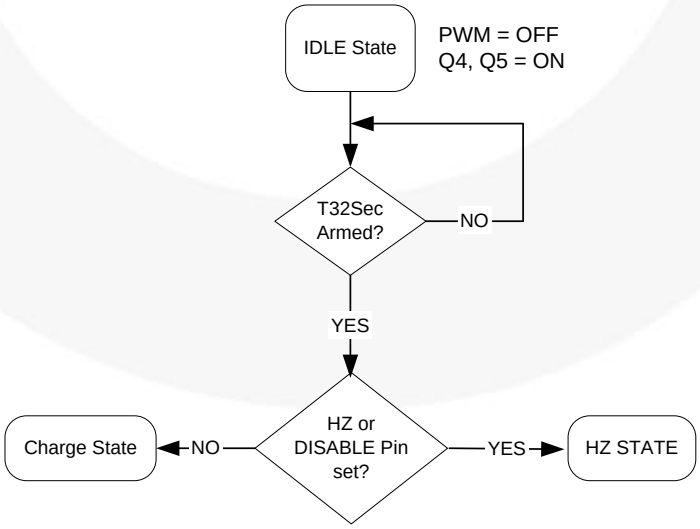



**Figure 42. IDLE State**

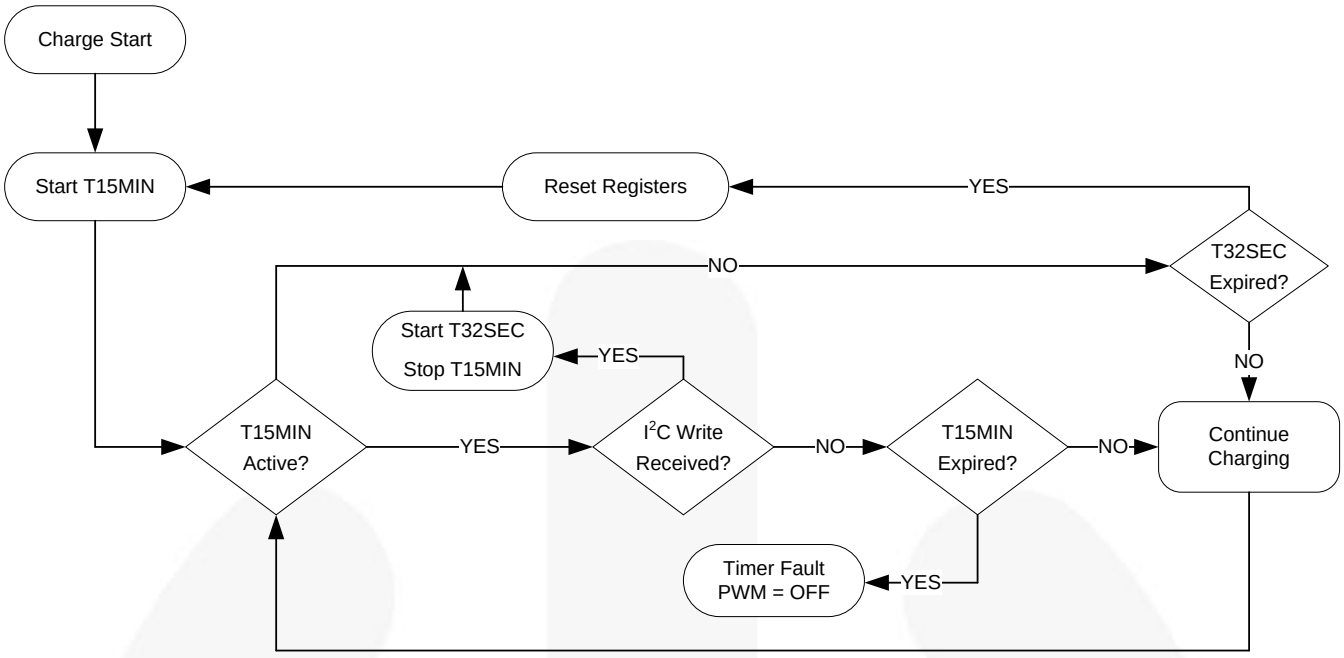



**Figure 43. Timer Flow Chart for FAN54040, FAN54042, FAN54047**

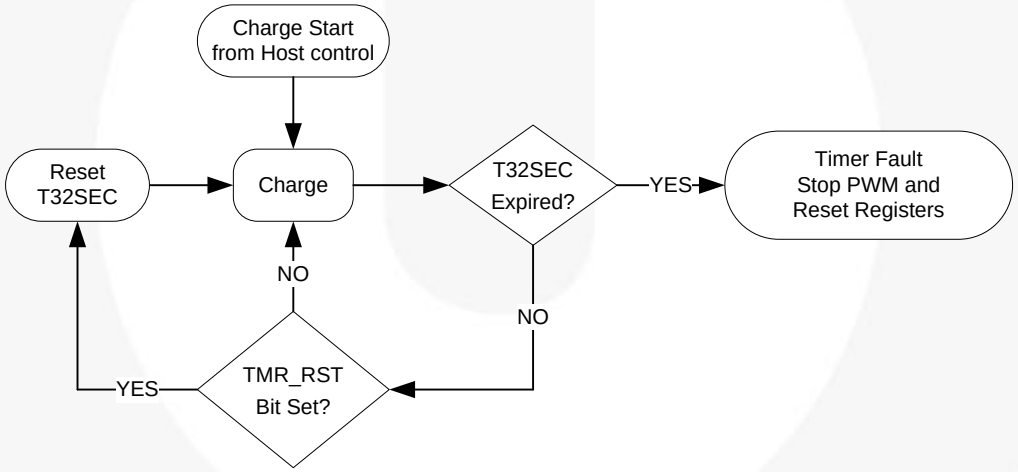



**Figure 44. Timer Flow Chart for FAN54041**

## Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the $I_{BUSLIM}$ bits (REG1[7:6]).

**Table 14. Input Current Limit**

| $I_{BUSLIM}$ REG1[7:6] | Input Current Limit |
|---|---|
| **00** | **100 mA** |
| 01 | 500 mA |
| 10 | 800 mA |
| 11 | No Limit |

For the FAN54041, no charging occurs automatically at VBUS POR, so the input current limit is established by the $I_{BUSLIM}$ bits.

## VBUS Control loop

The IC includes a control loop that limits input current in case a current-limited source is supplying $V_{BUS}$.

The control increases the charging current until either:

- $I_{BUSLIM}$ or $I_{OCHARGE}$ is reached OR
- $V_{BUS}$=$V_{BUSLIM}$.

If $V_{BUS}$ collapses to $V_{BUSLIM}$, the VBUS loop reduces its current to keep $V_{BUS}$=$V_{BUSLIM}$. When the VBUS control loop is limiting the charge current, the VLIM bit (REG5[3]) is set.

**Table 15. $V_{BUS}$ Limit as Function of VBUSLIM Bits (REG5[2:0])**

| $V_{BUSLIM}$ (REG5[2:0]) | | | |
|---|---|---|---|
| **DEC** | **BIN** | **HEX** | **$V_{BUSLIM}$** |
| 0 | 000 | 0 | 4.213 |
| 1 | 001 | 1 | 4.293 |
| 2 | 010 | 2 | 4.373 |
| 3 | 011 | 3 | 4.453 |
| **4** | **100** | **4** | 4.533 |
| 5 | 101 | 5 | 4.613 |
| 6 | 110 | 6 | 4.693 |
| 7 | 111 | 7 | 4.773 |

## Safety Settings

The IC contains a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and IOCHARGE (REG4[7:4]) from exceeding the values of the VSAFE and ISAFE values.

After $V_{BAT}$ rises above $V_{SHORT}$, the SAFETY register is loaded with its default value and may be written to only before writing to any other register. The same 8-bit value should be written to the Safety register twice to set the register value. After writing to any other register, the SAFETY register is locked until $V_{BAT}$ falls below $V_{SHORT}$.

The ISAFE (REG6[7:4]) and VSAFE (REG6[3:0]) registers establish values that limit the maximum values of $I_{OCHARGE}$ and $V_{OREG}$ used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

**Table 16. Maximum $I_{OCHARGE}$ as Function of ISAFE Bits (REG6[7:4])**

| **DEC** | **BIN** | **HEX** | **$I_{OCHARGE(MAX)}$ (mA)** |
|---|---|---|---|
| 0 | 0000 | 0 | 550 |
| 1 | 0001 | 1 | 650 |
| 2 | 0010 | 2 | 750 |
| 3 | 0011 | 3 | 850 |
| **4** | **0100** | **4** | **950** |
| 5 | 0101 | 5 | 1,050 |
| 6 | 0110 | 6 | 1,150 |
| 7 | 0111 | 7 | 1,250 |
| 8 | 1000 | 8 | 1,350 |
| 9 | 1001 | 9 | 1,450 |
| 10-15 | 1010-1111 | A-F | 1,550 |

**Table 17. $V_{SAFE}$ ($V_{OREG}$ Limit) as Function of VSAFE Bits (REG6[3:0])**

| VSAFE (REG6[3:0]) | | | | |
|---|---|---|---|---|
| **DEC** | **BIN** | **HEX** | **OREG Max. (REG2[7:2])** | **VOREG Max.** |
| **0** | **0000** | **0** | **100011** | **4.20** |
| 1 | 0001 | 1 | 100100 | 4.22 |
| 2 | 0010 | 2 | 100101 | 4.24 |
| 3 | 0011 | 3 | 100110 | 4.26 |
| 4 | 0100 | 4 | 100111 | 4.28 |
| 5 | 0101 | 5 | 101000 | 4.30 |
| 6 | 0110 | 6 | 101001 | 4.32 |
| 7 | 0111 | 7 | 101010 | 4.34 |
| 8 | 1000 | 8 | 101011 | 4.36 |
| 9 | 1001 | 9 | 101100 | 4.38 |
| 10 | 1010 | A | 101101 | 4.40 |
| 11 | 1011 | B | 101110 | 4.42 |
| 12-15 | 1100-1111 | C-F | 101111-110010 | 4.44 |

## Thermal Regulation and Protection

When the IC's junction temperature reaches $T_{CF}$ (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Additional $\theta_{JA}$ data points, measured using the FAN54040 evaluation board, are given in Table 18 (measured with $T_A$=25°C). Note that as power dissipation increases, the effective $\theta_{JA}$ decreases due to the larger difference between the die temperature and ambient.

**Table 18. Evaluation Board Measured $\theta_{JA}$**

| **Power (W)** | **$\theta_{JA}$** |
|---|---|
| 0.504 | 54°C/W |
| 0.844 | 50°C/W |
| 1.506 | 46°C/W |

## Charge Mode Input Supply Protection

### Sleep Mode

When $V_{BUS}$ falls below $V_{BAT}$ + $V_{SLP}$ and $V_{BUS}$ is above $V_{IN(MIN)}$, the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

### Input Supply Low-Voltage Detection

The IC continuously monitors $V_{BUS}$ during charging. If $V_{BUS}$ falls below $V_{IN(MIN)}$, the IC:

1. Terminates charging
2. Pulses the STAT pin, sets the STATUS bits to 11, and sets the FAULT bits to 011.

If $V_{BUS}$ recovers above the $V_{IN(MIN)}$ rising threshold after time $t_{INT}$ (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

### Input Over-Voltage Detection

When the $V_{BUS}$ exceeds $VBUS_{OVP}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to 001, sets the STATUS bits to 11, and pulses the STAT pin.

When $V_{BUS}$ falls about 100 mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after $V_{BUS}$ is revalidated *(see VBUS POR / Non-Compliant Charger Rejection)*.

### VBUS Short While Charging

If VBUS is shorted with a very low impedance while the IC is charging with $I_{BUSLIMIT}$=100 mA, the IC may not meet datasheet specifications until power is removed. To trigger this condition, $V_{BUS}$ must be driven from 5 V to GND with a high slew rate. Achieving this slew rate requires a 0 Ω short to the USB cable less than 10 cm from the connector.

### SYS Short During Discharge / Supplemental Mode

Caution should be taken to ensure the SYS pin is not shorted when connected to a battery. This condition can induce high current flow through the BATFET (Q4) until the battery's own safety circuit trips. The resulting high current can damage the IC.

## Charge Mode Battery Detection & Protection

### $V_{BAT}$ Over-Voltage Protection

The OREG voltage regulation loop prevents $V_{BAT}$ from overshooting $V_{OREG}$ by more than 50 mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set and a battery is inserted that is charged to a voltage higher than $V_{OREG}$; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to 100, sets the STATUS bits to 11, and pulses the STAT pin.

### Battery Detection During Charging

The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set and CE# = 0. During normal charging, once $V_{BAT}$ is close to $V_{OREG}$ and the charge current falls below $I_{TERM}$; the PWM charger continues to provide power to SYS and Q4 is turned off. It then turns on a discharge current, $I_{DETECT}$, for $t_{DETECT}$. If $V_{BAT}$ is still above $V_{OREG}$ – $V_{RCH}$, the battery is present and the IC sets the STATUS bits to 10 (Charge Done). If $V_{BAT}$ is below $V_{OREG}$ – $V_{RCH}$, the battery is absent and the IC:

1. Sets the charging parameters to their default values.
2. Sets the FAULT bits to 111 (Battery Absent) and sets the NOBAT bit.
3. If EOC=0, the IC turns off the PWM for $t_{INT}$, then resumes charging. If the battery is still absent, the battery absent fault is then re-enunciated every $t_{INT}$.
4. If EOC = 1, the PWM remains on to provide power to SYS, but charge termination and the battery absent test are performed every $t_{INT}$.

### Linear Charging

If the battery voltage is below the short-circuit threshold ($V_{SHORT}$); a linear current source, $I_{SHORT}$, charges $V_{BAT}$ until $V_{BAT}$ > $V_{SHORT}$.

For $I_{BUSLIM}$ settings of 100 mA or 500 mA, the linear charging current is typically 13 mA. For higher $I_{BUSLIM}$ settings, the linear charging current is increased to 30 mA.

## Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

**Table 19. STAT Pin Function**

| EN_STAT | Charge State | STAT Pin |
|---|---|---|
| 0 | X | OPEN |
| X | Normal Conditions | OPEN |
| 1 | Charging | LOW |
| X | Fault (Charging or Boost) | 128 μs Pulse, then OPEN |

The FAULT bits (R0[2:0]) indicate the type of fault in Charge Mode *(see Table 28).*

## Production Test Mode (PTM)

PTM provides 4.2 V at up to 2.3 A to VBAT when $V_{BUS}$ = 5.5 V ±5%.

The IC enters PTM when the PROD bit is set and the NOBAT bit is HIGH, indicating that the IC has detected battery absence. A battery absence detection test after VBUS POR is performed automatically for FAN54040, FAN54042, and FAN54047 only.

A battery-absent detection test can be performed at any time by setting the TE bit, setting $V_{OREG}$ to at least 4.0 V, then resetting the CE# bit. If no battery is present; charge termination occurs, followed by a battery absent test, which sets the NOBAT bit. Battery-absence detection is completed within 500 ms from the time that CE# is set.

In PTM, GATE is LOW, Q4 and Q5 are on, and all auxiliary control loops are disabled. Only the OREG loop is active, which controls $V_{BAT}$ to 4.2 V, regardless of the OREG register setting. Thermal shutdown remains active.

During PTM, high current pulses (load currents greater than 1.5 A) must be limited to 20% duty cycle with a minimum period of 10 ms.

### Charge Mode Control Bits

Setting either HZ_MODE through $I^2C$ or DIS pin to HIGH disables the charger, puts the IC into High-Impedance Mode, and stops $t_{32S}$. If $V_{BAT} < V_{LOWV}$ while in High-Impedance Mode, $t_{32S}$ begins running and, when it overflows, all registers (except SAFETY) reset, which enables $t_{15MIN}$ charging on versions with the 15-minute timer if DIS=0.

When $t_{15MIN}$ overflows, the IC enters High-Impedance Mode (IDLE). A new charge cycle can only be initiated through $I^2C$ or VBUS POR.

Setting the RESET bit clears all registers. If HZ_MODE bit was set when the RESET bit is set, this bit is also cleared, but the $t_{32S}$ timer is not started and the IC remains in High-Impedance Mode.

**Table 20. DIS Pin and HZ_MODE Bit Functionality**

| Charging | DIS Pin | HZ_MODE |
|---|---|---|
| ENABLE | 0 | 0 |
| DISABLE | X | 1 |
| DISABLE | 1 | X |

Raising the DIS pin stops $t_{32S}$ from advancing, but does not reset it. If the DIS pin is raised during $t_{15MIN}$ charging, the $t_{15MIN}$ timer is reset. CE# determines whether charging to $V_{BAT}$ is enabled or not.

## Boost Mode

Boost Mode can be enabled if the IC is in 32-Second Mode by setting the OPA_MODE bit HIGH and clearing the HZ_MODE bit.

**Table 21. Enabling Boost**

| HZ_MODE | OPA_MODE | BOOST |
|---|---|---|
| 0 | 1 | Enabled |
| 1 | X | Disabled |
| X | 0 | Disabled |

To remain in Boost Mode, the TMR_RST must be set by the host before the $t_{32S}$ timer times out. If $t_{32S}$ times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading R0 clears the fault condition.

## Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate $V_{BUS}$. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant $V_{BAT}$, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 33 and Figure 45.

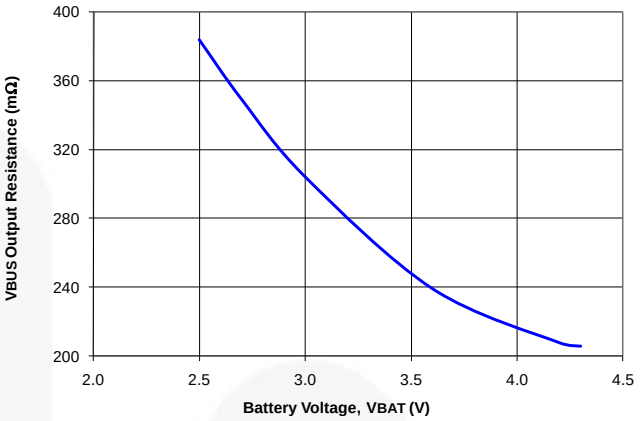



**Figure 45. Output Resistance ($R_{OUT}$)**

$V_{BUS}$ as a function of $I_{LOAD}$ can be computed when the regulator is in PWM Mode (continuous conduction) as:

$$V_{OUT} = 5.07 - R_{OUT} \bullet I_{LOAD} \quad \text{EQ. 1}$$

At $V_{BAT}$=3.0 V and $I_{LOAD}$=300 mA, $V_{BUS}$ drops to:

$$V_{OUT} = 5.07 - 0.30 \bullet 0.3 = 4.98V \quad \text{EQ. 2}$$

At $V_{BAT}$=3.6 V and $I_{LOAD}$=500 mA, $V_{BUS}$ drops to:

$$V_{OUT} = 5.07 - 0.24 \bullet 0.5 = 4.95V \quad \text{EQ. 3}$$

## PFM Mode

If $V_{BUS}$ > $VREF_{BOOST}$ (nominally 5.07 V) when the minimum off-time ends, the regulator enters PFM Mode. Boost pulses are inhibited until $V_{BUS}$ < $VREF_{BOOST}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

**Table 22. Boost PWM Operating States**

| Mode | Description | Invoked When |
|---|---|---|
| LIN | Linear Startup | $V_{BAT} > V_{BUS}$ |
| SS | Boost Soft-Start | $V_{BUS} < V_{BST}$ |
| BST | Boost Operating Mode | $V_{BAT} > UVLO_{BST}$ and SS Completed |

## Startup

When the boost regulator is shut down, current flow is prevented from $V_{BAT}$ to $V_{BUS}$, as well as reverse flow from $V_{BUS}$ to $V_{BAT}$.

### LIN State

When EN rises, if $V_{BAT}$ > $UVLO_{BST}$; the regulator first attempts to bring PMID within 400 mV of $V_{BAT}$ using an internal 450 mA current source from VBAT (LIN State). If PMID has not achieved $V_{BAT}$ – 400 mV after 560 μs, a FAULT state is initiated.

### SS State

When PMID > $V_{BAT}$ – 400 mV, the boost regulator begins switching with a reduced peak current limit of about 50% of its normal current limit. The output slews up until $V_{BUS}$ is within 5% of its setpoint; at which time, the regulation loop is closed and the current limit is set to 100%.

If the output fails to achieve 95% of its setpoint ($V_{BST}$) within 128 μs, the current limit is increased to 100%. If the output fails to achieve 95% of its setpoint after this second 384 μs period, a fault state is initiated.

### BST State

This is the normal operating mode of the regulator. The regulator uses a minimum $t_{OFF}$-minimum $t_{ON}$ modulation scheme. The minimum $t_{OFF}$ is proportional to $\frac{V_{IN}}{V_{OUT}}$, which keeps the regulator's switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to $V_{BAT}$ and is a higher value if the inductor current reached 0 before $t_{OFF(MIN)}$ in the prior cycle.

To ensure $V_{BUS}$ does not overshoot the regulation point, the boost switch remains off as long as $V_{FB}$ > $V_{REF(BST)}$.

### Boost Faults

If a BOOST fault occurs:

1. The STAT pin pulses.
2. OPA_MODE bit is reset.
3. The power stage is in High-Impedance Mode.
4. The FAULT bits (REG0[2:0]) are set per Table 23.

### Restart After Boost Faults

OPA_MODE is reset on boost faults. Boost Mode can only be re-enabled by setting the OPA_MODE bit.

**Table 23. Fault Bits During Boost Mode**

| Fault Bit | | | Fault Description |
|---|---|---|---|
| B2 | B1 | B0 | |
| 0 | 0 | 0 | Normal (no fault) |
| 0 | 0 | 1 | $V_{BUS}$ > $VBUS_{OVP}$ |
| 0 | 1 | 0 | $V_{BUS}$ fails to achieve the voltage required to advance to the next state during soft-start or sustained (>50 μs) current limit during the BST state. |
| 0 | 1 | 1 | $V_{BAT}$ < $UVLO_{BST}$ |
| 1 | 0 | 0 | NA: This code does not appear. |
| 1 | 0 | 1 | Thermal shutdown |
| 1 | 1 | 0 | Timer fault; all registers reset. |
| 1 | 1 | 1 | NA: This code does not appear. |

## Monitor Registers (Reg10H, Reg11H)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High-Impedance Mode is valid only when $V_{BUS}$ is valid.

## $I^2C$ Interface

The FAN5404X's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode $I^2C$ bus specifications. The FAN5404X SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

### Slave Address

**Table 24. $I^2C$ Slave Address Byte**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | R/$\overline{W}$ |

In hex notation, the slave address assumes a 0 LSB. The hex slave address is D6H for all parts in the family. Other slave addresses can be accommodated upon request. *Contact a Fairchild Semiconductor representative.*

### Bus Timing

As shown in Figure 46, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

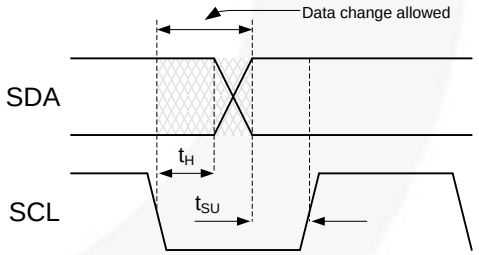



**Figure 46. Data Transfer Timing**

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 47

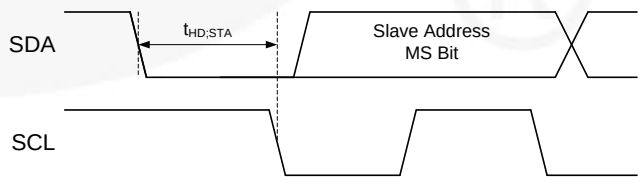



**Figure 47. Start Bit**

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 48.

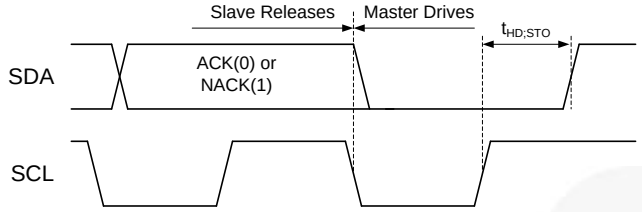



**Figure 48. Stop Bit**

During a read from the FAN5404X (Figure 51), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 49.

## High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1 MHz clock); slaves do not ACK the transmission.

The master then generates a repeated start condition (Figure 49) that causes all slaves on the bus to switch to HS Mode. The master then sends $I^2C$ packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 48) is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 49).

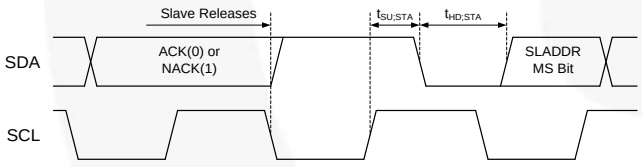



**Figure 49. Repeated Start Timing**

## Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

**Table 25. Bit Definitions for Figure 50 - Figure 53**

| Symbol | Definition |
|---|---|
| S | START, *see Figure 47* |
| A | ACK. The slave drives SDA to 0 to acknowledge the preceding packet. |
| $\overline{A}$ | NACK. The slave sends a 1 to NACK the preceding packet. |
| R | Repeated START, *see Figure 49* |
| P | STOP, *see Figure 48* |

## Multi-Byte (Sequential) Read and Write Transactions

### Sequential Write (Figure 52)

The Slave Address, Reg Addr address, and the first data byte are transmitted to the FAN5404x in the same way as in a byte write (Figure 50). However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte written and its ACK bit received, the master issues a STOP bit. The IC contains an 8-bit counter that increments the address pointer after each byte is written.

### Sequential Read (Figure 53)

Sequential reads are initiated in the same way as a single-byte read (Figure 51), except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave's $I^2C$ logic to transmit the next sequentially addressed 8-bit word. The FAN5404x contains an 8-bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one $I^2C$ transaction.

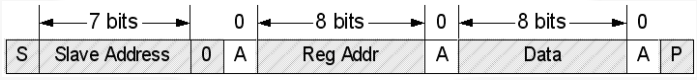



**Figure 50. Single-Byte Write Transaction**

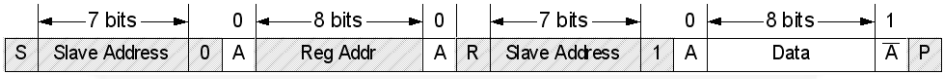



**Figure 51. Single-Byte Read Transaction**

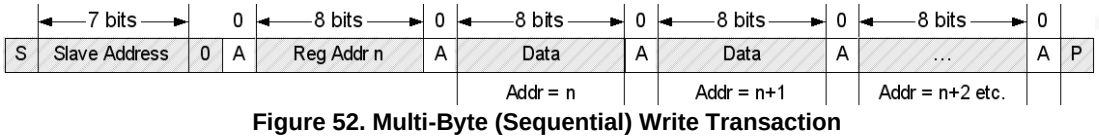



**Figure 52. Multi-Byte (Sequential) Write Transaction**

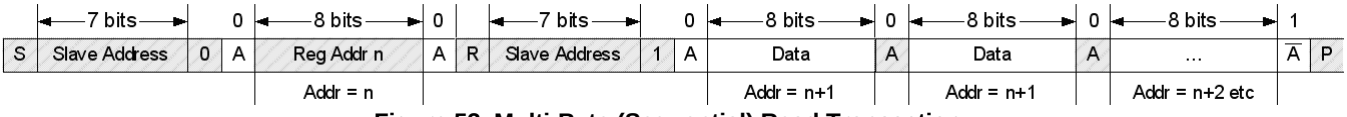



**Figure 53. Multi-Byte (Sequential) Read Transaction**

## Register Descriptions

The eight user-accessible IC registers are defined in Table 26.

**Table 26. I²C Register Address**

| Register | | Address Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **REG#** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| CONTROL0 | 0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CONTROL1 | 1H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| OREG | 2H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| IC_INFO | 3H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| IBAT | 4H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| VBUS_CONTROL | 5H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| SAFETY | 6H | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| POST_CHARGING | 7H | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| MONITOR0 | 10H | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| MONITOR1 | 11H | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| NTC | 12H | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| WD_CONTROL | 13H | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

**Table 27. Register Bit Definitions**

This table defines the operation of each register bit for all IC versions. Default values are in **bold** text.

| Bit | Name | Value | Type | Description |
|---|---|---|---|---|
| **CONTROL0** | | | | **Register Address: 00** **Default Value=0100 0000** |
| 7 | TMR_RST | **0** | W | Writing a 1 resets the $t_{32S}$ timer; writing a 0 has no effect.<br>Reading this bit always returns 0 |
| 6 | EN_STAT | 0 | R/W | Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults |
| | | **1** | | Enables STAT pin to be LOW when IC is charging |
| 5:4 | STAT | **00** | R | Ready |
| | | 01 | | PWM Enabled. Charging is occurring if CE# = 0. |
| | | 10 | | Charge done |
| | | 11 | | Fault |
| 3 | BOOST | **0** | R | IC is not in Boost Mode |
| | | 1 | | IC is in Boost Mode |
| 2:0 | FAULT | | R | **Table 28. Charger Mode Faults** |

| Fault Bit | | | Fault Description |
|---|---|---|---|
| **2** | **1** | **0** | |
| 0 | 0 | 0 | Normal (No Fault) |
| 0 | 0 | 1 | VBUS OVP |
| 0 | 1 | 0 | Sleep Mode |
| 0 | 1 | 1 | Poor Input Source |
| 1 | 0 | 0 | Battery OVP |
| 1 | 0 | 1 | Thermal Shutdown |
| 1 | 1 | 0 | Timer Fault |
| 1 | 1 | 1 | No Battery |

*For Boost Mode faults, see Table 23*

| Bit | Name | Value | Type | Description |
|---|---|---|---|---|
| **CONTROL1** | | | | **Register Address: 01** **Default Value=0011 0X00** |
| 7:6 | $I_{BUSLIM}$ | | R/W | Input current limit; **defaults to 00 (100 mA)**, *see Table 14* |
| 5:4 | $V_{LOWV}$ | 00 | R/W | 3.4 V — Weak battery voltage threshold |
| | | 01 | | 3.5 V |
| | | 10 | | 3.6 V |
| | | **11** | | **3.7 V** |
| 3 | TE | **0** | **R/W** | **Disable charge current termination** |
| | | 1 | | Enable charge current termination |
| 2 | CE# | 0 | R/W | Charging enabled. **Default for FAN54040, FAN54042, FAN54047.** |
| | | 1 | | Charging disabled. **Default for FAN54041, FAN54045 , FAN54046.** |
| 1 | HZ_MODE | **0** | **R/W** | **Not High-Impedance Mode** — *See Table 21* |
| | | 1 | | High-Impedance Mode |
| 0 | OPA_MODE | **0** | **R/W** | **Charge Mode** |
| | | 1 | | Boost Mode |
| **OREG** | | | | **Register Address: 02** **Default Value=0000 1000 (08H)** |
| 7:2 | OREG | | R/W | Charger output “float” voltage; programmable from 3.5 to 4.44 V in 20 mV increments; **defaults to 000010 (3.54 V)**, *see Table 4.* |
| 1 | DBAT_B | **0** | R/W | Indicates that the IC detected a dead battery after VBUS_POR and that the charger has not yet completed the three steps to ensure that the battery’s protection switch is closed if a battery is present, as described in the Dead Battery section on page 21. Writing a 0 to this bit is ignored. |
| | | 1 | | The IC sets this bit to 1 if any of the following are true:<br>1. Dead Battery ($V_{BAT} < V_{SHORT}$) was not detected at VBUS_POR.<br>2. The IC has completed the three steps to ensure that if the battery is present, the battery’s protection switch has closed, as described in the Dead Battery section on page 21.<br>If the host sets this bit while the IC is charging the battery and DBAT_B is LOW, the three steps are aborted and normal Power Path or PWM charging proceeds. |
| 0 | EOC | **0** | R/W | If no battery is detected when a full battery (end of charge) is reached, PWM stops, Q4 and Q5 remain on, and the charger automatically restarts after two seconds with TE and CE# bits unchanged. |
| | | 1 | | If no battery is detected when a full battery (end of charge) is reached, the PWM charger stays on, allowing the host processor to continue to run with no battery. |
| **IC_INFO** | | | | **Register Address: 03** **Default Value=100X XXXX** |
| 7:6 | Vendor Code | **10** | R | Identifies Fairchild Semiconductor as the IC supplier |
| 5:3 | PN | | R | Part number bits, *see the Ordering Info on page 2* |
| 2:0 | REV | | R | IC Revision, revision 1.X, where X is the decimal of these three bits |
| **IBAT** | | | | **Register Address: 04** **Default Value=1000 0001 (81H)** |
| 7 | RESET | 1 | W | Writing a 1 resets all registers, except the Safety register (Reg6), to their defaults: writing a 0 has no effect; read returns 1 |
| 6:3 | IOCHARGE | Table 5 | R/W | Programs the maximum charge current, *see Table 5* |
| 2:0 | ITERM | Table 6 | R/W | Sets the current used for charging termination, *see Table 6* |

| Bit | Name | Value | Type | Description |
|---|---|---|---|---|
| **VBUS_CONTROL** | | | | **Register Address: 05** **Default Value=001X X100** |
| 7 | Reserved | **0** | R | This bit always returns 0 |
| 6 | PROD | **0** | R/W | Charger operates in Normal Mode. |
| | | 1 | | Charger operates in Production Test Mode. |
| 5 | IO_LEVEL | 0 | R/W | Battery current is controlled by IOCHARGE bits. |
| | | **1** | | Battery current control is set to 340 mA. |
| 4 | VBUS_CON | | R | 1 Indicates that $V_{BUS}$ is above 4.4 V (rising) or 3.8 V (falling). When VBUS_CON changes from 0 to 1, a STAT pulse occurs. |
| 3 | SP | 0 | R | VBUS control loop is not active ($V_{BUS}$ is able to stay above $V_{BUSLIM}$) |
| | | 1 | | VBUS control loop is active and $V_{BUS}$ is being regulated to $V_{BUSLIM}$ |
| 2:0 | VBUSLIM | Table 15 | R/W | VBUS control voltage reference, *see Table 15* |
| **SAFETY** | | | | **Register Address: 06** **Default Value=0100 0000 (40H)** |
| 7:4 | ISAFE | Table 16 | R/W | Sets the maximum $I_{OCHARGE}$ value used by the control circuit, *see Table 16* |
| 3:0 | VSAFE | Table 17 | R/W | Sets the maximum $V_{OREG}$ used by the control circuit, *see Table* 17 |
| **POST_CHARGING** | | | | **Register Address: 07** **Default Value=0000 0001 (01H)** |
| 7:6 | BDET | | R/W | These bits determine whether a battery absent detection will be performed when the NTC reading indicates out-of-range when charging.<br>**[7:6] — When NTC goes out-of-range**<br>**00 — Always do battery absent detection**<br>01 — Disable detection in Normal Mode<br>10 — Disable detection when Reg FA = B5 (PWM running after charge done.<br>11 — NTC out-of-range in charge done does not cause battery absent detection. |
| 5:4 | VBUS_LOAD | 0 | R/W | After charger termination, in the charge done state, these bits control VBUS loading to improve detection of AC power removal from the AC adapter.<br>**[5:4] — VBUS loading in Charge Done State:**<br>**00 — None**<br>01 — Load VBUS for 4 ms every two seconds<br>10 — Load VBUS for 131 ms every two seconds<br>11 — Load VBUS for 135 ms every two seconds |
| 3 | PC_EN | **0** | R/W | Post charging or background charging feature is disabled |
| | | 1 | | Post charging or background charging feature is enabled |
| 2:0 | PC_IT | Table 6 | R/W | Sets the termination current for post or underground charging, *see Table 6* |
| **MONITOR0** | | | | **Register Address: 10H (16)** **Default Value=XXX0 XXXX (XXH)** |
| 7 | ITERM_CMP | | R | ITERM comparator output, 1 when $I_{CHARGE} > I_{TER}M$ reference |
| 6 | VBAT_CMP | | R | Output of VBAT comparator, 1 when $V_{BAT} < V_{BUS}$ |
| 5 | LINCHG | | R | 1 when 30 mA linear charger ON ($V_{BAT} < V_{SHORT}$) |
| 4 | T_120 | | R | Thermal regulation comparator, 1 when the die temperature is greater than 120°C. During this condition, charge current is limited to 340 mA. |
| 3 | ICHG | | R | 0 indicates the ICHARGE loop is controlling the battery charge current. |
| 2 | IBUS | | R | 0 indicates the IBUS (input current) loop is controlling the battery charge current. |
| 1 | VBUS_VALID | | R | 1 indicates $V_{BUS}$ has passed validation and is capable of charging. |
| 0 | CV | | R | 1 indicates the constant-voltage loop (OREG) is controlling the charger and all current limiting loops have released. |

| Bit | Name | Value | Type | Description |
|---|---|---|---|---|
| **MONITOR1** | | | | **Register Address: 11H (17)** **Default Value=XX1X XXXX** |
| 7 | GATE | 0 | R | GATE pin is LOW, Q5 is driven on. |
| | | 1 | | GATE pin is HIGH, Q5 is off. |
| 6 | VBAT | 0 | R | $V_{BAT} < V_{BATMIN}$ in PP charging, $V_{BAT} < V_{LOW}$ in PWM charging |
| | | 1 | | $V_{BAT} > V_{BATMIN}$ in PP charging, $V_{BAT} > V_{LOW}$ in PWM charging |
| 5 | POK_B | 0 | R/W | POK_B Pin is LOW. |
| | | **1** | | POK_B Pin is HIGH. Writing to this bit sets the POK_B pin. |
| 4 | DIS_LEVEL | 0 | R | DIS pin is LOW. |
| | | 1 | | DIS pin is HIGH. |
| 3 | NOBAT | 1 | R | Battery absence |
| | | 0 | | Battery presence |
| 2 | PC_ON | 1 | R | Post charging (background charging) is under progress. |
| | | 0 | | Post charging (background charging) is not under progress. |
| 1:0 | Reserved | 0 | R | These bits always return 0. |
| **NTC** | | | | **Register Address: 12H (18)** **Default Value=000X XXXX** |
| 7:6 | Reserved | 00 | R | These bits always return 0. |
| 5 | TEMP_DIS | **0** | **R/W** | NTC Temperature measurement results affect charge parameters. |
| | | 1 | | NTC Temperature measurement results do not affect charge. Temperature measurements continue to be updated every second in the NTC1-4 monitor bits. |
| 4 | NTC_OK | | R | 0 if NTC is either shorted to GND, open, or shorted to REF. |
| 3 | NTC4 | | R | 1 indicates that NTC is above the T4 threshold. |
| 2 | NTC3 | | R | 1 indicates that NTC is above the T3 threshold. |
| 1 | NTC2 | | R | 1 indicates that NTC is above the T2 threshold. |
| 0 | NTC1 | | R | 1 indicates that NTC is above the T1 threshold. |
| **WD_CONTROL** | | | | **Register Address: 13H (19)** **Default Value = 0110 1100** |
| 7 | Reserved | **0** | R/W | These bits do not change the function of the IC. |
| 6:5 | Reserved | **11** | R/W | These bits do not change the function of the IC. |
| 4 | Reserved | **0** | R/W | These bits do not change the function of the IC. |
| 3 | Reserved | **1** | R/W | These bits do not change the function of the IC. |
| 2 | EN_VREG | 0 | **R/W** | VREG is off |
| | | **1** | | **VREG is on** |
| 1 | WD_DIS | **0** | **R/W** | **Watchdog timer (T32S) operation normal** |
| | | 1 | | Watchdog timer (T32S) disabled. |
| 0 | Reserved | 0 | R | This bit always returns 0 |
| **RESTART** | | | | **Register Address: FAH (250)** **Default Value = 1111 1111** |
| 7:0 | RESTART | | W | Writing B5H restarts charging when the IC is in the charge done state. This register reads back FF. |

*See Table 10 – Table 13*

## PCB Layout Recommendation

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. Power and ground pins should be routed directly to their bypass capacitors using the top copper layer. The copper area connecting to the IC should be maximized to improve thermal performance. See the layout recommendations in Figure 54.

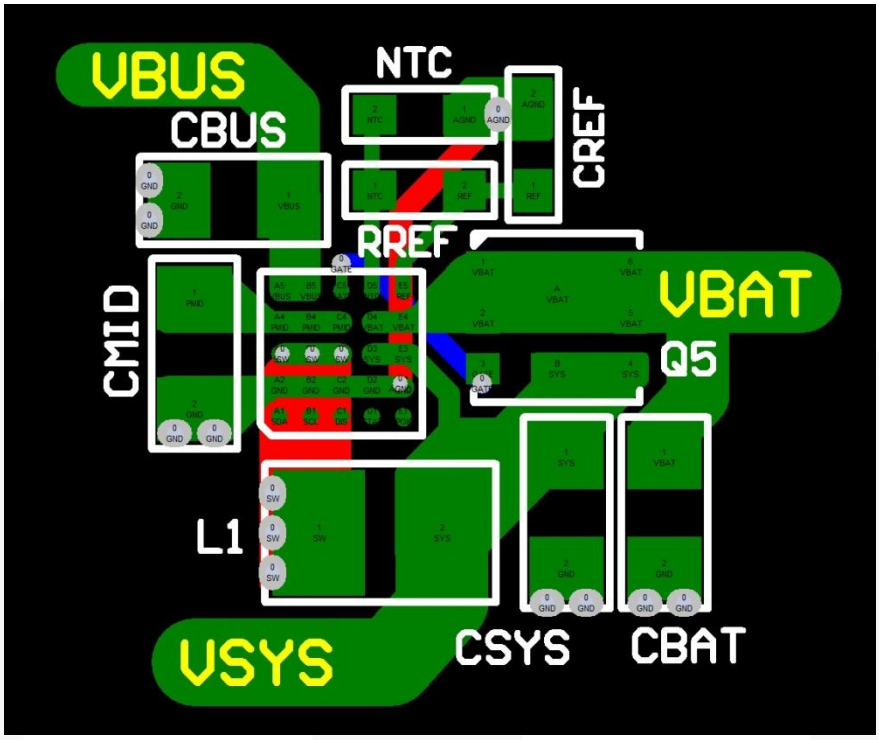
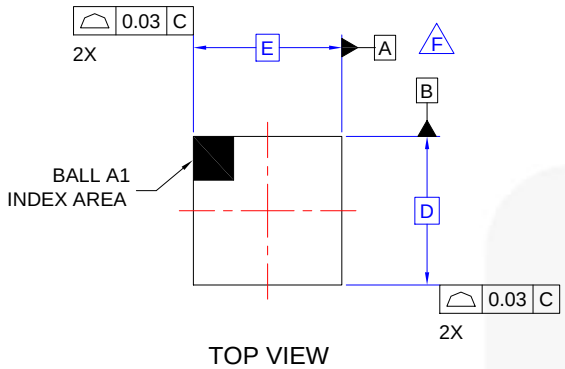
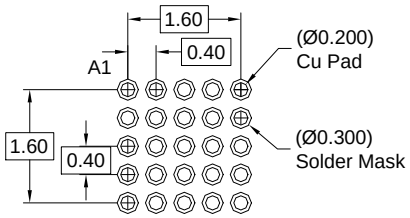



**Figure 54. PCB Layout Recommendation**

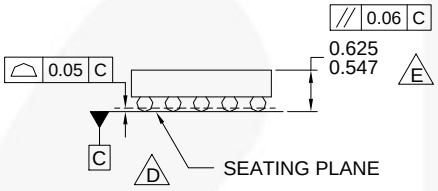
## Physical Dimensions

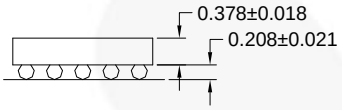



TOP VIEW

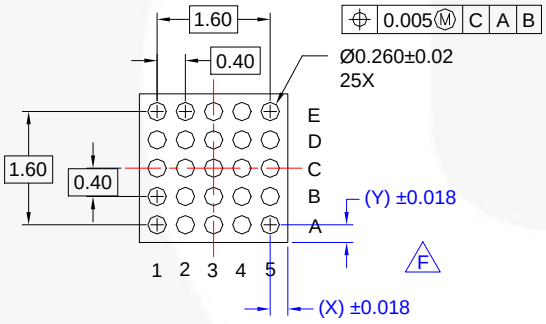



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)




SIDE VIEWS




BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE TABLE BELOW.

G. DRAWING FILNAME: MKT-UC025AArev2.

**Figure 55. 25-Ball WLCSP, 5X5 Array, 0.4 mm Pitch, 250 µm Ball**

## Product-Specific Dimensions

| Product | D | E | X | Y |
|---|---|---|---|---|
| FAN5404XUCX | 2.40 ±0.030 | 2.00 ±0.030 | 0.180 | 0.380 |

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