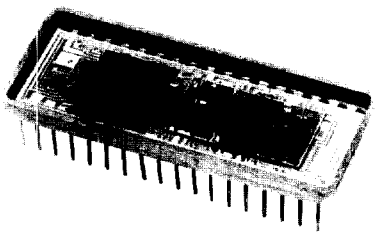
NATEL

HDSC2036

Two-Channel, Double-Buffered Four-Quadrant Multiplying SIN/COS DAC Microprocessor Compatible 16-bit Hybrid

Features

- **Single 36-pin hybrid DDIP package**
- **Two independent channels**
- **1 arc-minute accuracy**
- **0.03% radius accuracy**
- **Microprocessor compatible** (8 and 16-bit)
- **Double buffered inputs**
- **Pin-programmable gains** (0.5, 1.0, 2.0)
- **Buffered reference inputs**
- **Requires only ± 15-V power supplies**
- **TTL and CMOS compatible**
- **MIL-STD-883 Processing is Available**
- **Priced at $445/USA single unit price** (HDSC2036-14S)



ACTUAL SIZE

Applications

Two-speed digital-to-synchro converters
Coordinate conversion circuits
Resolver computing circuits
Axis rotation
Vector resolution
Radar and navigational systems
Flight instrumentation

Description

The HDSC2036 is the world's first 2-channel 16-bit digital-to-sin/cos converter that is available in a single 36-pin DDIP package. Rather than an extraordinary packaging feat, the converter was made possible by technological advances in Natel-designed LSI chips for the function. In fact, in spite of performing twice the functions of any converter available in this size, the design uses a single-layer conductor substrate. This not only provides the higher reliability, but also higher yields and productivity.

Offering both 8 and 16-bit microprocessor compatibility, the two independent channels of the Model 2036 accept a 16-bit (CMOS/TTL) digital input from a common 8- or 16-bit data bus. Each channel has its own double-buffered inputs and independent conversion circuitry. The analog inputs are buffered through operational amplifiers to minimize loading of the input signals. For each channel the digital input is multiplied by the analog voltage to generate the trigonometric functions $V_{IN} \bullet \sin\theta$ and $V_{IN} \bullet \cos\theta$. V_{IN} is the analog input voltage and θ is the digital input angle. The analog input voltage can be an ac or dc reference with an amplitude of ± 10V peak. The package actually contains two independent channels of Natel Model 2026 — the most advanced 4-quadrant multiplying digital-to-sin/cos converter available.

Along with a 50% P.C. board space saving, angular accuracy of up to 1 arc-minute and radius accuracy of 0.03% make the HDSC2036 an ideal choice for applications requiring multiple-channels, small size and true sine and cosine outputs. Resolver computing chains and coordinate conversion circuits are some examples of such multichannel applications.

The HDSC2036 converter does not require a +5-V logic supply. The digital inputs are TTL and 5-V CMOS compatible. Internally derived logic thresholds are 0.8 V-dc for a logic "low" and 2.4 V-dc for a logic "high."

All data bits (B1 through B16) are actively pulled down to ground. If the converter requires less than 16-bit resolution, the unused data bit pins may be left unconnected. Control Signals LBE, HBE and LDC for both channels are actively pulled-up to logic "high." When not required by your application, these pins may also be left open.

Model HDSC2036 converters are available with angular accuracies of 1, 2 and 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits.

Theory of Operation

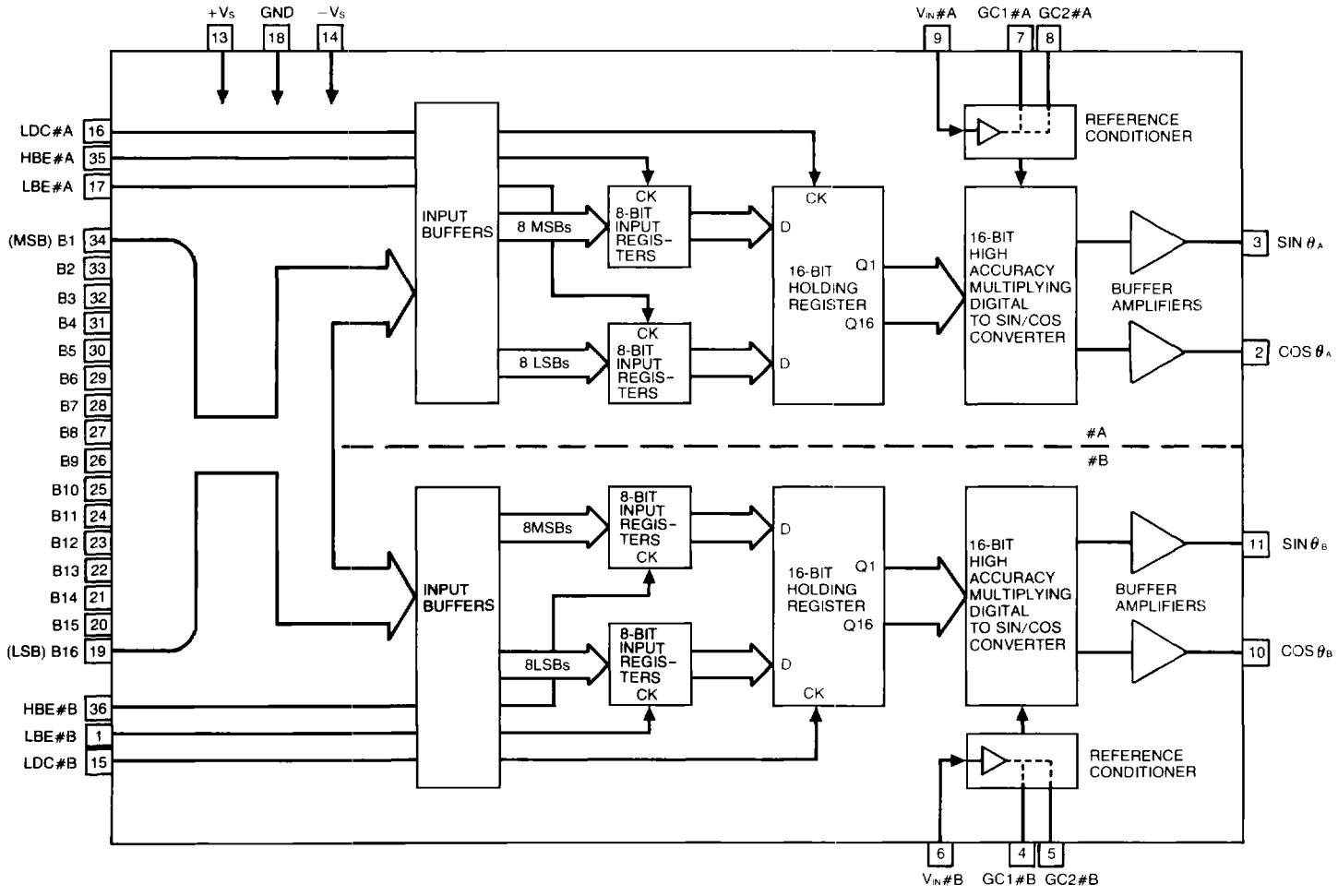


FIGURE 1 2036 BLOCK DIAGRAM

The operation of the Model 2036 is illustrated in the functional diagram of Figure 1. Except for 16-bit digital angle data pins, the two channels of digital-to-sine/cosine converter are completely independent. The two independent channels load data to the converter from a common 8- or 16-bit data bus. The description below explains the theory of operation for one channel of a digital-to-sine/cosine converter.

The reference voltage is buffered through an operational amplifier in the reference conditioner. In addition the reference conditioner allows the user to program the gain of the converter by appropriate pin connections (see Gain Programming). The digital word representing the input angle is applied to input buffers. Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus each input register can be independently enabled to accept the 16-bit word in two 8-bit bytes. When inter facing with 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word. The 16-bit data word is then parallel-loaded into a holding register and processed through a Multiplying Digital-to-Sin/Cos converter.

The multiplying digital-to-sin/cos converter is made up of two function generators (sin θ and cos θ) and quadrant select network. The digital input code is natural binary angle. The two most significant bits (Bit 1 = 180°, Bit 2 = 90°) determine the quadrant information. Bits 3 through 16, containing angular information together with buffered reference voltage, are applied to two function generators. The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the 2036 uses resistive ladder networks and solid state switching to control the attenuation of the reference voltage. The ladder networks, however, are designed to attenuate the input reference proportional to the sine and cosine of the digital input angle. A unique approach is used in the design of ladder networks to obtain high accuracy in the sine and cosine generation so that they can be used as independently accurate functions. The outputs of function generators are then applied to a quadrant select network to obtain true sin θ and cos θ outputs.

Specifications

PARAMETER	VALUE	REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)	MSB = 180° LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minutes (option V)	Accuracy applies over operating temp. range
Analog Input (V_{IN})	0 to ±10 V peak ac or dc	Independent for each channel
Frequency Range	dc to 1000 Hz (option 4) dc to 10 kHz (option 5)	
Input Impedance	5 MΩ minimum	Operational amplifier Buffer
Analog Outputs	$K \cdot V_{IN} \cdot \sin\theta$ and $K \cdot V_{IN} \cdot \cos\theta$	± 10 V peak ac or dc
Converter Gain (K)	0.5 ± 0.05% 1.0 ± 0.05% 2.0 ± 0.05%	SEE TEXT FOR CONNECTIONS
Radius accuracy	± 0.03%	Simultaneous amplitude variation in both outputs as a function of digital angle
Output current	2 mA-rms	Short circuit proof
Output impedance	< 1 ohm	Operational amplifier output
Zero offset (dc)	± 10 mV typical, ± 25 mV maximum	
Offset drift	25 μV/°C	
Output Settling time	20 μsec maximum to accuracy of the converter	For any analog or digital step change
Digital Inputs Logic Voltage Levels		CMOS transient protected
Logic "0" Logic "1"	−0.3 V-dc to 0.8 V-dc +2.4 V-dc to +5.5 V-dc	Does not need external logic voltage 0.1 TTL load
Input Currents		
Data Bits (B1-B16)	30μA typical, "active" pull down to Ground (GND)	For less than 16-bits input, unused pins can be left unconnected
HBE, LBE, LDC (#A and #B)	−15 μA typical, "active" pull up to internal logic supply	When not used pins can be left unconnected
Register Controls		Independent for each channel
HBE#A, HBE#B	Logic "1" Logic "0"	8 MSBs enter high byte input register High byte register remains unaffected
LBE#A, LBE#B	Logic "1" Logic "0"	8 LSBs enter low byte input register Low byte register remains unaffected
LDC#A, LDC#B	Logic "1" Logic "0"	Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum	For guaranteed data transfer
Data Set-up time	200 nsec minimum	Before data transfer
Data Hold time	200 nsec minimum	Before input data changes
Power Supplies		
Supply voltages (±V_S) Supply Currents Supply Rejection	±15 V-dc ± 10% ±40 mA maximum 80 dB typical	For ±10 V peak output
Physical Characteristics		
Type	36 PIN Double DIP	
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	3 standoffs are added to the package to insulate it from printed circuit board traces. (Standoffs included in 0.21-inch height dimension)
Weight	0.6 oz (17 g) max	

Absolute Maximum Ratings

Reference Input ..... $-V_S$ to $+V_S$
Power Supply Voltages (±V_S) ..... ±18 V-dc
Digital Inputs ..... −0.3 V-dc to +6.5 V-dc
Storage Temperature ..... -65°C to +135°C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the $+V_S$ and $-V_S$ supplies. A 1μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pins as possible.

Pin Designations

GND — Power Supply Ground
Digital Ground
Analog Signal Ground

B1 - B16 — Parallel Data Input Bits
B1 is MSB = 180 degrees
B16 is LSB = 0.0055 degree

HBE #A, HBE #B — High Byte Enable —
Data inputs B1 through B8 enter the corresponding input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins.

LBE #A, LBE #B — Low Byte Enable —
Data inputs B9 through B16 enter the corresponding input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.

LDC #A, LDC #B — Load Converter —
When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the corresponding 16-bit holding register. When LDC is set to Logic "Low," the corresponding converter channel is in the hold mode and is not affected by digital activity in the input registers.

+Vs, −Vs — Supply Voltages —
Typically ±15 V-dc

LBE #B	1	36	HBE #B
COS θ_A	2	35	HBE #A
SIN θ_A	3	34	B1
GC1 #B	4	33	B2
GC2 #B	5	32	B3
V_{IN} #B	6	31	B4
GC1 #A	7	30	B5
GC2 #A	8	29	B6
V_{IN} #A	9	28	B7
COS θ_B	10	27	B8
SIN θ_B	11	26	B9
N.C.	12	25	B10
+Vs	13	24	B11
−Vs	14	23	B12
LDC #B	15	22	B13
LDC #A	16	21	B14
LBE #A	17	20	B15
GND	18	19	B16

FIGURE 2 HDSC2036 Pin Assignments

V_{IN} #A, V_{IN} #B — Reference Voltage Inputs

GC1 #A, GC2 #A
GC1 #B, GC2 #B — Gain programming pins (see text for connections)

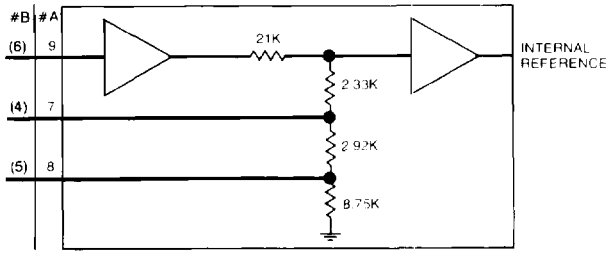
SIN θ_A, COS θ_A
SIN θ_B, COS θ_B — Output Analog Signals for channel A and channel B

Caution: Reversal of +Vs and −Vs power supply connections will result in permanent damage to the converter.

Analog Output Gain Control and Phasing

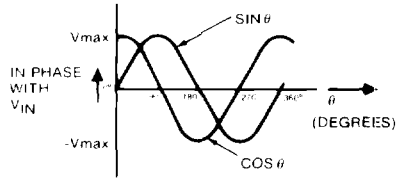
An equivalent circuit for gain control is shown in figure 3. When both gain-control pins 7 (4) and 8 (5) are left unconnected (OPEN), the gain of the converter is 2.0 (i.e., output analog signals are 2 x V_{IN} Sin θ and 2 x V_{IN} Cos θ). When pin 8 (5) is connected to GND and pin 7 (4) is left unconnected the converter gain is 1.0. When pin 7 (4) is connected to GND and pin 8 (5) is left unconnected the converter gain is 0.5. The accuracy of the gain resistors is 0.05%. As can be seen from the equivalent circuit, the gain of the converter can be modified by adding a resistor between pin 7 (4) or 8 (5) and GND. Users, however, are cautioned against using a large value resistor as the temperature coefficient of the external resistor will not be matched with TCR of internal resistor. Note that two channels can be set-up for different gains, if required.

Figure 4 shows the output phasing and gives mathematical relationship between reference voltage V_{IN} and output analog signals as function of digital angle θ and converter gain K.



GC1 #A (PIN 7)	GC2 #A (PIN 8)	GAIN (K)
GND	OPEN	0.5
OPEN	GND	1.0
OPEN	OPEN	2.0
GC1 #B (PIN 4)	GC2 #B (PIN 5)	GAIN (K)

FIGURE 3 Reference Conditioner



SIN OUTPUT = K • V_{IN} • (1 + n) SIN θ

COS OUTPUT = K • V_{IN} • (1 + n) COS θ

K IS THE GAIN OF THE CONVERTER AND n IS THE SCALE FACTOR VARIATION AS A FUNCTION OF DIGITAL ANGLE (±0.03%)

FIGURE 4 Output Phasing

Digital Interface

The digital interface structure of the HDSC2036 is identical to interfacing two (2) HDSC2026 converters sharing a common data bus. Each channel of the dual digital-to-sin/cos converter has its own double-buffered input register configuration for digital angle input. All control signals for registers are independent for each channel, allowing the user an easily implemented interface with an 8- or 16-bit microprocessor data bus. Independent register enable controls offer the flexibility of either asynchronous or synchronous updating of both channels of the converter.

Continuous Operation

As shown in Figure 5, for asynchronous operation, when using the same data word for both channels, all register enables may be left "floating." All inputs LBE#A, HBE#A, LDC#A, LBE#B, HBE#B and LDC#B have internal active pull ups ($\approx 15\mu A$), permitting these pins to be left unconnected for continuous update. Note that all registers are level-actuated or "transparent," allowing asynchronous data update when the enable controls are at logic "1" or open. The parallel information at the data inputs B1-B16 is continuously converted to sin θ and cos θ analog outputs for both channels multiplied by their own independent reference V_{IN}. For applications requiring less than 16-bit resolution unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

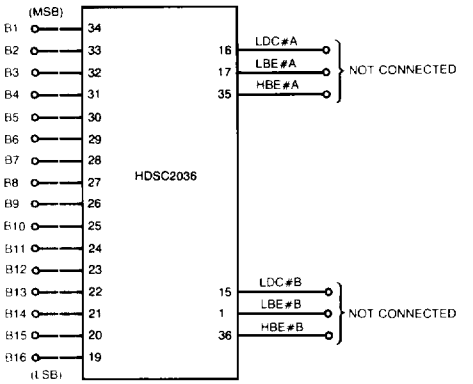


FIGURE 5 Digital Connections for Continuous Operation

Two-Byte Loading

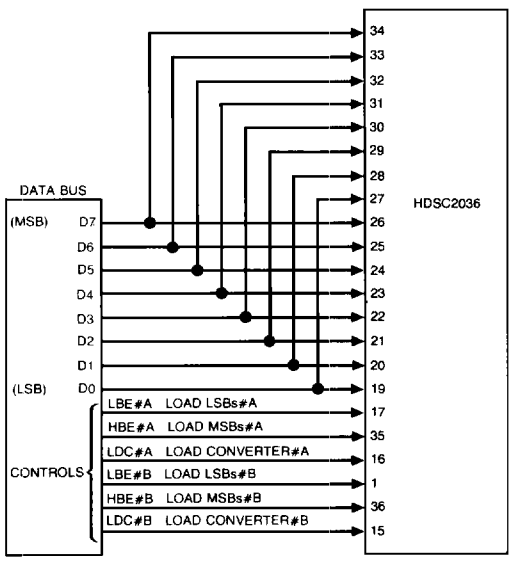


FIGURE 6 Digital Connections for Two-Byte Loading

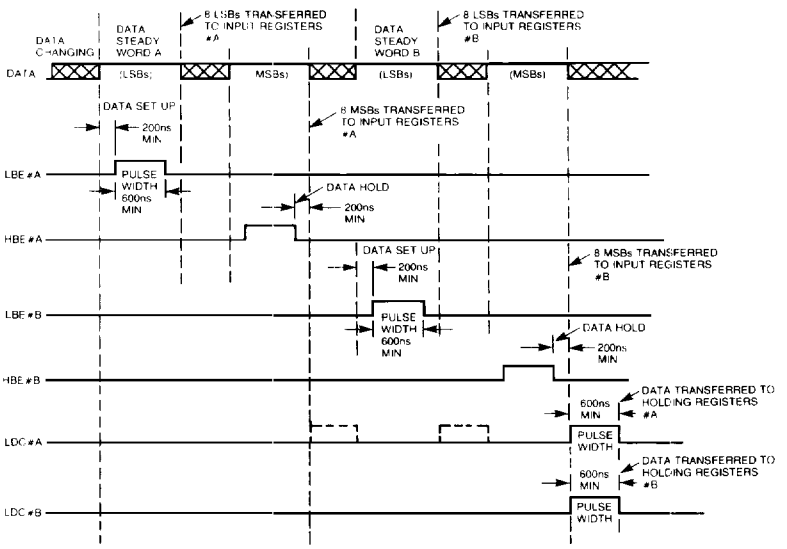


FIGURE 7 Two-Byte Loading.

The circuit configuration and timing diagram for two-byte loading of a common digital word for both channels is the same as for a single channel digital-to-sin/cos converter (see Natel data sheet HDSC2026), except that the corresponding enable controls for both channels are tied together i.e., LBEs (Pin 17 tied to Pin 1), HBEs (Pin 35 tied to Pin 36) and LDCs (Pin 16 tied to Pin 15).

The circuit configuration for two-byte loading of two separate digital words representing different angles for the two channels from an 8-bit data bus is shown in Figure 6. As shown in timing diagram of Figure 7, the 8 LSBs (B9-B16) are transferred to the low-byte input register of Channel A when LBE#A is a logic "1." LBE#A can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE#A goes "Low." Bits B1-B8 are transferred to the high-byte input register of Channel A when HBE#A is a logic "1." The timing requirements are the same as those for LBE#A. Similarly LBE#B and HBE#B control the transfer of data bits into input registers of Channel B.

Data for Channel A is transferred from two input registers of Channel A to its own holding register when LDC#A (load converter A) is at logic "1." If LDC#A is at logic "0," the contents of the holding register of Channel A are latched and remain at their previous values unaffected by changes at the data inputs of the common bus or input registers. Similarly LDC#B (load converter B) controls the holding register of Channel B. As shown in Figure 7 timing diagram, LDC#A can be applied at any time after Channel A data has been transferred to its input registers. For applications requiring simultaneous update of output analog signals LDC#A and LDC#B should be applied at the same time. An example of such applications is a 2-speed digital-to-synchro/resolver converter. Note that LBE, HBE and LDC for both channels are level actuated functions.

Single-Byte Loading

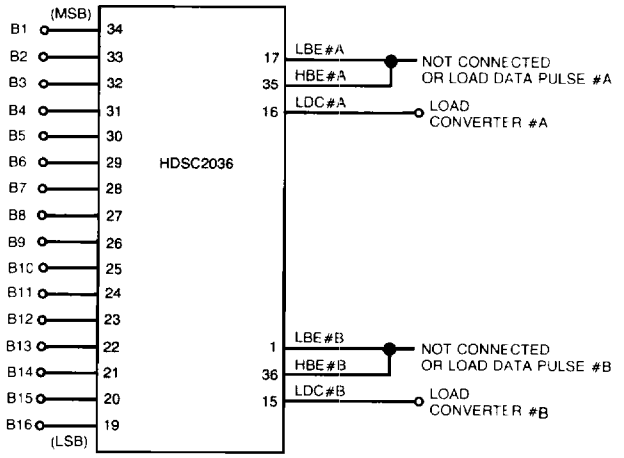


FIGURE 8 Digital Connections for One Byte (16 bits) Loading

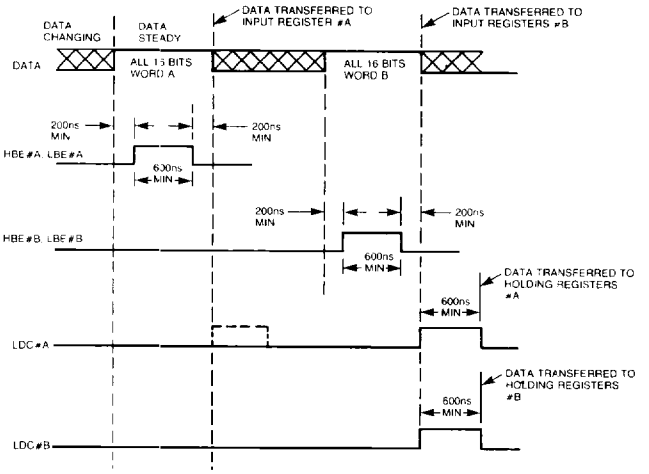


FIGURE 9 Single-Byte Loading.

The circuit configuration and timing diagram for one-byte loading of a common digital word for both channels is the same as for a single channel digital-to-sin/cos converter (see Natel data sheet HDSC2026) except that the two sets of input register controls and two holding register controls are tied together i.e., LBEs and HBEs (Pin 17, Pin 1, Pin 35 and Pin 36 tied together) and LDCs (Pin 16 tied to Pin 15).

Single 16-bit byte loading of two separate digital words representing different angles for the two channels is illustrated in Figure 8. As shown in timing diagram (Figure 9), 200 nsec after the data is stable for Channel A, the angular information can be transferred to the outputs of holding register by applying a logic "1" to LDC#A. Similarly LDC#B controls the data transfer for Channel B. Again, for simultaneous update of analog signals, both channels LDC#A and LDC#B should be applied at the same time.

Applications using HDSC2036

Resolver Computing Circuits

Two channels in a small physical size and high accuracy of the HDSC2036 converter make it a practical choice for flight control systems, missile seekers, and tracking systems where many coordinate rotations and transformations are required. The computations, if carried out by microcomputer, are time consuming and complex, whereas the converter approach requires very little hardware and the response time is limited only by the slew rate of the operational amplifiers used. Transformer coupling may also be used and, in fact, by appropriately interconnecting transformers and HDSC2036, complete resolver computing chains can be developed to solve a wide variety of coordinate conversion and transformation problems.

HDSC2036 connected as shown in figure 10 is the solid state equivalent of an electromechanical resolver of figure 11. While rivaling the accuracy of its electromechanical counterpart it eliminates the mechanical complexity of such systems and, since it is self-buffering, does not require the buffer amplifiers normally encountered in resolver computing chains.

Figure 12 shows a convenient shorthand notation for representing the computing resolver in a resolver chain computation. When representing the circuit of figure 10 it is understood that this notation includes the entire circuit and that the angle input is in digital form.

All basic vector operations such as resolution, coordinate rotations, coordinate transformations, etc. can be carried out using this basic circuit. Coupling transformers are employed as this method of summing and differencing the outputs of the converter offers better accuracy than operational amplifier summing and does not propagate dc offsets through the computation. The transformation ratio of the converter must be taken into account in these circuits to preserve the scale factor throughout the computation.

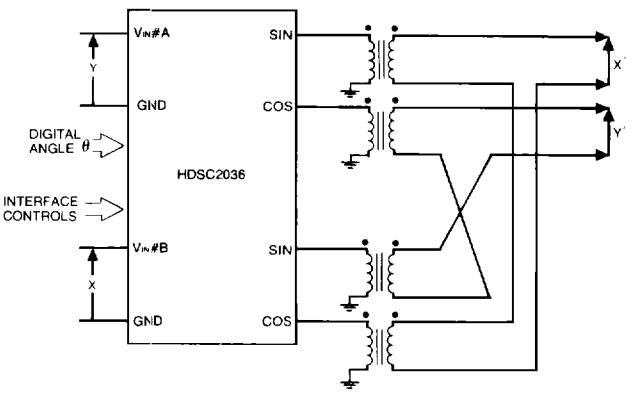


FIGURE 10 HDSC2036 Connected as Computing Resolver

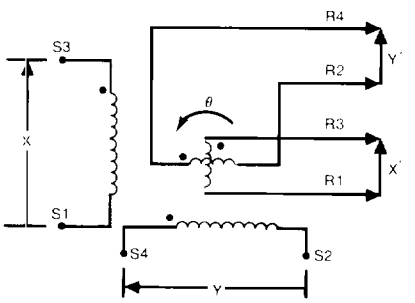


FIGURE 11 Computing Resolver Schematic

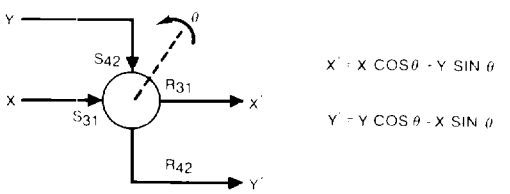
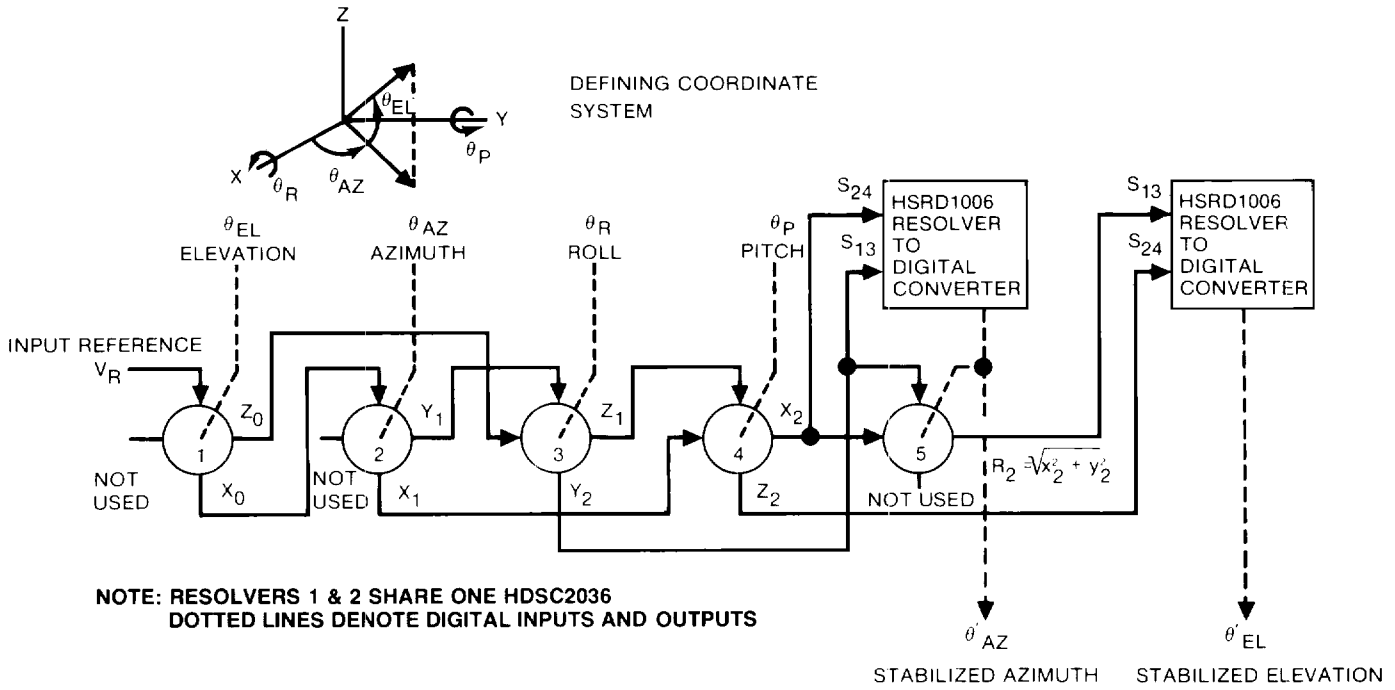


FIGURE 12 Computing Resolver Notation for Circuits of Figures 10 and 11



NOTE: RESOLVERS 1 & 2 SHARE ONE HDSC2036
DOTTED LINES DENOTE DIGITAL INPUTS AND OUTPUTS

TRANSFORMATION EQUATIONS

RESOLVER 1:
$$X_0 = V_R \cos\theta_{EL}$$
$$Z_0 = V_R \sin\theta_{EL}$$

RESOLVER 2:
$$X_1 = X_0 \cos\theta_{AZ}$$
$$Y_1 = X_0 \sin\theta_{AZ}$$

RESOLVER 3:
$$Y_2 = Y_1 \cos\theta_R - Z_0 \sin\theta_R$$
$$Z_1 = Y_1 \sin\theta_R + Z_0 \cos\theta_R$$

RESOLVER 4:
$$X_2 = Z_1 \sin\theta_P + X_2 \cos\theta_P$$
$$Z_2 = Z_1 \cos\theta_P - X_2 \sin\theta_P$$

OUTPUTS

$$\theta'_{AZ} = \tan^{-1}\frac{Y_2}{X_2}$$

$$\theta'_{EL} = \tan^{-1}\frac{Z_2}{\sqrt{X_2^2 + Y_2^2}}$$

FIGURE 13 Solid State Resolver Stabilization System

Figure 13 shows a resolver computation network to solve the problem of stabilizing an inertial platform undergoing motion about its azimuth, elevation, roll, and pitch axes. Such a system might be applied to controlling the stabilization vanes on a modern ship or a helicopter-mounted TV camera used for the evening news. The system performs the vector resolution and coordinate transformations required to maintain the platform at a constant inertial position.

In this example resolver networks 1 and 2 perform the vector resolutions of the platform azimuth θ_{AZ}, and the platform elevation, θ_{EL}, into their components in the X, Y and X, Z planes of the defining coordinate system. Resolvers 3 and 4 perform the coordinate transformation to the new coordinate system tilted by the roll angle, θ_R, and the pitch angle θ_P.

Finally the transformed vectors Y_2, Z_1 and X_2, Z_2 undergo vector composition to generate the stabilized azimuth, θ'_{AZ}, and elevation θ'_{EL} platform commands. The Resolver-to-Digital (R/D) converter (Natel Model HSRD1006) operating in conjunction with resolver network 5 computes both the stabilized azimuth angle and the vector R_2 required to calculate the stabilized elevation angle, θ'_{EL}. From the notation in figure 12, resolver network 5 solves the equation:

$$X' = X_2 \cos\theta'_{AZ} + Y_2 \sin\theta'_{AZ}$$

where θ'_{AZ} is supplied by the R/D converter.

Since $\theta'_{AZ} = \tan^{-1}\frac{Y_2}{X_2}$, then

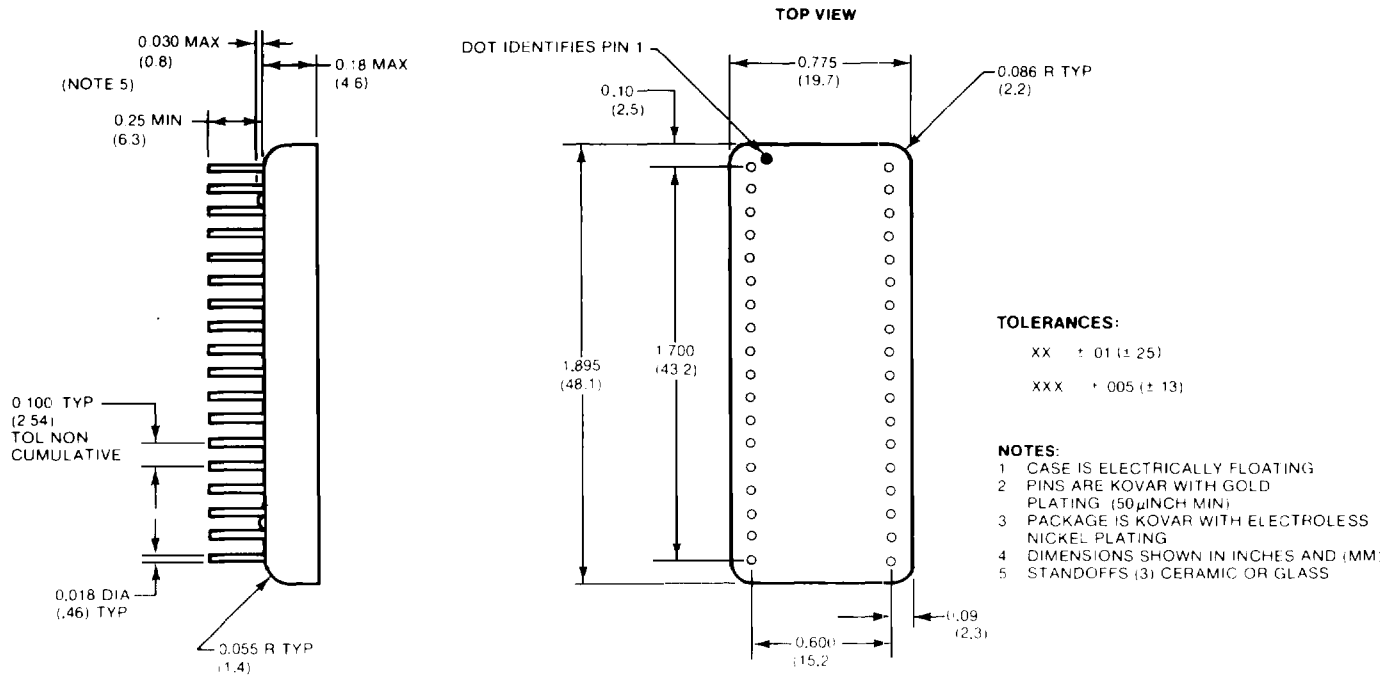
$\cos\theta'_{AZ} = \frac{X_2}{R_2}$ and $\sin\theta'_{AZ} = \frac{Y_2}{R_2}$

Substituting these values in the equation for X′ gives:

$$X' = X_2\left(\frac{X_2}{R_2}\right) + Y_2\left(\frac{Y_2}{R_2}\right)$$

$$X' = \frac{X_2^2 + Y_2^2}{R_2} \quad \text{or} \quad \boxed{X' = R_2}, \text{ as } R_2^2 = X_2^2 + Y_2^2$$

Thus, an entire coordinate conversion system can be implemented with only six hybrid converters at significantly less cost than its electromechanical counterpart and requires much less space. Added bonuses are the low power consumption, data-bus compatibility and high accuracy. Since the computations are carried continuously, significant improvement in computation time is gained over performing these complex calculations in a computer or microprocessor.



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HDSC2036 - T F A

Temperature Range
1 = 0°C to +70°C
2 = -25°C to +85°C
3 = -55°C to +125°C

Frequency Range
4 = dc to 1000 Hz
5 = dc to 10 kHz

Accuracy
S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit synchro(resolver)-to-digital converters pin-compatible with existing designs, but with superior performance (HSD/HRD1014)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006)
- 14-bit Digital-to-Synchro/Resolver converter that is pin-compatible with existing designs, with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504).

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Third Printing 5K 9/89
H407 - 2.5M 2/87