

**RADIATION HARDENED
 LOGIC LEVEL POWER MOSFET
 SURFACE MOUNT (UB) and (UBC)**

**2N7626UB
 IRHLUB7970Z4
 2N7626UBC
 IRHLUBC7970Z4
 60V, P-CHANNEL
 TECHNOLOGY**

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLUB7970Z4	100K Rads (Si)	1.40 Ω	- 0.53A
IRHLUBC7970Z4			
IRHLUB7930Z4	300K Rads (Si)	1.40 Ω	-0.53A
IRHLUBC7930Z4			



International Rectifier's R7™ Logic Level Power Mosfets provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Complimentary N-Channel Available - IRHLUB770Z4, IRHLUBC770Z4

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ $V_{GS} = -4.5V, T_C = 25^\circ C$	Continuous Drain Current	-0.53	A
I_D @ $V_{GS} = -4.5V, T_C = 100^\circ C$	Continuous Drain Current	-0.33	
I_{DM}	Pulsed Drain Current ①	-2.12	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	0.57	W
	Linear Derating Factor	0.0045	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
EAS	Single Pulse Avalanche Energy ②	33.5	mJ
I_{AR}	Avalanche Current ①	-0.53	A
EAR	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-4.4	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	43 (Typical)	mg

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
B _V DSS	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔB _V DSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.055	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.40	Ω	V _{GS} = -4.5V, I _D = -0.33A ^④
V _{GS(th)}	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	3.1	—	mV/°C	
g _{fs}	Forward Transconductance	0.8	—	—	S	V _{DS} = -10V, I _{DS} = -0.33A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100	nA	V _{GS} = 10V
Q _g	Total Gate Charge	—	—	3.6	nC	V _{GS} = -4.5V, I _D = -0.53A V _{DS} = -30V
Q _{gs}	Gate-to-Source Charge	—	—	1.5		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
t _{d(on)}	Turn-On Delay Time	—	—	22	ns	V _{DD} = -30V, I _D = -0.53A, V _{GS} = -5.0V, R _G = 7.5Ω
t _r	Rise Time	—	—	22		
t _{d(off)}	Turn-Off Delay Time	—	—	27		
t _f	Fall Time	—	—	27		
L _S + L _D	Total Inductance	—	8.4	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	167	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	43	—		
C _{rss}	Reverse Transfer Capacitance	—	10	—		
R _g	Gate Resistance	—	56	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.53	A	T _j = 25°C, I _S = -0.53A, V _{GS} = 0V ^④
I _{SM}	Pulse Source Current (Body Diode) ^①	—	—	-2.12		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _F = -0.53A, di/dt ≤ -100A/μs
t _{rr}	Reverse Recovery Time	—	—	50	ns	V _{DD} ≤ -25V ^④
Q _{RR}	Reverse Recovery Charge	—	—	25	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJA}	Junction-to-Ambient	—	—	220	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHLUB7970Z4, 2N7626UB IRHLUBC7970Z4, 2N7626UBC

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V _{GS} = 0V, I _D = -250μA
V _{GS(th)}	Gate Threshold Voltage	-1.0	-2.0	V	V _{GS} = V _{DS} , I _D = -250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100		V _{GS} = 10V
I _{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-39) ④	—	1.36	Ω	V _{GS} = -4.5V, I _D = -0.33A
	Static Drain-to-Source On-state Resistance (UB and UBC)	—	1.40	Ω	V _{GS} = -4.5V, I _D = -0.33A
V _{sd}	Diode Forward Voltage ④	—	-5.0	V	V _{GS} = 0V, I _D = -0.53A

1. Part numbers IRHLUB7970Z4, IRHLUB7930Z4 and IRHLUBC7970Z4, IRHLUBC7930Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V	@VGS= 8V	@VGS= 10V
Br	37	285	36.8	-60	-60	-60	-60	-60	-50	-35	-25
I	60	345	32.7	-60	-60	-60	-60	-60	-20	-	-
Au	82	357	28.5	-60	-60	-60	-60	-	-	-	-

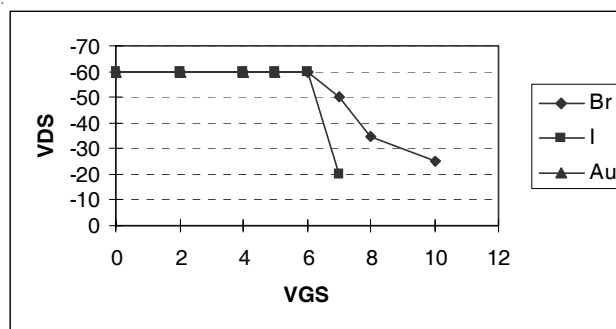


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

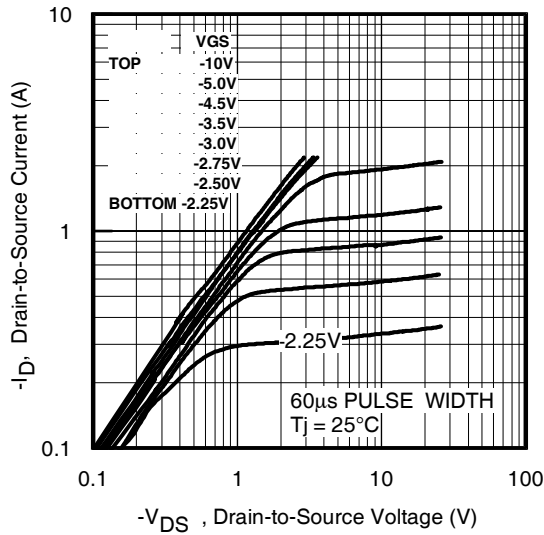


Fig 1. Typical Output Characteristics

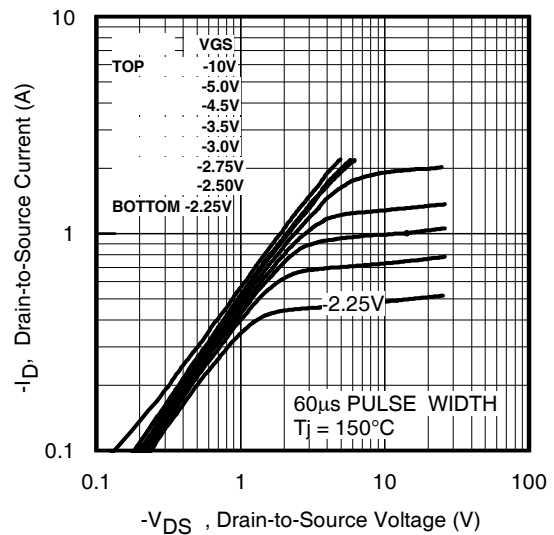


Fig 2. Typical Output Characteristics

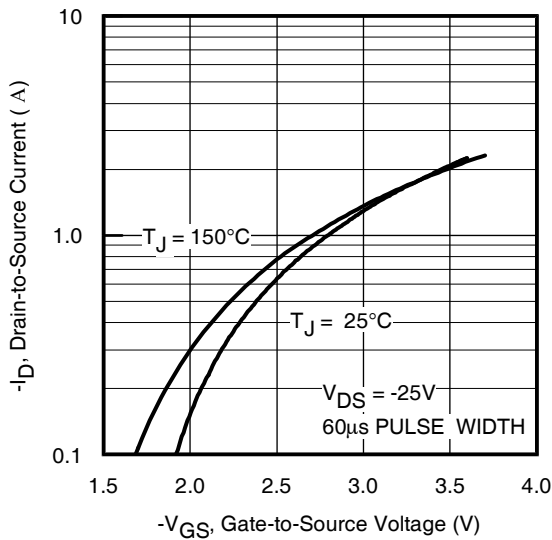


Fig 3. Typical Transfer Characteristics

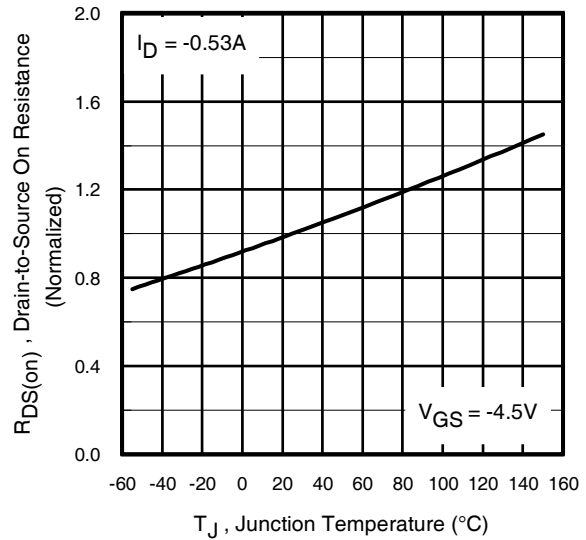


Fig 4. Normalized On-Resistance Vs. Temperature

Pre-Irradiation

IRHLUB7970Z4, 2N7626UB
IRHLUBC7970Z4, 2N7626UBC

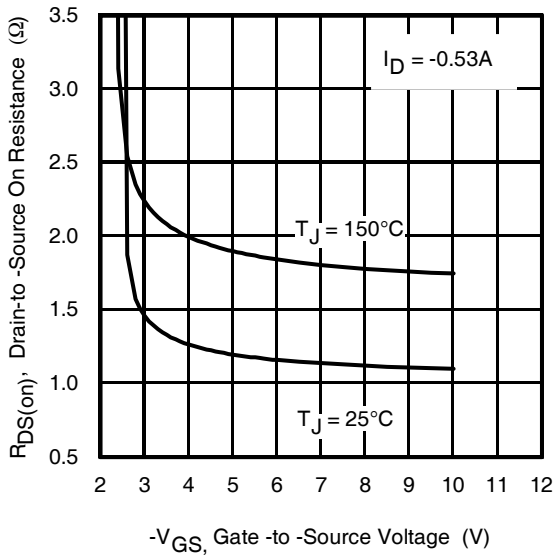


Fig 5. Typical On-Resistance Vs Gate Voltage

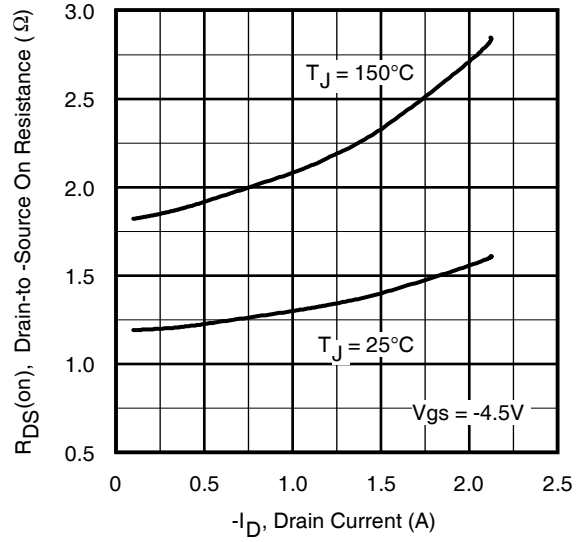


Fig 6. Typical On-Resistance Vs Drain Current

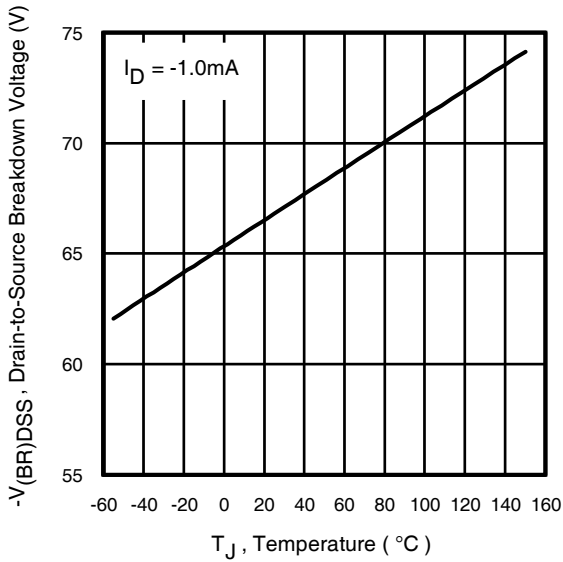


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

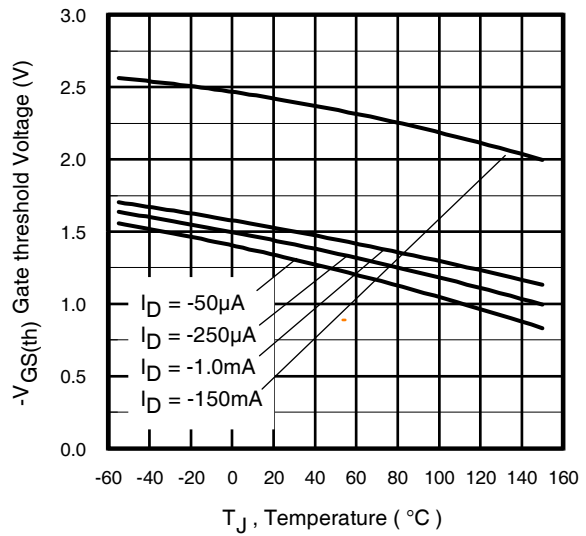


Fig 8. Typical Threshold Voltage Vs Temperature

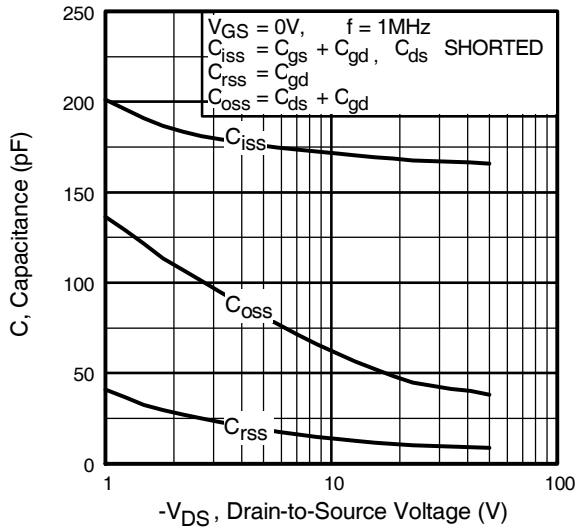


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

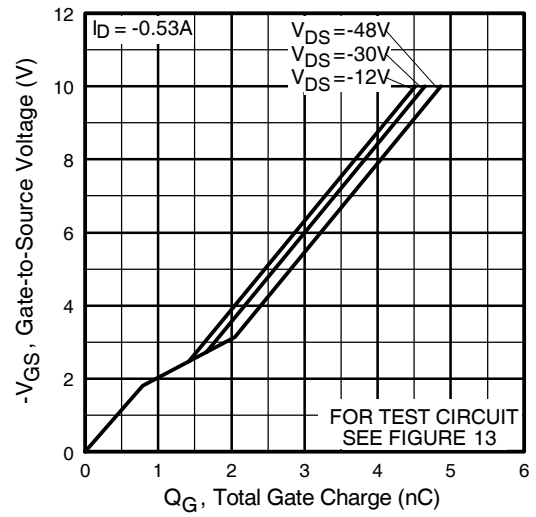


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

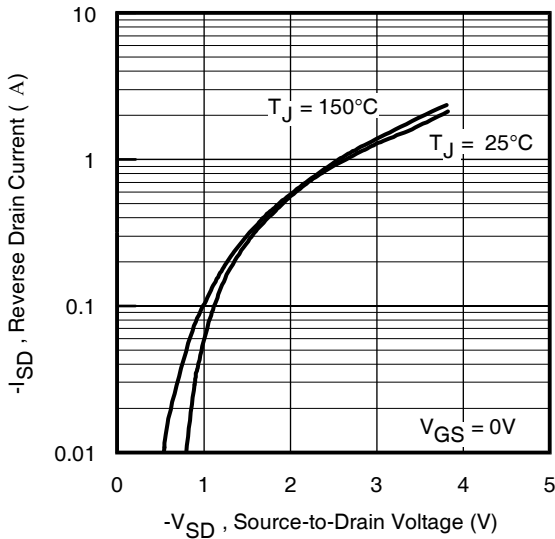


Fig 11. Typical Source-Drain Diode Forward Voltage

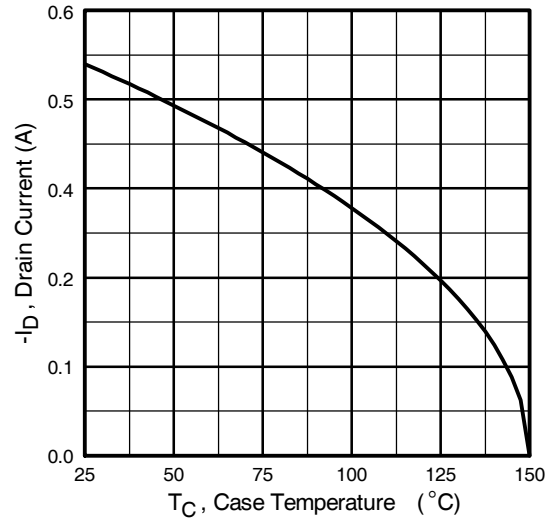


Fig 12. Maximum Drain Current Vs. Case Temperature

Pre-Irradiation

IRHLUB7970Z4, 2N7626UB
 IRHLUBC7970Z4, 2N7626UBC

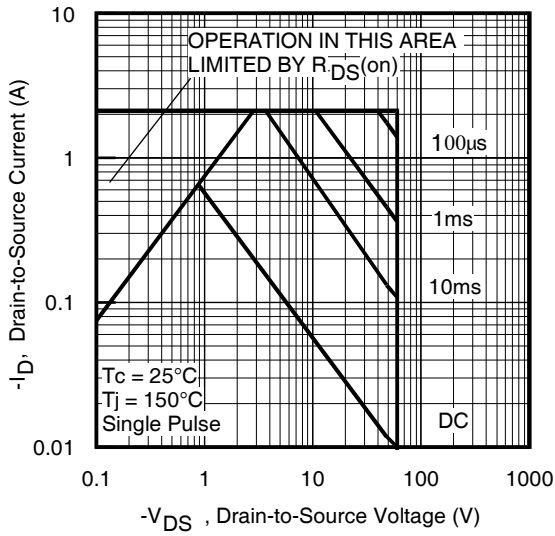


Fig 13. Maximum Safe Operating Area

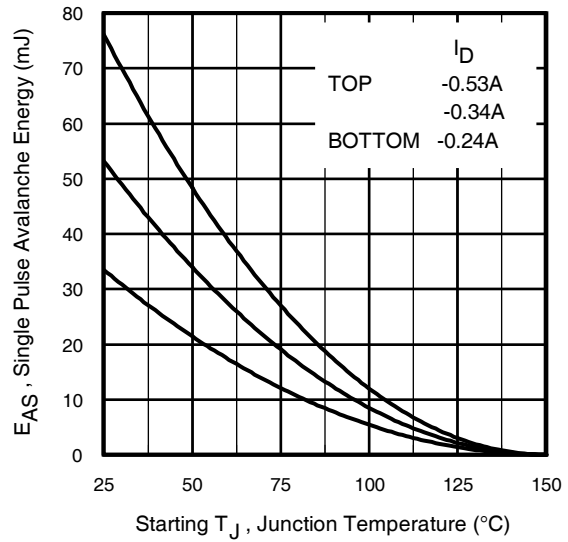


Fig 14. Maximum Avalanche Energy Vs. Drain Current

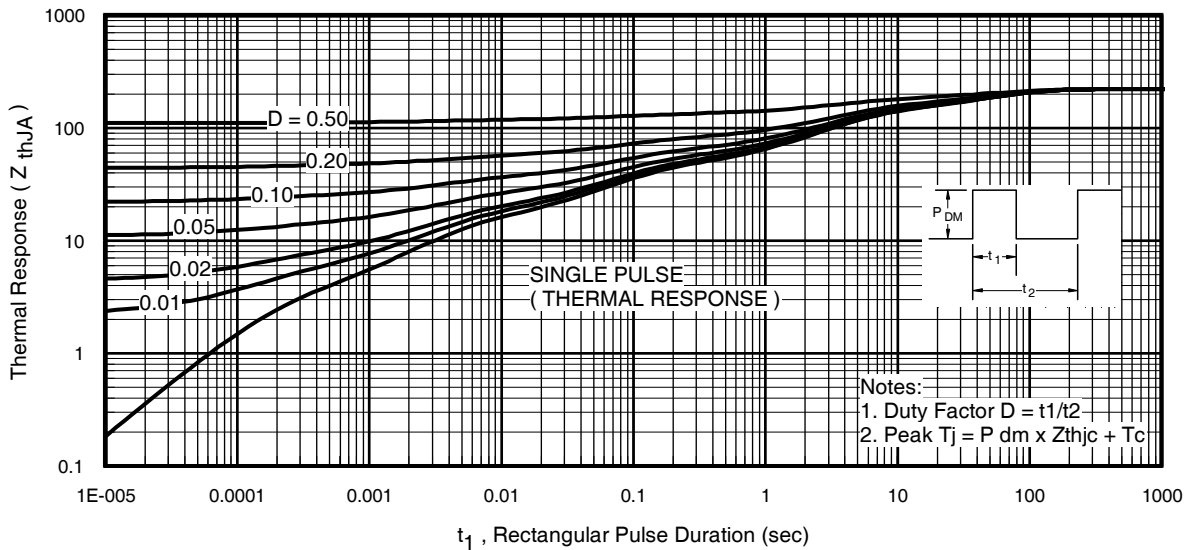


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRHLUB7970Z4, 2N7626UB
 IRHLUBC7970Z4, 2N7626UBC

Pre-Irradiation

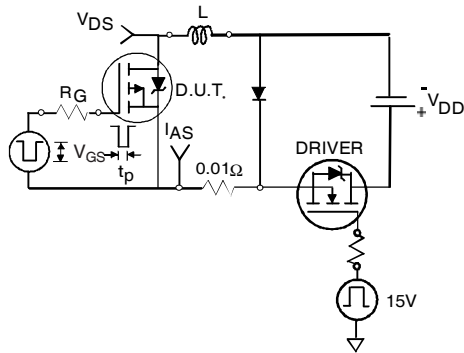


Fig 16a. Unclamped Inductive Test Circuit

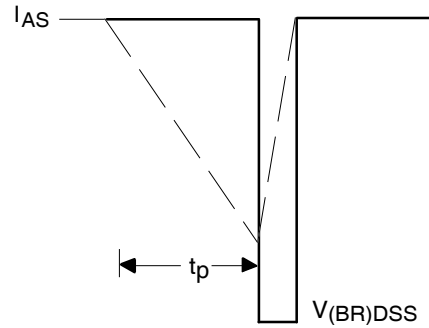


Fig 16b. Unclamped Inductive Waveforms

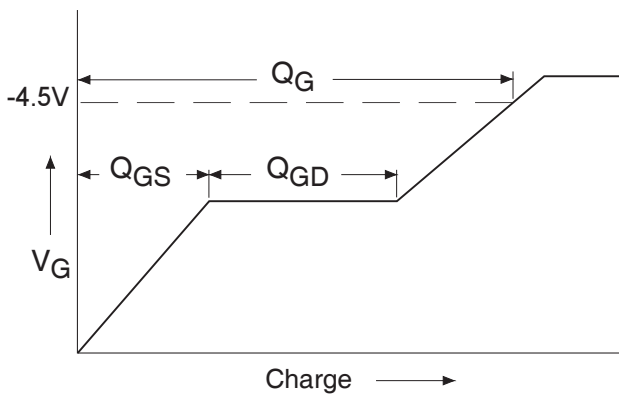


Fig 17a. Basic Gate Charge Waveform

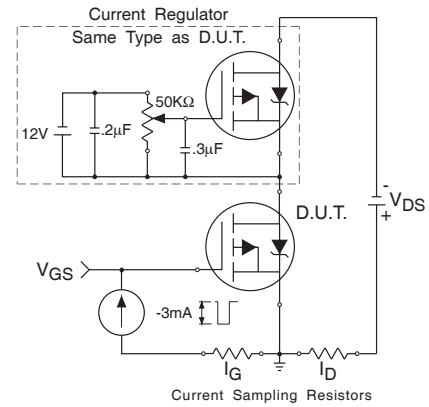


Fig 17b. Gate Charge Test Circuit

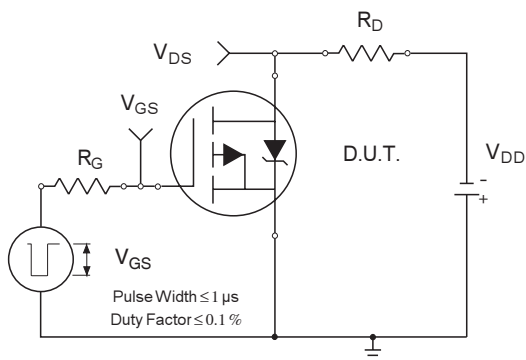


Fig 18a. Switching Time Test Circuit

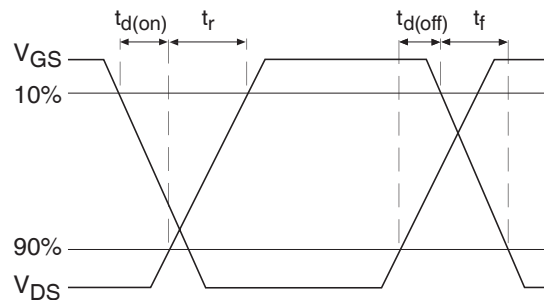
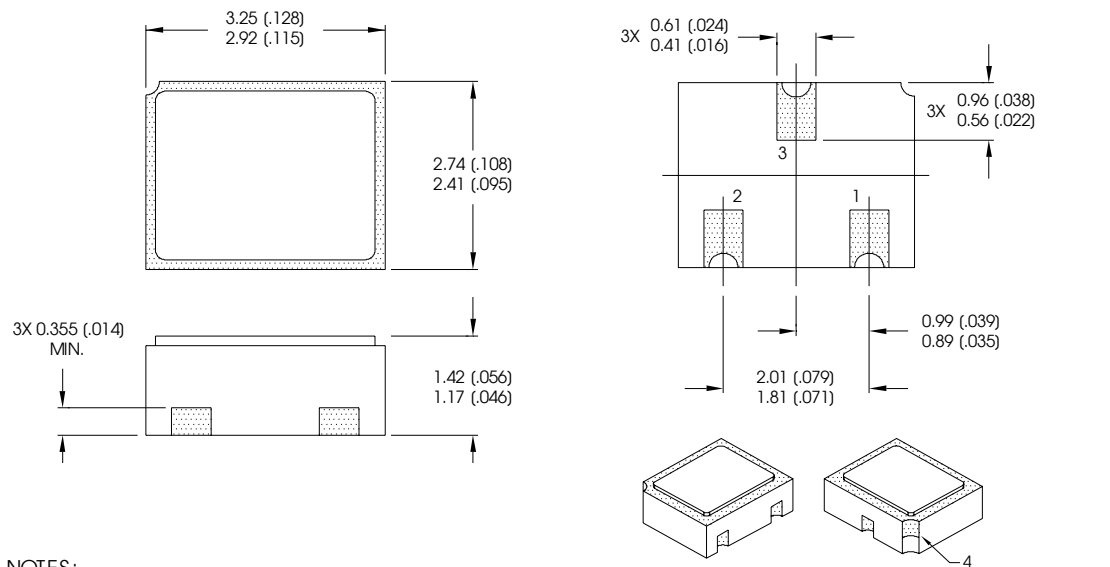


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions — UB (Metal Lid)



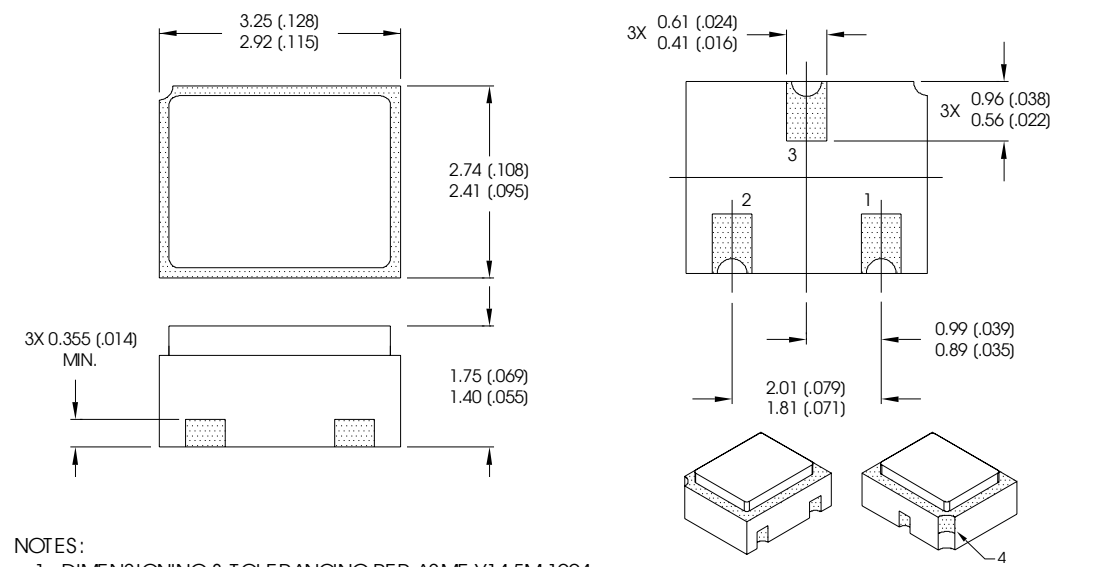
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.

PAD ASSIGNMENTS

- 1 = GATE
- 2 = SOURCE
- 3 = DRAIN
- 4 = SHIELDING CONNECTED TO THE LID

Case Outline and Dimensions — UBC (Ceramic Lid)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.

PAD ASSIGNMENTS

- 1 = GATE
- 2 = SOURCE
- 3 = DRAIN
- 4 = SHIELDING CONNECTED TO THE LID

IRHLUB7970Z4, 2N7626UB
IRHLUBC7970Z4, 2N7626UBC

Pre-Irradiation

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 238mH$
Peak $I_L = -0.53A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -0.53A$, $di/dt \leq -100A/\mu s$,
 $V_{DD} \leq -60V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

International
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