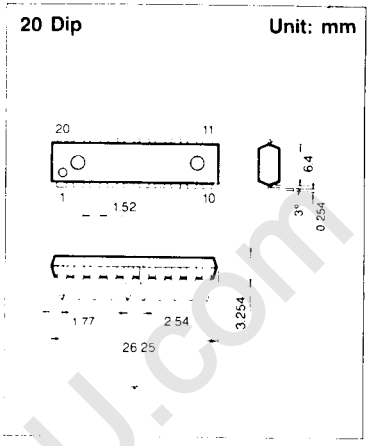
Octal Buffers and Line Drivers with 3-States Outputs



The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

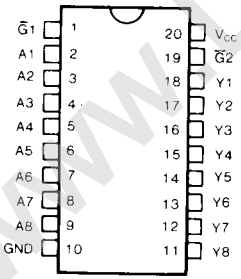
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FEATURES

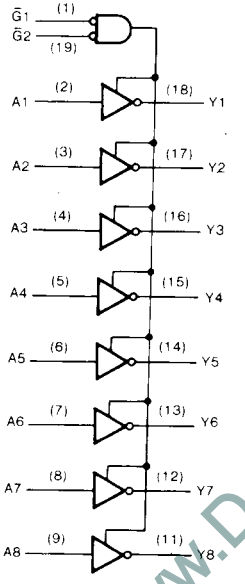
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C

PIN CONFIGURATION

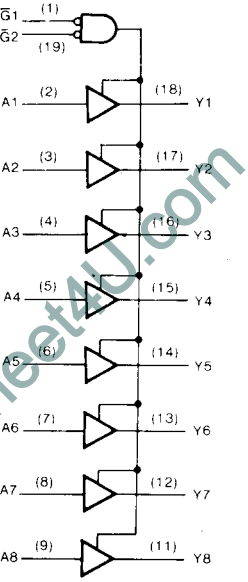


LOGIC DIAGRAM

'540



'541



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Ratings	Unit
Supply Voltage Range	V_{CC}	−0.5 to +7.0	V
DC Input Diode Current (V_I<−0.5V or V_I>V_{CC} +0.5V)	I_{ik}	±20	mA
DC Output Diode Current (V_O<−0.5V or V_O>V_{CC} +0.5V)	I_{ok}	±20	mA
Continuous Output Current Per Pin (−0.5V<V_O<V_{CC} +0.5V)	I_o	±70	mA
Continuous Current Through V_{CC} or GND pins		±250	mA
Power Dissipation Per Package	P_d†	500	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Value			Unit
			Min	Typ	Max	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
DC Input & Output Voltages*		V_{IN}, V_{OUT}	0		V_{CC}	V
Operating Temperature Range	KS74AHCT KS54AHCT	T_A	−40 −55		+85 +125	°C °C
Input Rise & Fall Times		t_r, t_f			500	ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_A=25°C	KS74AHCT T_A=−40°C to +85°C	KS54AHCT T_A=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT540/541

Characteristic	Symbol	Conditions†		$T_A = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54AHCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay, Delay, A to Y	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		6 12	10 19	12 23	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		6 12	10 19	12 23	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	11 17	18 27	22 33	ns
	t_{PZL}		$C_L = 50pF$ $C_L = 50pF$	11 17	18 27	22 33	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		9	14	17	ns
	t_{PLZ}			9	14	17	
Maximum Input Capacitance	C_{IN}			5			pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10			pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G} = V_{CC}$ $\overline{G} = GND$		5 30			pF

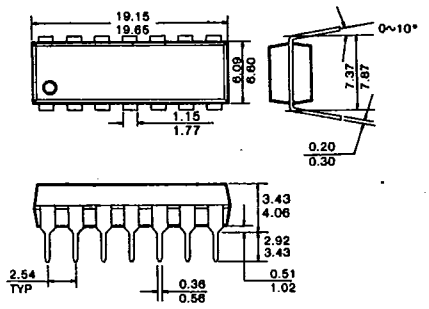
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

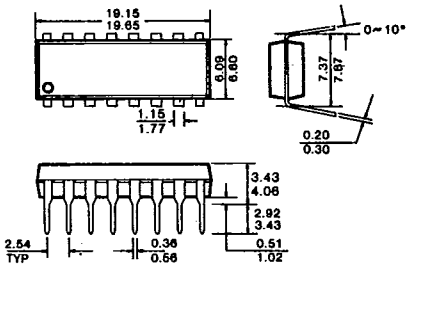
T-90-20

1. PLASTIC PACKAGES

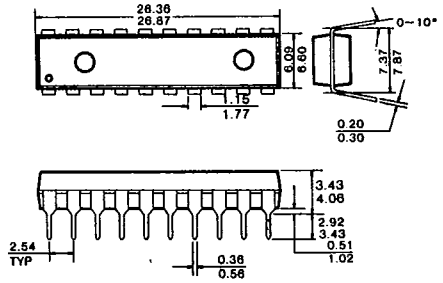
14-Pin Plastic DIP **Units: mm**



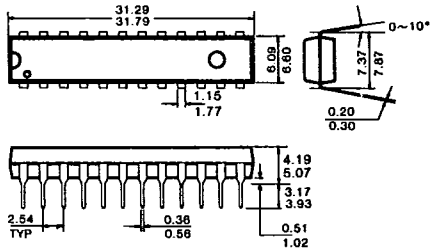
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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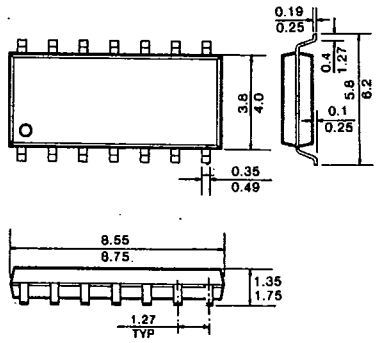
PACKAGE DIMENSIONS

T-90-20

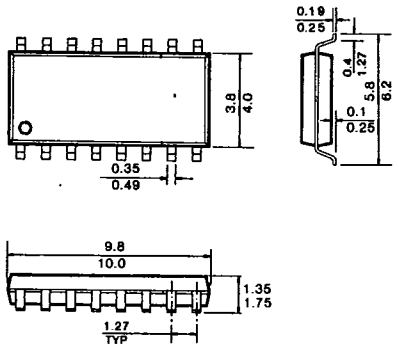
14-Pin SOP

Unit: mm



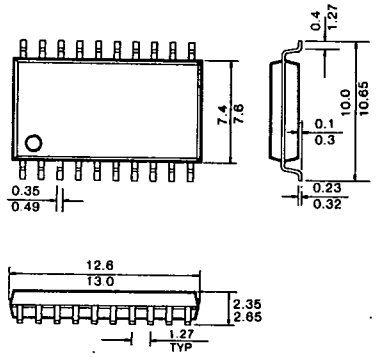
16-Pin SOP

Unit: mm



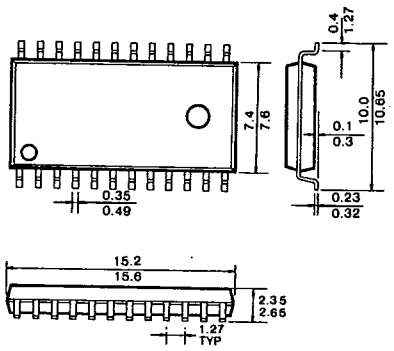
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

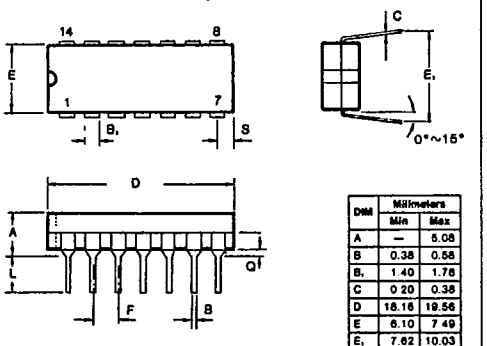


PACKAGE DIMENSIONS

T-90-20

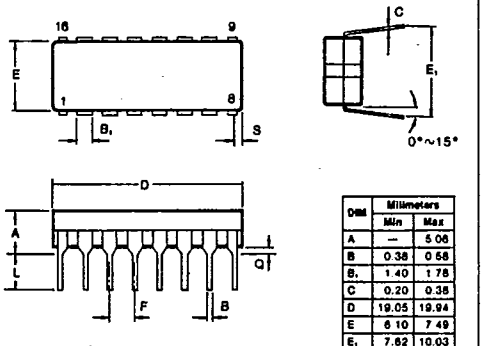
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



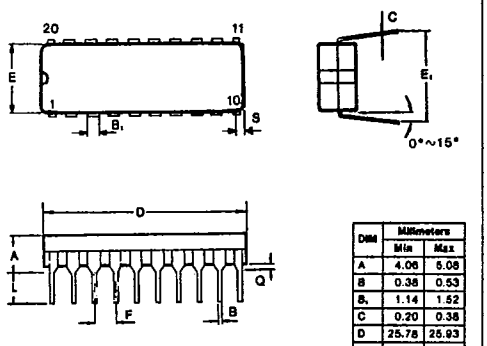
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



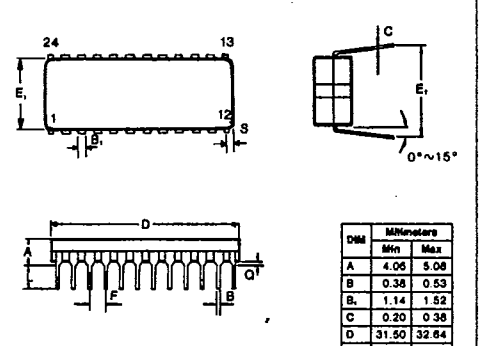
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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