OKI Semiconductor

MSM5839C

40-DOT SEGMENT DRIVER

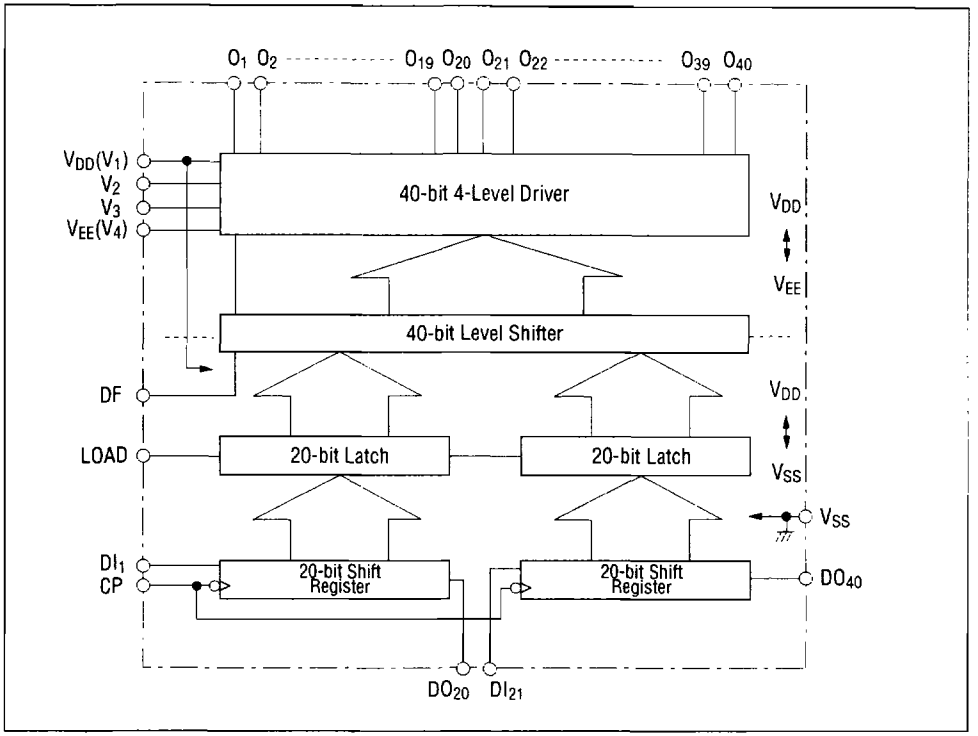
GENERAL DESCRIPTION

The MSM5839C is a dot matrix LCD segment driver LSI which is fabricated with low power CMOS metal gate technology. This LSI consists of 40-bit shift register (two 20-bit shift registers), 40-bit latch (two 20-bit latches), 40-bit level shifter and 40-bit 4-level driver.
It converts serial data, which is received from LCD controller LSI, into parallel data and outputs LCD driving waveform to the LCD panel.
This LSI can drive a variety of LCD panels because the bias voltage, which determines an LCD driving voltage, can be optionally supplied from the external source.

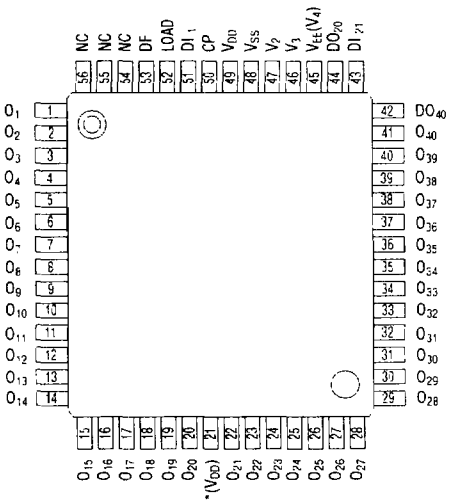
FEATURES

- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 4 to 11V
- Applicable LCD duty : 1/3 to 1/64
- Bias voltage can be supplied externally.
- Recommended controller LSI: MSM6262-xx
- Package options
  56-pin plastic QFP (QFP56-P-910-2K) (Product name: MSM5839CGS-2K)
  56-pin plastic QFP (QFP56-P-910-K) (Product name: MSM5839CGS-K)
  56-pin plastic QFP (QFP56-P-910-L2) (Product name: MSM5839CGS-L2)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

56-Pin Plastic QFP

- This pin is internally connected with V_{DD}, so it must not be connected to other signals. It is also prohibited to use the 21 pin as a V_{DD} independently. This pin may be used as a line reinforcing V_{DD}.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	T_a = 25°C	-0.3 to +6	V
Supply Voltage (2)	V_{DD} - V_{EE} *1	T_a = 25°C	0 to 12	V
Input Voltage	V_I	T_a = 25°C	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	–	-55 to +150	°C

*1: $V_{DD} > V_2 > V_3 > V_{EE}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	–	4.5 to 5.5	V
Supply Voltage (2)	V_{DD} - V_{EE} *1	–	4 to 11	V
Operating Temperature	T_{op}	–	-20 to +85	°C

*1: $V_{DD} > V_2 > V_3 > V_{EE}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ±10%, Ta = -20 to +85°C)

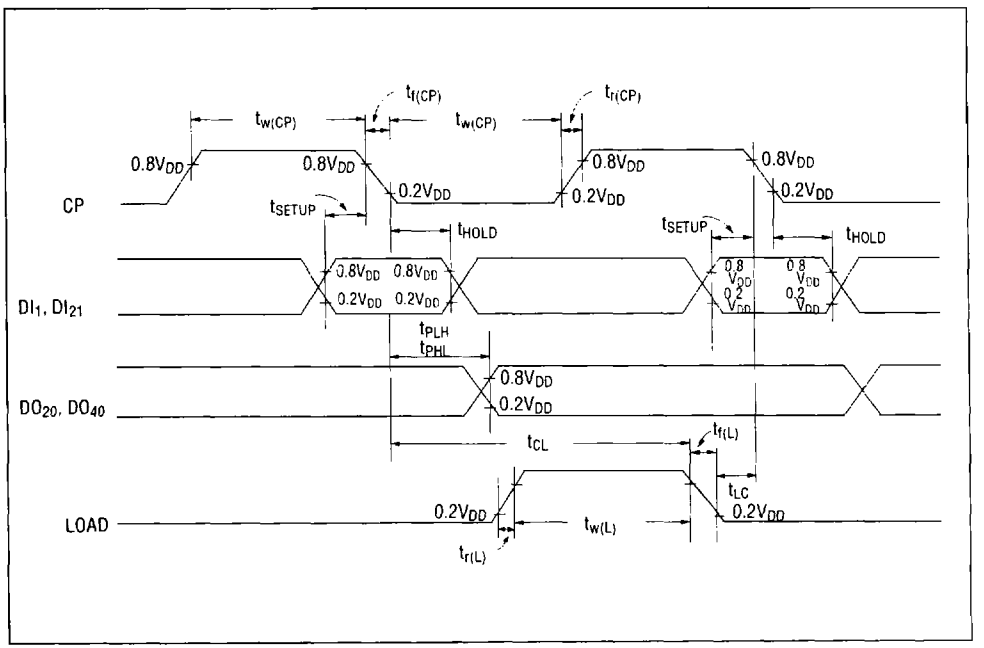
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	–	0.8V_{DD}	–	V_{DD}	V
"L" Input Voltage	V_{IL} *1	–	V_{SS}	–	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	V_{IH} = V_{DD}	–	–	1	µA
"L" Input Current	I_{IL} *1	V_{IL} = 0V	–	–	-1	µA
"H" output Voltage	V_{OH} *2	I_O = -0.4 mA	V_{DD} – 0.4	–	–	V
"L" output Voltage	V_{OL} *2	I_O = 0.4 mA	–	–	0.4	V
ON Resistance	R_{ON} *4	V_{DD} - V_{EE} = 8V IV_N - V_OI = 0.25V *3	–	5	10	kΩ
Current Consumption	I_{DD}	CP = DC V_{DD} - V_{EE} = 11V, No load	–	–	100	µA

*1: Applicable to LOAD, CP, DI_1, DI_{21}, DF
*2: Applicable to DO_{20}, DO_{40}
*3: $V_N = V_{DD} - V_{EE}$, $V_2 = \frac{7}{9}(V_{DD} - V_{EE})$, $V_3 = \frac{2}{9}(V_{DD} - V_{EE})$
*4: Applicable to O_1 - O_{40}

Switching Characteristics

(V_{DD} = 5V ±10%, Ta = -20° to +85°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PLH} t_{PHL}	–	–	–	250	ns
Clock Frequency	f_{CP}	DUTY = 50%	–	–	2	MHz
Clock Pulse Width	$t_{W(CP)}$	–	150	–	–	ns
LOAD Pulse Width	$t_{W(L)}$	–	150	–	–	ns
Data Setup Time DI → CP	t_{SETUP}	–	100	–	–	ns
CP → LOAD Time	t_{CL}	–	250	–	–	ns
LOAD → CP Time	t_{LC}	–	0	–	–	ns
DATA Hold Time DI → CP	t_{HOLD}	–	50	–	–	ns
CP Rise/Fall Time	$t_{r(CP)}$ $t_{f(CP)}$	–	–	–	50	ns
LOAD Rise/Fall Time	$t_{r(L)}$ $t_{f(L)}$	–	–	–	1	µs



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **DI_1**
  The data input pin for the 20-bit shift register (from 1st to 20th bit).

- **CP**
  Clock pulse input pin for the two 20-bit shift registers. The data is shifted in the two 20-bit shift registers at the falling edge of the clock pulse. Data setup time (t_{SETUP}) and data hold time (t_{HOLD}) are required each between DI_1, DI_{21} and CP.

- **DO_{20}**
  The 20th bit output of the shift register.
  The data which is input from DI_1 is clocked out with the delay in the number of bits of the shift register (20). The 40-bit shift register is configured by connecting the output of this pin to DI_{21} pin.

- **DI_{21}**
  The data input pin for the 20-bit shift register (from 21st to 40th bit).
  The connection of DO_{20} pin and this pin allows the device to be used as the 40-bit shift register.

- **DO_{40}**
  The 40th bit output of the shift register.
  The data which is input from DI_1 is clocked out with the delay in the number of the bits of the shift register.
  When extending the number of characters, this pin is used to connect in cascade to the next MSM5839C.

- **DF**
  Alternate signal input pin for LCD driving waveform.

- **$V_{DD}(V_1)$, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 to 5.5V.
  V_{SS} is a ground pin (V_{SS} = 0V).

- **V_2, V_3, $V_{EE}(V_4)$**
  Bias supply voltage pins to drive the LCD. Bias voltage is usually used as supply voltage source.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H", the shift register contents are transferred to 40-bit 4-level driver.
  When LOAD pin is set at "L", the last display output data (O_1 to O_{40}), which was transferred when LOAD pin was at "H", is held.

- **O_1 to O_{40}**
  Display data output pins which correspond to each data bit in the latch.
  One of the V_{DD}, V_2, V_3 or V_{EE} (V_4) is selected as a display driving voltage source according to the combination of latched data level and DF signal. Refer to the truth table.
  These pins should be connected to the SEGMENT side of the LCD panel.

Truth Table

Latched data	DF	Display data output level
H	H	V_{EE} (V_4)
	L	V_{DD}
L	H	V_3
	L	V_2