P2732A
32K (4K x 8) PRODUCTION EPROM

- **200 ns (P2732A-2) Maximum Access Time . . . HMOS*-E Technology**
- **Compatible with High-Speed 8 MHz iAPX 186 . . . Zero WAIT State**
- **Two Line Control**
- **Compatible with 12 MHz 8051 Family**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Low Active Current . . . 100 mA Max.**
- **int$_e$ligent Identifier™ Mode**
- **Fast 20 ms Programming Time**
- **TTL Compatible**

The Intel P2732A is a 5V-only, Electrically Programmable Read-Only Memory in a plastic package. One time programmable, it has been designed for high volume production environments where a programmable memory is required for flexibility. The standard P2732A access time is 250 ns with speed selection (P2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the P2732A allows the microprocessor to operate without the addition of WAIT states.

The P2732A is ideal for volume production environments where inventory and lead time risks occur for program codes. Inventoried in the unprogrammed state, the P2732A is programmed quickly and efficiently when the need to change code arises. Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and high reliability of the P2732A make it the ideal component for these production applications.

Using Intel's HMOS*-E technology, low power consumption combined with high speed data access are achieved. The maximum P2732A active current is 100 mA, while standby is only 35mA. The standby mode is selected by applying a TTL-high signal to the $\overline{CE}$ input.

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/V_{PP}
O_0-O_7	OUTPUTS

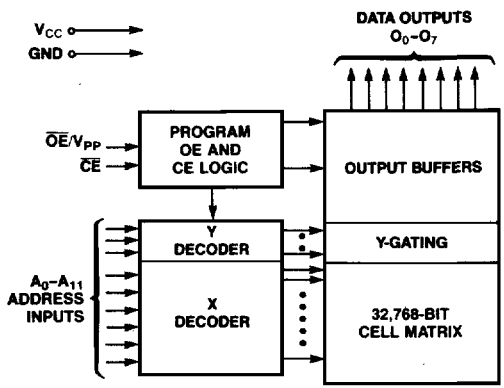

Figure 1. Block Diagram

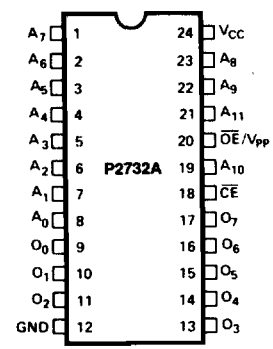

Figure 2. Pin Configuration

*HMOS is a patented process of Intel Corporation.

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to −0.3V
Voltage on Pin 22 with Respect to Ground ..... +13.5V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming ..... +22V to −0.3V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	P2732A/A-2/A-3/A-4
Operating Temperature Range	0°C–70°C
V_{CC} Power Supply[1,2]	5V ± 5%

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Conditions
		Min.	Typ.[1]	Max.		
I_{IL}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{CC1}[2]	V_{CC} Current (Standby)		15	35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2}[2]	V_{CC} Current (Active)		60	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{PP}[2]	V_{PP} Read Voltage	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25V$

A.C. CHARACTERISTICS

Symbol	Parameter	P2732A-2		P2732A		P2732A-3		P2732A-4		Units	Test Conditions†
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		70		100		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}[4]	$\overline{OE}$ High to Output Float	0	60	0	60	0	105	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

†A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times ..... ≤20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs ..... 0.8 and 2.0V
Outputs ..... 0.8 and 2.0V

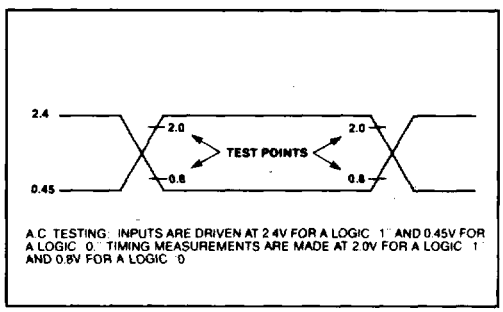
NOTES:

1. *Typical values are for $T_A = 25°C$ and nominal supply voltages.*
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven — *see timing diagram on page 4-18*
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.
4. *When programming the 2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.*

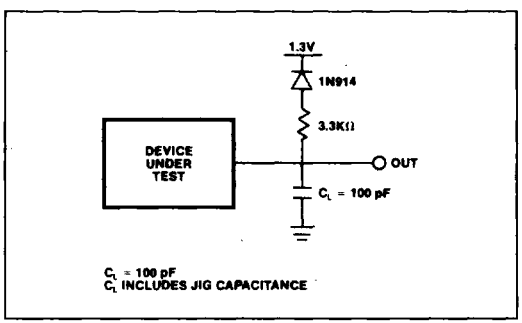
CAPACITANCE[2] (T_A = 25°C, F = 1 MHz)

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

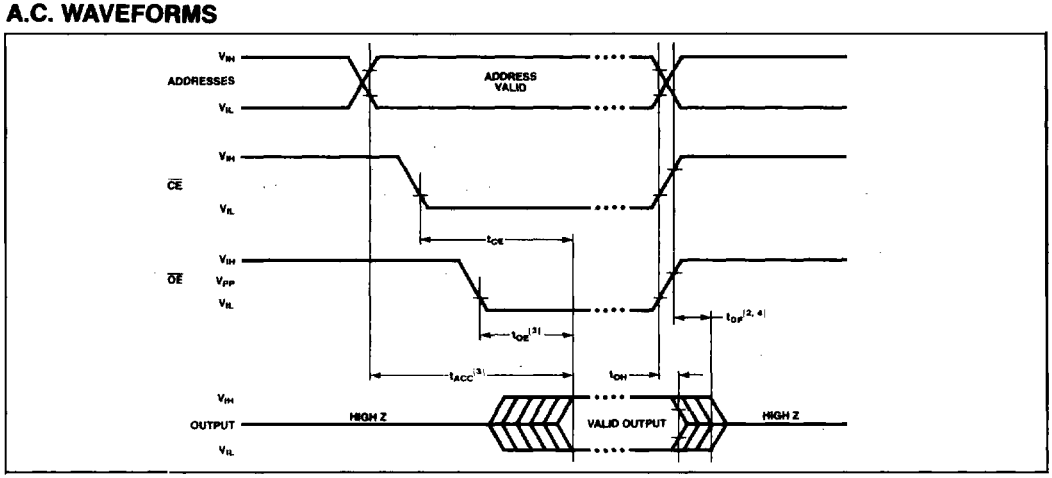
A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram on this page.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.
4. When programming the P2732A, a 0.1µF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

APPLICATIONS INFORMATION

Intel's P2732A is the result of a multi-year effort to make EPROMs more cost effective for production applications. The benefits of a plastic package enable the P2732A to be used for high volume production with lower profile boards and easier production assembly (no cover over UV transparent windows).

The reliability of plastic EPROMs is equivalent to traditional CERDIP packaging. The plastic is rugged and durable making it optimal for auto insertion and auto handling equipment. Design and testing ensures device programmability, data integrity, and impermeability to moisture.

Intel's Plastic EPROMs are designed for total compatibility with their CERDIP packaged predecessors. This encompasses quality, reliability, and programming. All Intel Plastic EPROMs have passed Intel's strict process and product reliability qualifications.

DEVICE OPERATION

The six modes of operation of the P2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming and 12V on A_9 for the int$_e$ligent Identifier™ mode. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	A_9 (22)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Int$_e$ligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	Code

NOTES:
1. X can be V_{IH} or V_{IL}
2. $V_H = 12V \pm 0.5V$

Read Mode

The P2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gather data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The P2732A has a standby mode which reduces the maximum active current from 100 mA to 35 mA. The P2732A is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) The lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 18) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

System Consideration

The power switching characteristics of HMOS-E EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's two line control and by use of properly selected decoupling capacitors. It is recommended that a 0.1μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

Application Note AP-72, which is available from Intel's Literature Department, describes microprocessor system implementation of the two-line control function on Intel's EPROMs.

PROGRAMMING

CAUTION: Exceeding 22V on Pin 20 ($\overline{OE}/V_{PP}$) will permanently damage the P2732A.

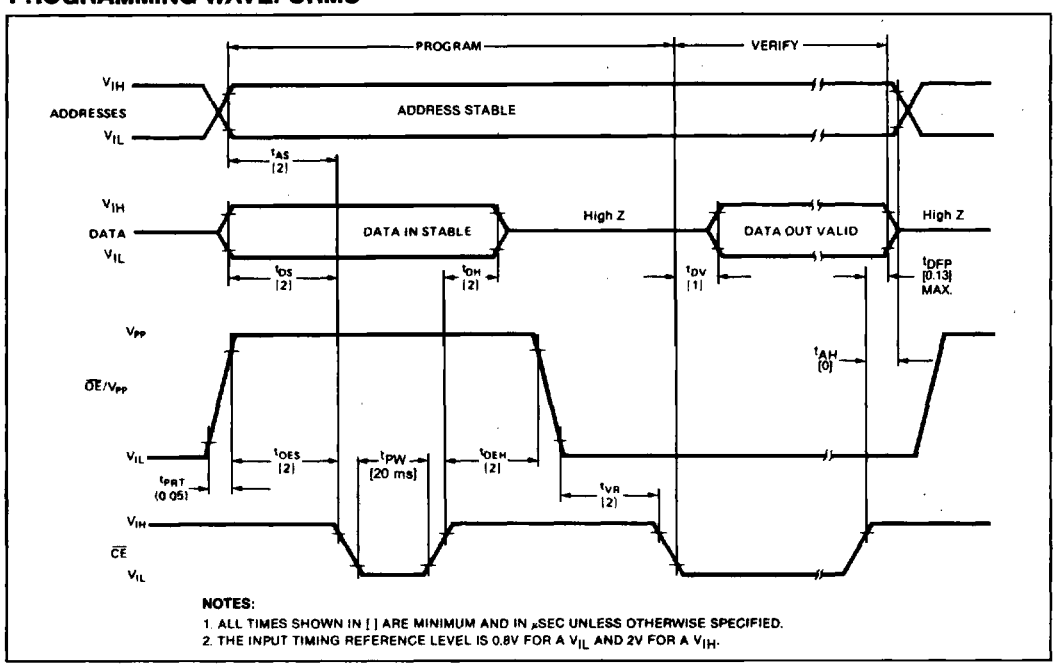
Initially all bits of the P2732A are in the "1" state. Data is introduced by selectively programming "0's" into the bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be present in the data word.

The P2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 20ms active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The P2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple P2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled P2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled P2732A.

PROGRAMMING WAVEFORMS



NOTES:
1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8V FOR A V_{IL} AND 2V FOR A V_{IH}.

PROGRAMMING[1]

D.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC}	V_{CC} Supply Current		85	100	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		$V_{CC}+1$	V	
I_{PP}	V_{PP} Supply Current			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$
V_{ID}	Ag *int*$_e$*ligent Identifier Voltage*	11.5		12.5	V	

A.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions†
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Not Driven	0		130	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
t_{PW}	$\overline{CE}$ Pulse Width During Programming	20	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

A.C. TEST CONDITIONS

Input Rise and Fall Time (10% to 90%) ... ≤ 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTE:
1. When programming the P2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

Program Inhibit

Programming of multiple P2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel P2732As may be common. A TTL low level pulse applied to a P2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that P2732A. A high level $\overline{CE}$ input inhibits the other P2732As from being programmed.

Verify

A verify (Read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 22) of the P2732A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 8) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1(A0 = V_{IH}) the device identifier code. For the Intel P2732A, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

Table 2: P2732A Int$_e$ligent Identifier™ Bytes

Identifier \ Pine	A_8 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01