Ordering number : EN6206

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SANYO Semiconductors

DATA SHEET

LA7137M — Monolithic Linear IC DVD Analog Video Output I/F IC

Overview

The LA7137M is a video output interface IC for DVD players and is optimal as the driver IC for DVD players that provide composite signal/S signal, component signal, and RGB signal video outputs.
Since this IC integrates a Y/C mixer on the same chip, the D/A converter composite output can be omitted. The LA7137M also integrates S1 and S2 DC voltage and D/A converter reference voltage generation on chip, allowing most components other than the drivers to be omitted.

Functions

- Clamps
- Amplifier
- 75Ω driver
- Y/C mixer
- S1 and S2 DC output
- D/A converter reference voltage output

Features

- Video signal-to-noise ratio : -80dB
- Frequency characteristics : flat to 10MHz
- Y/C time difference : less than 2ns
- Signal dynamic range : 170IRE.
- Can support all major signal types : composite/S signals, component signals, and baseband (RGB) signals. Furthermore, the IC input type can be switched by the system microcontroller (since the input capacitors are shared).
- Two 75Ω driver systems that can be independently muted by the system microcontroller.
- The clamp pulses required for component signal input are generated internally in the IC.
- Either of two amplifier gain levels, 8.5 and 6dB, can be selected.
- A built-in regulator circuit provides a stable DC voltage output that is independent of V_{CC} fluctuations.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		10.0	V
Allowable power dissipation	Pd max	Ta ≤ 75°C * Mounted on a board	525	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

* Only when mounted on a 114.3×76.1×1.6mm³ glass epoxy board

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Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		8.0	V
Operating supply voltage range	V_{CC} op		7.6 to 8.4	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 7.6 to 8.4V

Parameter	Symbol	Input signal	Test point	Conditions	Ratings			Unit
					min	typ	max	
Current drain 1	$I_{CC}1$			Video system current drain	14.3	17.9	21.5	mA
Current drain 2	$I_{CC}2$			75Ω driver current drain ; no signal	14.4	18.0	21.6	mA
(A) For a pin 10 (Y signal) input when composite/S selected								
Amplifier gain (low)	G_YM	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_YH	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	$C_{10}H$	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(B) For a pin 6 (chrominance signal) input when composite/S selected								
Amplifier gain (low)	G_CM	Sig.2	T17/19	The gain for a 711mVp-p 3.58MHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_CH	Sig.2	T17/19	The gain for a 544mVp-p 3.58MHz signal	7.38	7.6	7.81	dB
Chrominance signal input DC voltage	D_6H	Sig.2	T6	The T6 offset voltage for a 544mVp-p input	4.4	4.75	5.1	V
(C) For a pin 3 (composite signal) input when composite selected								
Amplifier gain (low)	G_SM1	Sig.3	T21/23	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_SH1	Sig.3	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	C_3H	Sig.3	T3	The T3 sync tip potential for a 761mVp-p input	4.0	4.35	4.7	V
(D) For a pins 6 and 10 (S signal) input when S is selected								
Amplifier gain (low)	G_SM2	Sig.1 Sig.2	T21/23	The gain for a 996mVp-p 100kHz signal or a 711mVpp 3.58kHz signal	4.92	5.27	5.61	dB
Amplifier gain (high)	G_SH2	Sig.1 Sig.2	T21/23	The gain for a 761mVp-p 100kHz signal or a 544mVpp 3.58kHz signal	7.25	7.6	7.94	dB
(E) The gain ratios between the different signals when composite is selected								
Y/chrominance amplifier gain ratio	ΔY_C	Sig.1 Sig.2	T13/15 T17/19	The ratio of the G_YH gain for (A) and the G_CH gain for (B)	-3	0	3	%
Y/composite amplifier gain ratio	ΔY_S1	Sig.1 Sig.3	T13/15 T21/23	The ratio of the G_YH gain for (A) and the G_SH1 gain for (C)	-3	0	3	%
Chrominance/composite amplifier gain ratio	ΔC_S1	Sig.2 Sig.3	T17/19 T21/23	The ratio of the G_CH gain for (B) and the G_SH1 gain for (C)	-3	0	3	%
(F) The gain ratios between the different signals when S is selected								
Y/S amplifier gain ratio	ΔY_S2	Sig.1 Sig.2	T13/15 T21/23	The ratio of the G_YH gain for (A) and the G_SH2 gain for (D)	-4.5	0	4.5	%
Chrominance/S amplifier gain ratio	ΔC_S2	Sig.1 Sig.2	T17/19 T21/23	The ratio of the G_CH gain for (B) and the G_SH2 gain for (D)	-4.5	0	4.5	%
(G) The pin 10 (Y signal) input when component is selected								
Amplifier gain (low)	G_YM	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_YH	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Y input clamp voltage	$C_{10}H$	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(H) The pin 6 (B-Y or R-Y signal) input when component is selected								
Amplifier gain (low)	G_NM	Sig.4	T17/19	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_NH	Sig.4	T17/19	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input pedestal clamp voltage	P_6H	Sig.4	T6	The T6 pedestal potential for a 761 mVp-p input	4.4	4.75	5.1	V
Amplifier gain (low)	G_NM	Sig.4	T21/23	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB

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Parameter	Symbol	Input signal	Test point	Conditions	Ratings			Unit
					min	typ	max	
(I) The pin 3 (B-Y or R-Y signal) input when component is selected								
Amplifier gain (high)	G_NH	Sig.4	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input pedestal clamp voltage	P_3H	Sig.4	T3	The T3 pedestal potential for a 761 mVp-p input	4.4	4.75	5.1	V
(J) The gain ratios between the different signals when component is selected								
Y/component amplifier gain ratio 1	ΔY1	Sig.1 Sig.4	T13/15 T17/19	The ratio of the G_YH gain for (E) and the G_NH gain for (F)	-3	0	3	%
Y/component amplifier gain ratio 2	ΔY2	Sig.1 Sig.4	T13/15 T21/23	The ratio of the G_YH gain for (E) and the G_NH gain for (G)	-3	0	3	%
Component amplifier gain ratio	ΔN	Sig.4 Sig.4	T17/19 T21/23	The ratio of the G_NH gain for (F) and the G_NH gain for (G)	-3	0	3	%
(K) The pin 10 (RGB signal) input when baseband is selected								
Amplifier gain (low)	G_BM	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_BH	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input clamp voltage	$C_{10}H$	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(L) The pin 6 (RGB signal) input when baseband is selected								
Amplifier gain (low)	G_BM	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_BH	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input clamp voltage	C_6H	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	4.0	4.35	4.7	V
(M) The pin 3 (RGB signal) input when baseband is selected								
Amplifier gain (low)	G_BM	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G_BH	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Input clamp voltage	C_3H	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	4.0	4.35	4.7	V
(N) The gain ratios between the different signals when baseband is selected								
Baseband amplifier gain ratio 1	ΔB1	Sig.1 Sig.1	T13/15 T17/19	The ratio of the G_BH gain for (I) and the G_BH gain for (J)	-3	0	3	%
Baseband amplifier gain ratio 2	ΔB2	Sig.1 Sig.1	T13/15 T21/23	The ratio of the G_BH gain for (I) and the G_BH gain for (K)	-3	0	3	%
Baseband amplifier gain ratio 3	ΔB3	Sig.1 Sig.1	T17/19 T21/23	The ratio of the G_BH gain for (J) and the G_BH gain for (K)	-3	0	3	%
(O) Gain frequency characteristics (Common to all modes and input signals other than Y/C mixed mode)								
6MHz low-pass filter attenuation	F_Y6	Sig.1	T13/15	The difference between G_YH and the gain for a 761mVp-p, 6MHz input	-0.5	0	+0.5	dB
10MHz low-pass filter attenuation	F_Y10	Sig.1	T13/15	The difference between G_YH and the gain for a 761mVp-p, 10MHz input	-0.5	0	+0.5	dB
(P) DC voltage when output muting applied (Common to all modes)								
Pin 13 voltage	V_{13}		T13		3.7	4.05	4.4	V
Pin 15 voltage	V_{15}		T15		3.7	4.05	4.4	V
Pin 17 voltage	V_{17}		T17		3.9	4.25	4.6	V
Pin 19 voltage	V_{19}		T19		3.9	4.25	4.6	V
Pin 21 voltage	V_{21}		T21		3.9	4.25	4.6	V
Pin 23 voltage	V_{23}		T23		3.9	4.25	4.6	V
(Q) Output DC voltage characteristics								
D/A converter reference voltage	V_{DA}		T12	When driving an 800μA load current	3.2	3.4	3.6	V
4 : 3 output mode DC	V_{43}		T16	In 4 : 3 control mode (no load)	0	0.01	0.35	V
Letterbox output DC	V_{LB}		T16	In letterbox control mode (when driving a 500μA load current)	2.05	2.2	2.35	V
Squeezed output DC	V_{SQ}		T16	In squeeze control mode (when driving a 500μA load current)	4.4	4.7	5.0	V

Note : The amplifier gain and amplifier gain ratios are the values when the components shown in the test circuit diagram are all connected.

Switching Characteristics ("-" indicates OK under all conditions)

Symbol	Control voltage (unit: V)						Switching conditions	
	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
$I_{CC}1$	0	0	3.3	0	3.3	3.3	ON	ON
$I_{CC}2$	0	0	3.3	0	3.3	3.3	ON	ON
(A) For a pin 10 (Y signal) input when composite/S selected								
$G_{Y}M$	0/3.3	0	-	-	0	3.3	ON/OFF	ON
$G_{Y}H$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
$C_{10}H$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(B) For a pin 6 (chrominance signal) input when composite/S selected								
$G_{C}M$	0/3.3	0	-	-	0	3.3	ON/OFF	ON
$G_{C}H$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
$C_{6}H$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(C) For a pin 3 (composite signal) input when composite selected								
$G_{S}M1$	0/3.3	0	-	-	0	3.3	ON/OFF	ON
$G_{S}H1$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
$C_{3}H$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(D) For a pins 3 (S signal) input when S is selected								
$G_{S}M2$	0/3.3	0	-	-	0	3.3	ON/OFF	ON
$G_{S}H2$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(E) The gain ratios between the different signals when composite is selected								
ΔY_{C}	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
$\Delta Y_{S}1$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
$\Delta C_{S}1$	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(F) The gain ratios between the different signals when S is selected								
$\Delta Y_{S}2$	0/3.3	0	-	-	3.3	0	ON/OFF	ON
$\Delta C_{S}2$	0/3.3	0	-	-	3.3	0	ON/OFF	ON
(G) The pin 10 (Y signal) input when component is selected								
$G_{Y}M$	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON
$G_{Y}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
$C_{10}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
(H) The pin 6 (B-Y or R-Y signal) input when component is selected								
$G_{N}M$	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON
$G_{N}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
$P_{6}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
(I) The pin 3 (B-Y or R-Y signal) input when component is selected								
$G_{N}M$	0/3.3	3.3	-	-	0	3.3	ON/OFF	ON
$G_{N}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
$P_{3}H$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
(J) The gain ratios between the different signals when component is selected								
$\Delta Y1$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
$\Delta Y2$	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
ΔN	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
(K) The pin 10 (RGB signal) input when baseband is selected								
$G_{B}M$	0/3.3	-	-	-	0	3.3	ON/OFF	OFF
$G_{B}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
$C_{10}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
(L) The pin 6 (RGB signal) input when baseband is selected								
$G_{B}M$	0/3.3	-	-	-	0	3.3	ON/OFF	OFF
$G_{B}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
$C_{6}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
(M) The pin 3 (RGB signal) input when baseband is selected								
$G_{B}M$	0/3.3	-	-	-	0	3.3	ON/OFF	OFF
$G_{B}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
$C_{3}H$	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF

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Symbol	Control voltage (unit: V)						Switching conditions	
	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
(N) The gain ratios between the different signals when baseband is selected								
ΔB1	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
ΔB2	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
ΔB3	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
(O) Gain frequency characteristics (Common to all modes and input signals other than Y/C mixed mode)								
F_Y6	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
F_Y10	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(P) DC voltage when output muting applied (Common to all modes)								
V_{13}	0	-	-	-	0/3.3	0/3.3	ON	-
V_{15}	3.3	-	-	-	0/3.3	0/3.3	ON	-
V_{17}	0	-	-	-	0/3.3	0/3.3	ON	-
V_{19}	3.3	-	-	-	0/3.3	0/3.3	ON	-
V_{21}	0	-	-	-	0/3.3	0/3.3	ON	-
V_{23}	3.3	-	-	-	0/3.3	0/3.3	ON	-
(Q) Output DC voltage characteristics								
V_{DA}	-	-	-	-	0/3.3	0/3.3	-	-
V_{43}	-	-	0	0	0/3.3	0/3.3	-	-
V_{LB}	-	-	0	3.3	0/3.3	0/3.3	-	-
V_{SQ}	-	-	3.3	0	0/3.3	0/3.3	-	-

Control Pin Functions

Pin No.	Pin state	Low	Open	High
1	Pin voltage	0 to 0.6V	1.55 to 1.75V	2.7 to 5V
	75Ω driver muting	13, 17, 21 muted	Not muted	15, 19, 23 muted
2	Pin voltage	0 to 0.6V	1.55 to 1.75V	2.7 to 5V
	Signal input type switching	Composite/S mode	Baseband mode	Component mode
11	Pin voltage	0 to 1V		2.7 to 8V (note)
	Amplifier gain switching	6dB		8.5dB
22	Pin voltage	0 to 1V		2.7 to 8V (note)
	Y/C mixer control	Y/C mixed mode		Composite mode

Note : Never apply a voltage higher than the V_{CC} voltage at pins 9 and 20 to pin 11 or pin 22.

* : Y/C mixed mode is illegal in modes other than composite/S mode.

* : In composite mode, use pin 6 to input the chrominance signal capacitor-coupled, pin 3 for the clamped composite signal, and pin 10 for the clamped Y signal. However, in S mode, pin 3 will have no input.
In component mode, pins 3 and 6 will be pedestal clamped B-Y and R-Y signals, respectively, while pin 10 will be the clamped Y signal input.
In baseband mode, pins 3, 6, and 10 are all clamped inputs, for the RGB signals, respectively.
Pins 11 and 22 must never be left open.

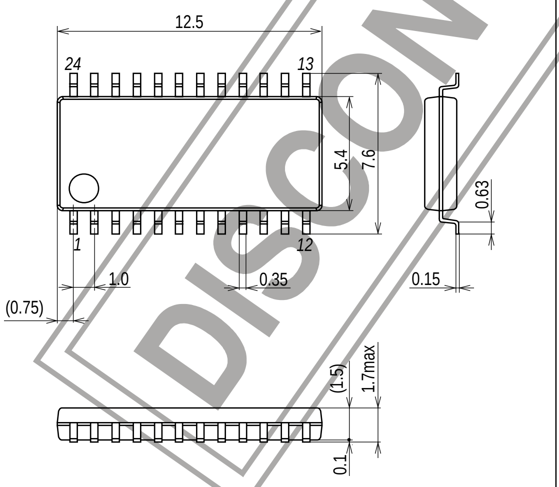
Pin 4	Pin 5	Pin 16 output DC
0 to 1V	0 to 1V	Low (0V) → 4 : 3 mode
0 to 1V	2.6 to 5V	Middle (2.5V) → Letterbox mode
2.6 to 5V	0 to 1V	High (5V) → Squeezed mode
2.6 to 5V	2.6 to 5V	Illegal values

Design Guaranteed Items (at Ta = 25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<Modes Other than Y/C Mixed Mode>						
Inter-channel crosstalk	CT	Input an f = 4MHz signal to another channel such that the capacitor-coupled output becomes 1Vp-p. Measure the amplitude of the 4MHz component on the monitored channel. This parameter is stipulated to be the ratio of that level with the amplitude of the 4MHz component on that other channel.		-65	-60	dB
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11. Measure the signal-to-noise ratio in the output signal.		-80	-78	dB
Differential gain	DG	Input a standard 1Vp-p staircase signal (color) and leave pin 11 open. Measure the differential gain in the output signal. Note that the components shown in the test circuit diagram for this parameter must be inserted at this time.		0.5	2	%
Differential phase	DP	Input a standard 1Vp-p staircase signal (color) and leave pin 11 open. Measure the differential phase in the output signal. Note that the components shown in the test circuit diagram for this parameter must be inserted at this time.	-1	0	1	dB
<Y/C Mixed Mode>						
Inter-channel crosstalk	CT	Input an f = 4MHz signal to another channel such that the capacitor-coupled output becomes 1Vp-p. Measure the amplitude of the 4MHz component on the monitored channel. This parameter is stipulated to be the ratio of that level with the amplitude of the 4MHz component on that other channel.		-65	-60	dB
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11. Measure the signal-to-noise ratio in the output signal.		-74	-72	dB
Differential gain	DG	Input a standard 761mVp-p staircase signal (color) and apply a 3.3V level to pin 11. Measure the differential gain in the output signal. Note that the components shown in the test circuit diagram for this parameter must be inserted at this time.		4	5.5	%
Differential phase	DP	Input a standard 761mVp-p staircase signal (color) and apply a 3.3V level to pin 11. Measure the differential gain in the output signal. Note that the components shown in the test circuit diagram for this parameter must be inserted at this time.	-1	0.5	1.5	dB

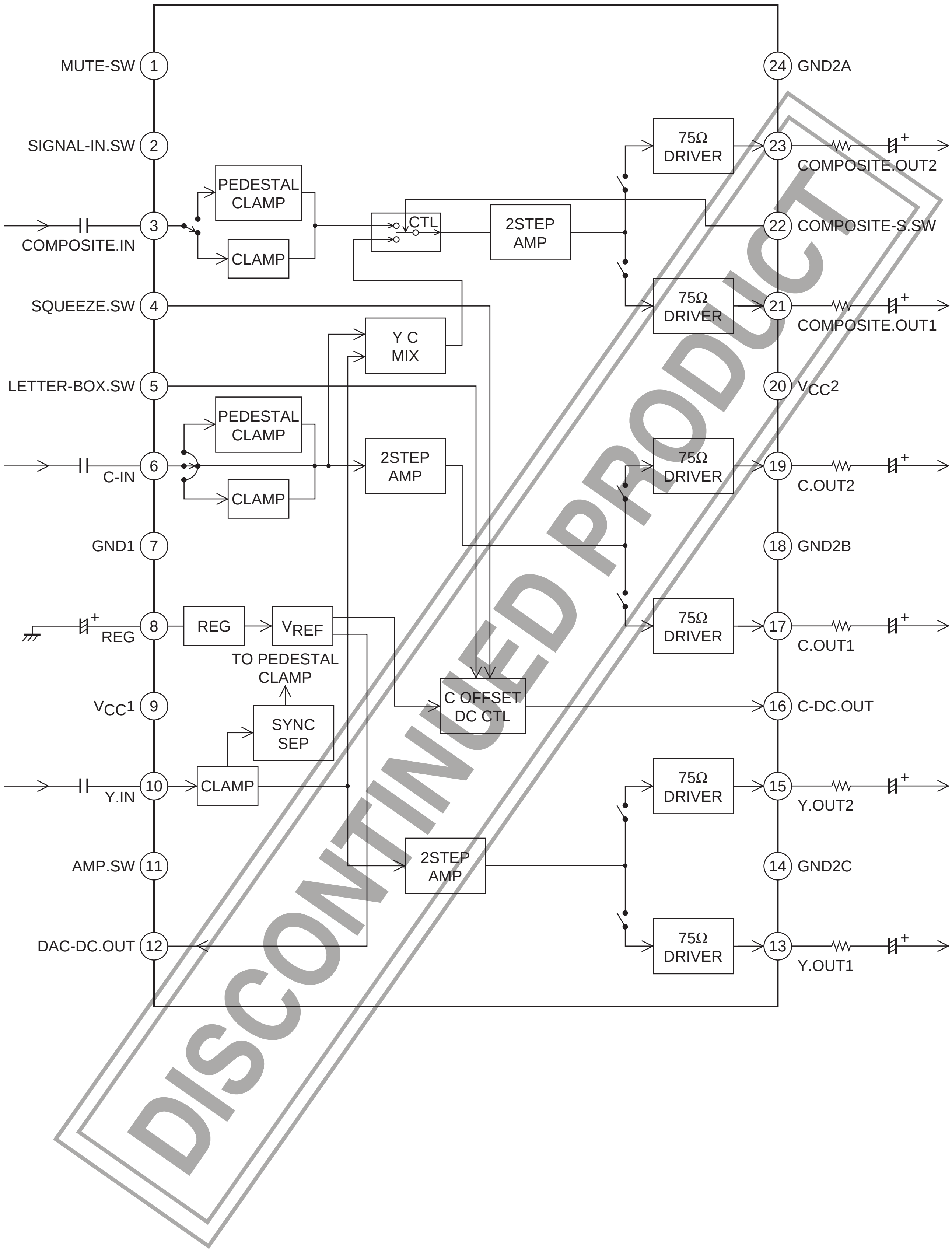
Package Dimensions

unit : mm (typ)
3112B



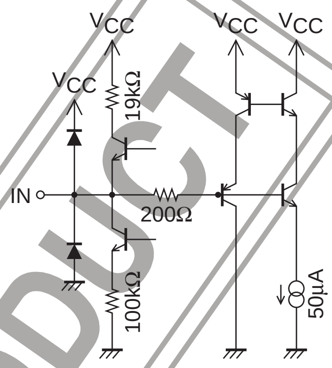
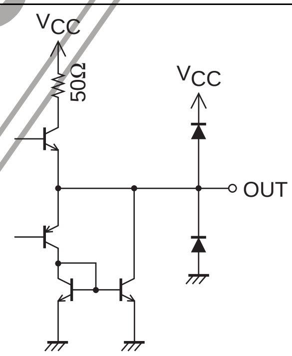
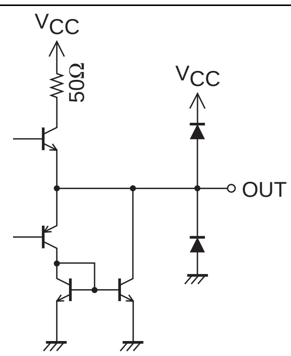
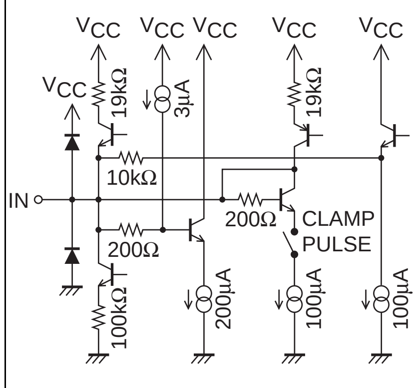
SANYO : MFP24S(300mil)

Block Diagram



Pin Functions

For more information on the pin functions, see the I/O circuit diagrams, and for an operating description, see the block diagram.
Note that the data shown below consists of typical values and that detailed ratings are provided in the Electrical Characteristics.

Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
10	Y-IN	I	4.2V	Clamp form	Input pin for either the Y or a baseband signal. This pin is used for the Y signal for composite/S and component signal input, and for one of the RGB signals with sync. Keyed clamping (clamping at the lowest point in the signal, that is, at the sync tip) is applied whichever signal is input. If a component signal is input, sync separation is performed and a clamp pulse for pedestal clamping is produced. The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	
13	Y.OUT1	O	2.7V	11.6Ω	75Ω driver output for the signal input to pin 10. The pin 10 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	
15	Y.OUT2	O	2.7V	11.6Ω	75Ω driver output for the signal input to pin 10. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the 75Ω driver.	
6	C-IN	I	4.8V	10kΩ	Input pin for chrominance, component, and baseband signals. The chrominance signal must be input to this pin when a composite/S signal input is used. The signal must be capacitor coupled. The B-Y or R-Y signal must be input to this pin when a component signal is input. The signal is clamped at the pedestal level. Any one of the RGB with sync signals must be input to this pin when a baseband signal is input. Keyed clamping will be applied to the signal. The capacitor coupled or clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	

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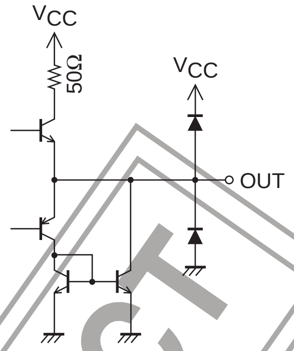
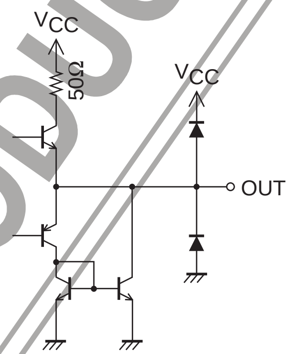
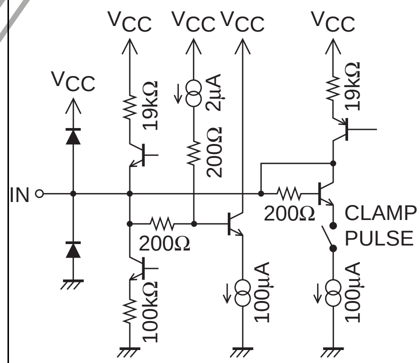
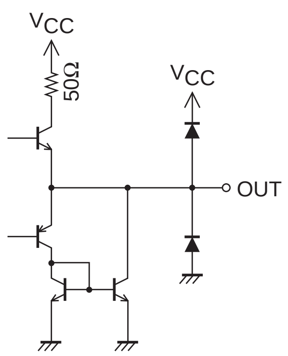
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
17	C.OUT1	O	3.9V	11.6kΩ	75Ω driver output for the signal input to pin 6. The pin 6 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	
19	C.OUT2	O	3.9V	11.6kΩ	75Ω driver output for the signal input to pin 6. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the 75Ω driver.	
3	COMPOSITE.IN	I	4.5V	Clamp form	Input pin for composite, component, and baseband signals. If a composite signal is input, it must be input to this pin, and if a baseband signal is input, any one of the RGB with sync signals must be input to this pin. Keyed clamping will be applied to the signal. For S signal input, this pin must be dropped to ground. For component signal input, input either the B-Y or R-Y signal to this pin. The signal will be clamped at the pedestal level. The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	
21	COMPOSITE. OUT1	O	3.57V	11.6Ω	75Ω driver output for the signal input to pin 3. The pin 3 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	

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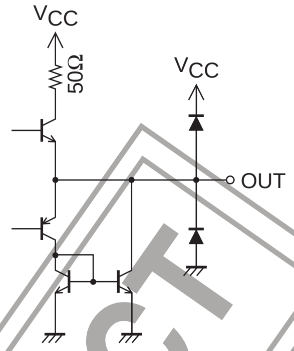
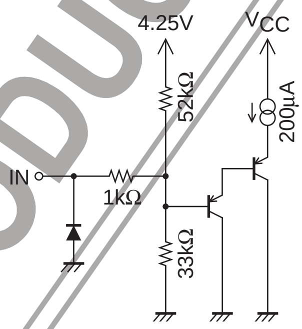
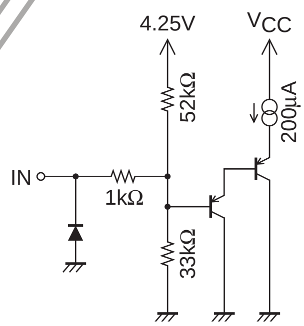
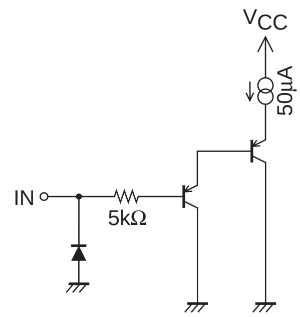
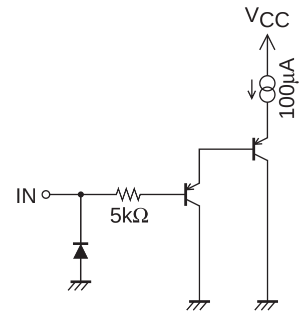
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
23	COMPOSITE. OUT2	O	3.57V	11.6Ω	75Ω driver output for the signal input to pin 3. Of the pin 3 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the 75Ω driver.	
1	MUTE-SW	I	1.7V	21kΩ	Controls the muting applied to the output signals. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	
2	SIGNAL-IN.SW	I	1.7V	21kΩ	Switches the input circuit types of pins 3 and 6 to match the type of the input signal. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	
4	SQUEEZE.SW	I	2.40V	9.0GΩ	Inputs squeeze control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	
5	LETTER-BOX.SW	I	2.43V	8.1GΩ	Inputs letterbox control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	

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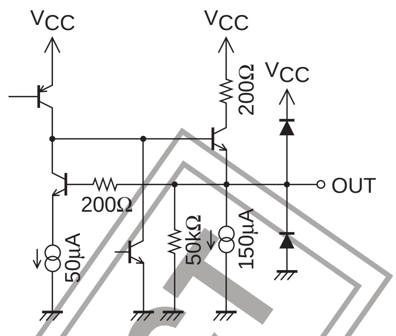
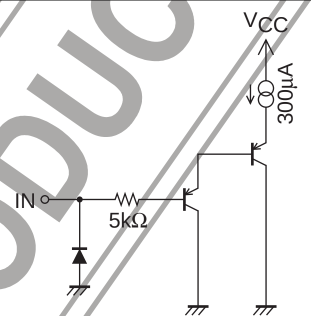
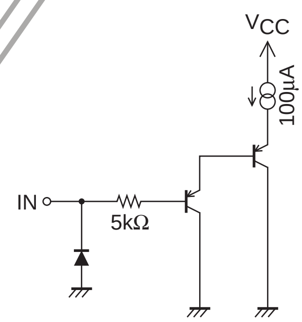
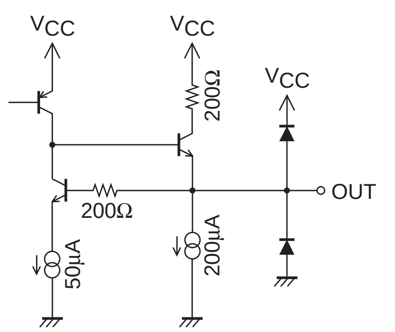
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
16	C-DC.OUT	O	4.7V	4.1Ω	The LA7137M creates, and outputs from this pin, a stabilized DC voltage based on the control information input to pins 4 and 5. This pin outputs a low level (0V) for 4 : 3 mode, a middle level (2.2V) for letterbox mode, and a high level (5V) for squeeze mode. A 10kΩ resistor must be inserted to superimpose the DC voltage output from pin 17 on the capacitor coupled chrominance output. (See the application circuit diagram.)	
11	AMP-SW	I	2.4V	9.0GΩ	Control pin that switches the amplifier gain to match the amplitude of the input signal. This pin's input level can be switched between V_{CC} and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	
22	COMPOSITE-S.SW	P	2.4V	9.0GΩ	Controls the on/off state of the Y/C mixer. When using a D/A converter that omits the composite output, the Y/C mixer must be turned on. At the same time as mixing the Y signal input to pin 10 with the chrominance signal input to pin 6, pin 3 will be dropped to ground. When pin 2 control specifies a signal type other than composite/S signal, this pin must be tied high. This pin's input level can be switched between V_{CC} and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	
12	DAC-DC.OUT	O	3.4V	4.0Ω	Outputs a DC reference voltage for use by a D/A converter. In particular, it outputs a 3.3V level. This reference voltage is unaffected by V_{CC} fluctuations or temperature and can be used in conjunction with a resistor divider to produce the DC level required by the D/A converter.	
7	GND1	P	0V		Ground for systems other than the 75Ω driver system.	

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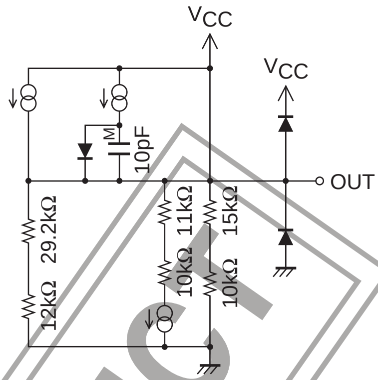
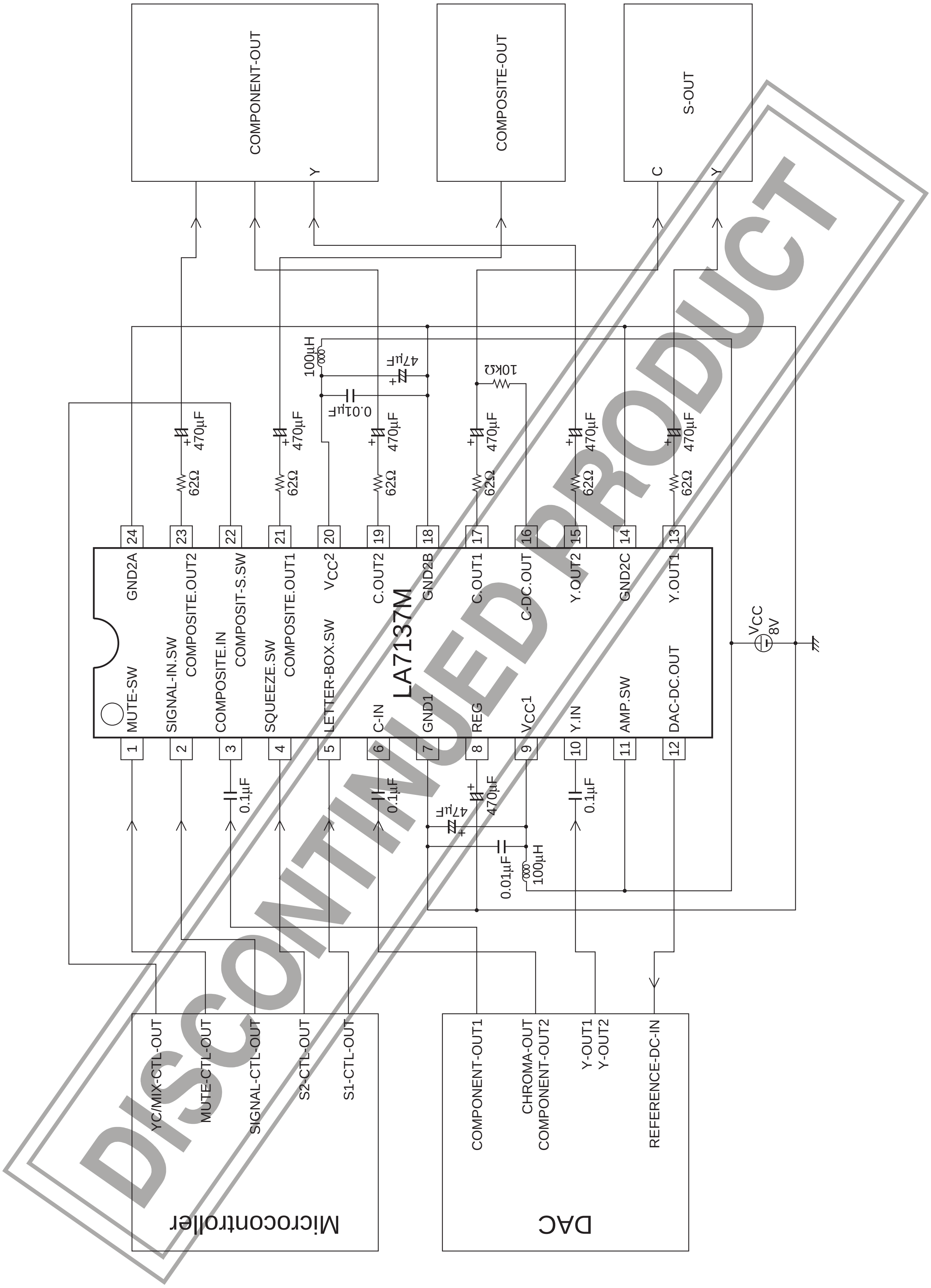
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
8	REG	O	4.35V	1.5kΩ	External pin for the regulator circuit that creates the IC internal reference voltage. Since the IC internal noise is influenced by the stability of this regulator, we recommend connecting a 470μF capacitor to this pin to if assuring a -80dB signal-to-noise ratio is required.	
9	$V_{CC}1$	P	8V		V_{CC} (8V applied) for systems other than the 75Ω driver system. Insert a 47μF capacitor between this pin and pin 7.	
20	$V_{CC}2$	P	8V		V_{CC} (8V applied) for the 75Ω driver system. Insert a 47μF capacitor between this pin and pin 14, 18, or 24. The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
14	GND2C	P	0V		Ground for the 75Ω driver system (pin 13 or 15). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
18	GND2B	P	0V		Ground for the 75Ω driver system (pin 17 or 19). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
24	GND2A	P	0V		Ground for the 75Ω driver system (pin 21 or 23). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	

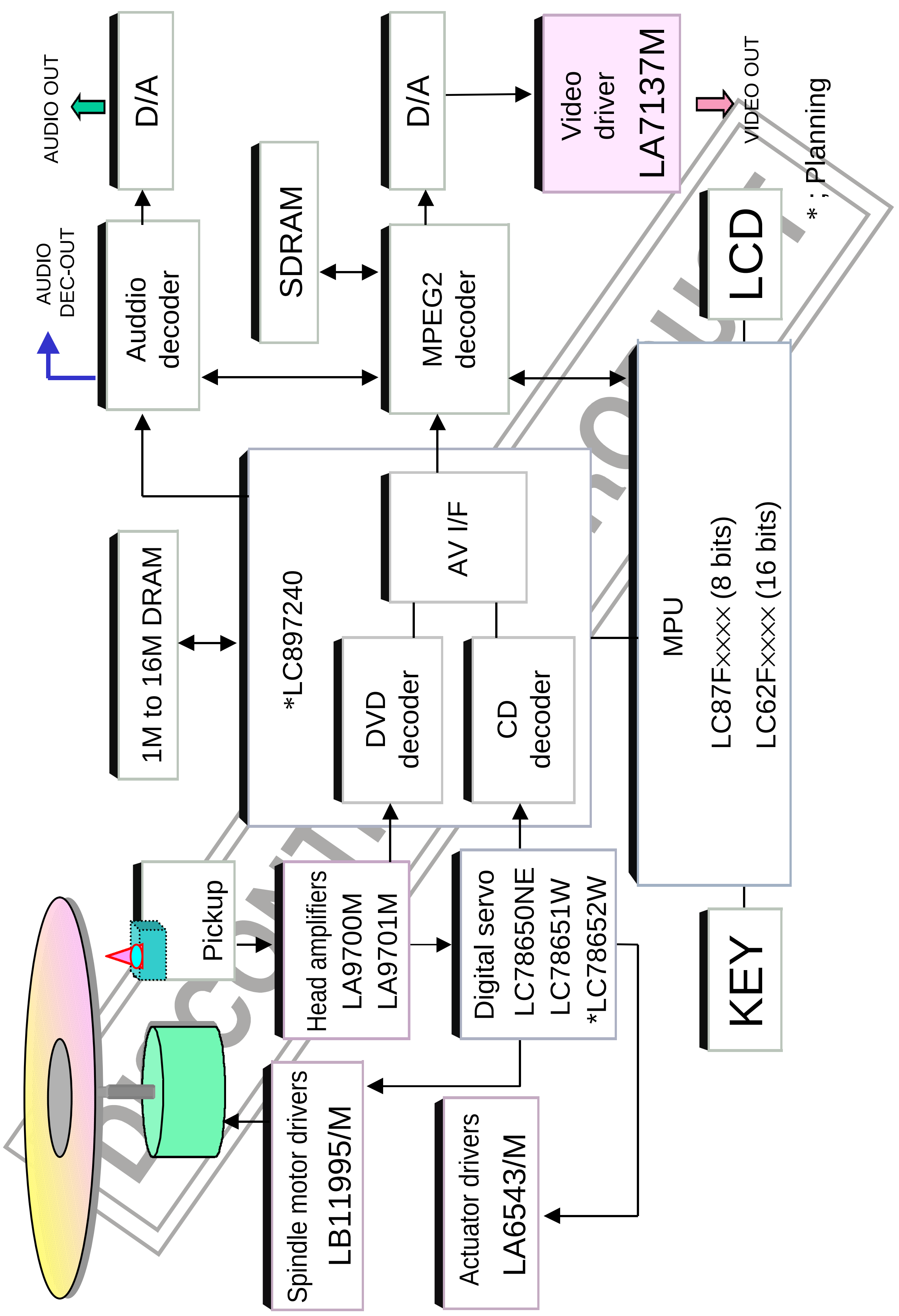
Sample Application Circuit

Single composite/S signal plus single component signal application using a single D/A converter

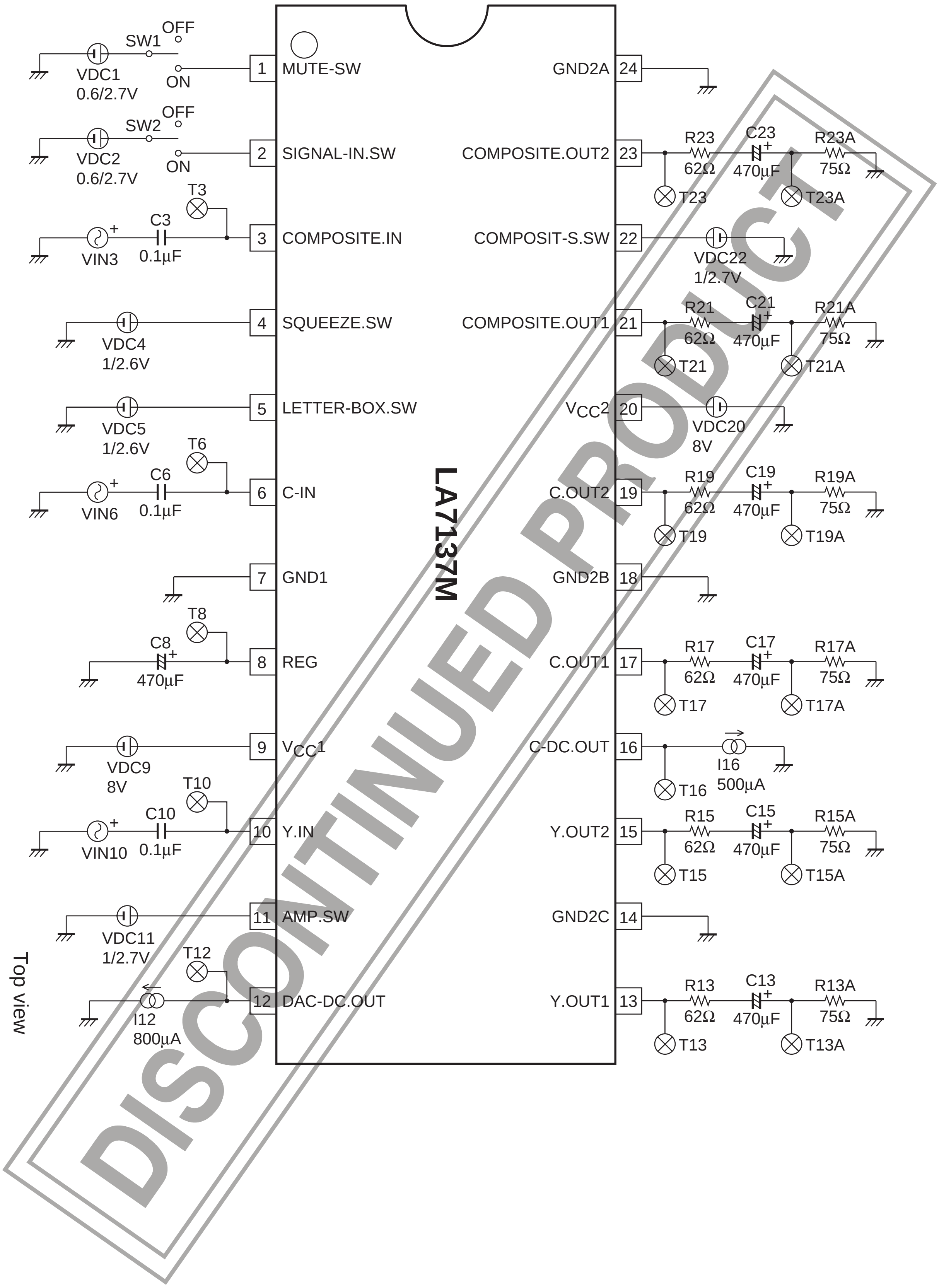


Application circuit diagram for end product that provides one output system each for composite/S and component outputs and the D/A converter output pin is shared between the S signal and the component signal systems. The muting control can be used to switch between the composite/S and component outputs.
The system microcontroller must be programmed to turn the Y/C mixer off when the component signal system is used.

DVD Video Player System Block Diagram

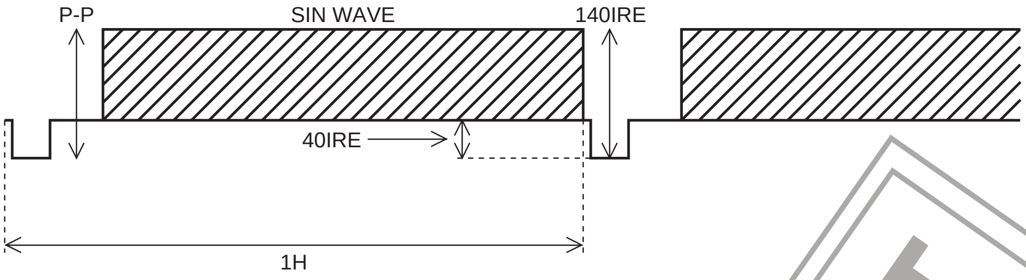


Test Circuit

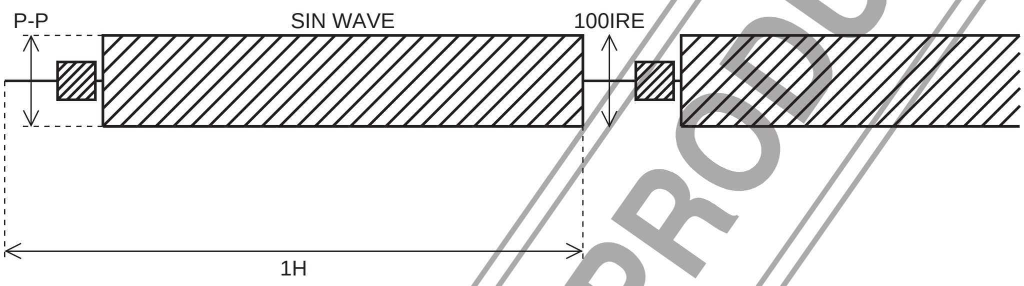


Input Signal for Test

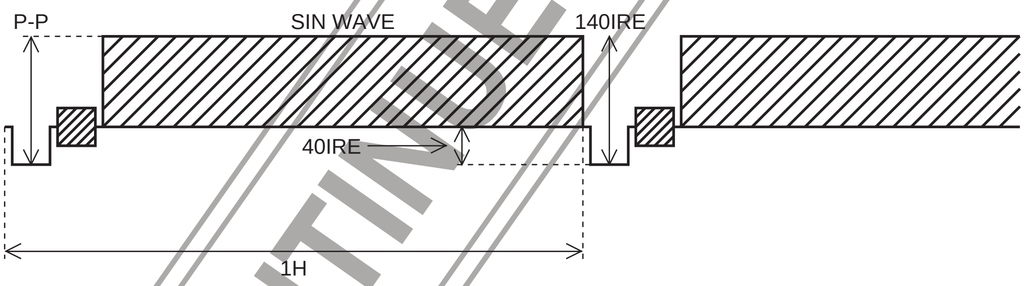
SIG.1



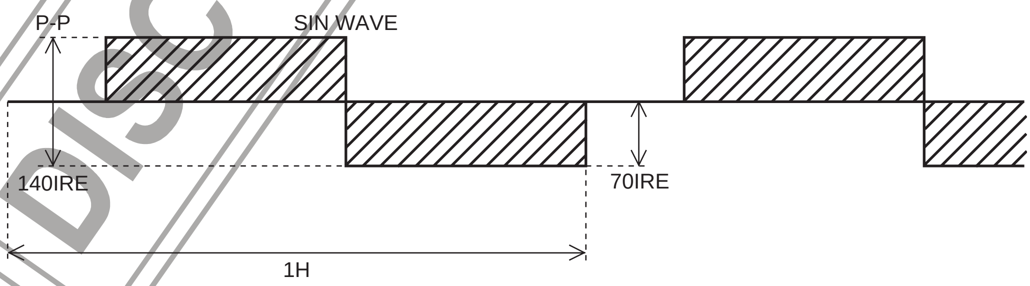
SIG.2



SIG.3



SIG.4



This catalog provides information as of November, 2006. Specifications and information herein are subject to change without notice.