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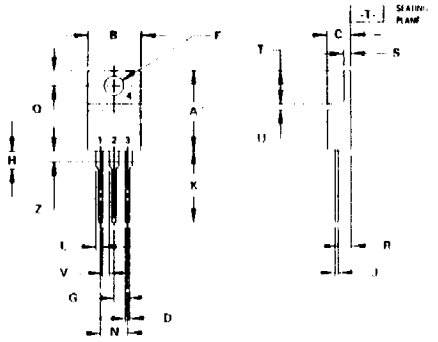
MTP2N80

Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS



STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

TO-220AB

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15		0.045	
Z		2.04		0.080

MAXIMUM RATINGS

Rating	Symbol		Unit
Drain-Source Voltage	V_{DSS}	800	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	800	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-repetitive (t_p ≤ 50 μs)	V_{GSM}	± 40	Vpk
Drain Current — Continuous	I_D	2	Adc
— Pulsed	I_{DM}	7	
Total Power Dissipation @ T_C = 25°C	P_D	75	Watts
Derate above 25°C		0.6	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient — TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	800	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	20 16	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	33 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%