CMOS 8-BIT MICROCONTROLLERS
TMP91P642N/TMP91P642F

1. OUTLINE AND CHARACTERISTICS

The TMP91P642 is a system evaluation LSI having a built in One-Time PROM for TMP91C642A.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP91C642A by programming to the internal PROM.

PARTS No.	ROM	RAM	PACKAGE	ADAPTER SOCKET NO.
TMP91P642N	OTP 16384×8 bit	320×8 bit	64-SDIP	BM1144
TMP91P642F			64-QFP	BM1145

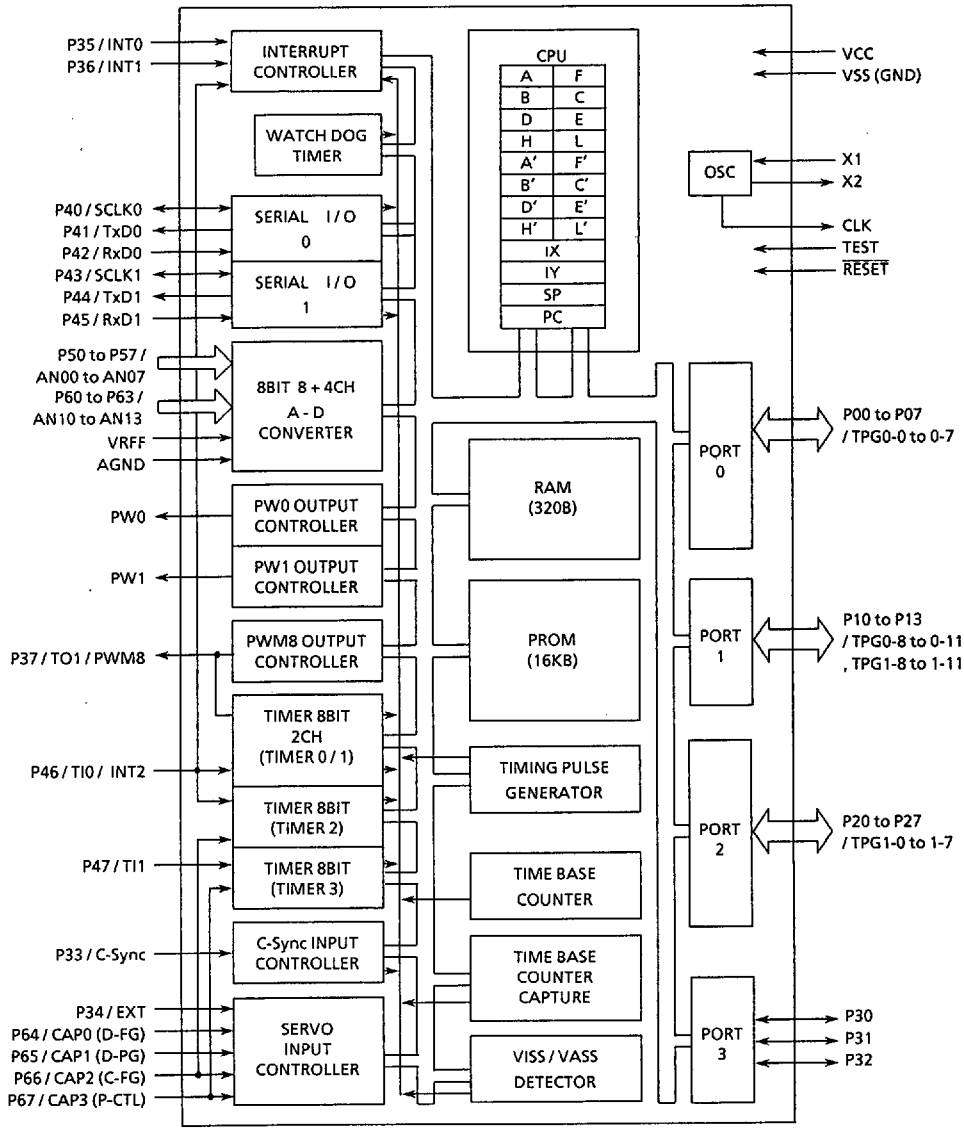


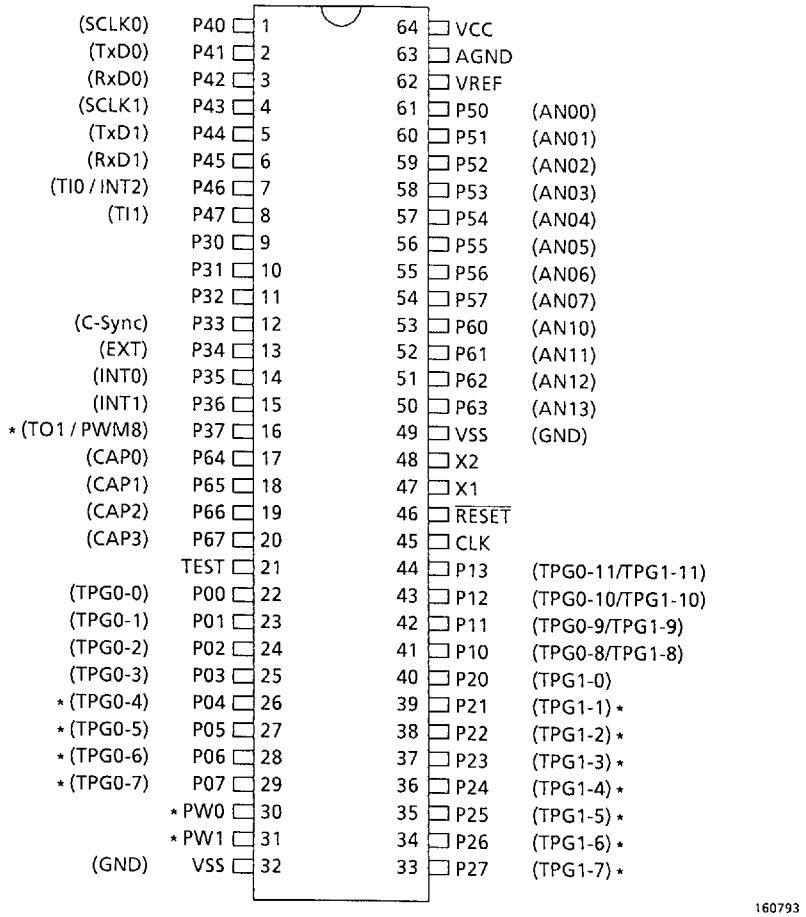
Figure 1 TMP91P642 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

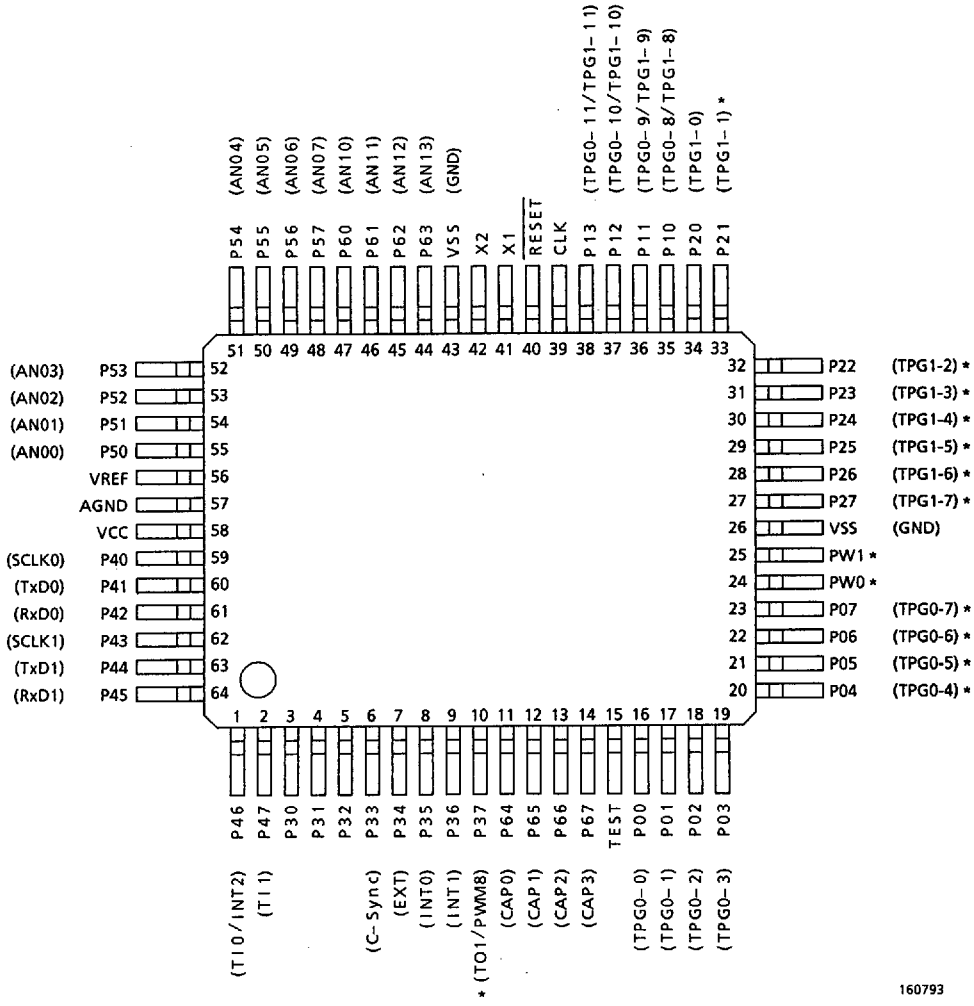
Figure 2.1 (1) shows pin assignment of the TMP91P642N.



*) open drain pin

Figure 2.1 (1) Pin Assignment (Shrink DIP package)

Figure 2.1 (2) shows pin assignment of the TMP91P642F.



*) open drain pin

Figure 2.1 (2) Pin Assignment (Flat package)

2.2 Pin Names and Functions

The TMP91P642 has MCU mode and PROM mode.

(1) The functions of MCU mode are summarized in Table 2.2 (1). (TMP91C642A and the TMP91P642 are pin compatible. However, the CLK pin of the TMP91C642A is always pulled up.)

Table 2.2 (1) Pin Names and Functions (1/3)

Pin name	Number of pins	I/O or 3-state	Function
P00/TPG0-0 to P07/TPG0-7	8	I/O, 3-state* (P04 to P07 are open drain output pins.)	Port 0 : 8-bit I/O port. I/O specifiable in units of bytes.
			Timing pulse generator (TPG) output: Can also be used as TPG0-0 to TPG0-7 output pins. *P00 only can be set to 3-state by internal signals to TPG0-15.
P10/TPG0-8 /TPG1-8 to P13/TPG0-11 /TPG1-11	4	I/O, 3-state*	Port 1 : 4-bit I/O port. I/O specifiable in units of bits.
			Timing pulse generator (TPG) output: Can also be used as TPG0-8 to TPG0-11 / TPG1-8 to TPG1-11 output pins. *P10 only can be set to 3-state by internal signals to TPG0-14/TPG1-14.
P20/TPG1-0 to P27/TPG1-7	8	I/O, 3-state* (P21 to P27 are open drain output pins.)	Port 2 : 8-bit I/O port. I/O specifiable in units of bits.
			Timing pulse generator (TPG) output: Can also be used as TPG1-0 to TPG1-7 output pins. *P20 only can be set to 3-state by internal signals to TPG1-15.
P30 to P32	3	I/O	Port 3 : 3-bit I/O port. I/O specifiable in units of bits.
P33 / C-Sync	1	I/O	Port 3 : 1-bit I/O port. I/O specifiable.
			Composite sync input
P34 / EXT	1	I/O	Port 3 : 1-bit I/O port. I/O specifiable.
			Servo signal trigger input
P35 / INT0	1	Input	Port 3 : 1-bit input port.
			Interrupt request pin 0 : Level and rising edge are programmable.
P36 / INT1	1	Input	Port 3 : 1-bit input port.
			Interrupt request pin 1 : at rising edge.
P37 / PWM8 / TO1	1	Open drain output	Port 3 : 1-bit output port.
			Motor control output : PWM8 output
			Timers 0 and 1 output : timer 0 and 1 output.

(Note) * : Only 1 put can be set to the 3-state.

Table 2.2 (1) Pin Names and Functions (2/3)

Pin name	Pin name	I/O or 3-state	Function
P40 / SCLK0, P43 / SCLK1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial clock I/O 0 and 1
P41 / TxD0, P44 / TxD1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial send data 0 and 1
P42 / RxD0, P45 / RxD1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial receive data 0 and 1
P46 / TI0 / INT2	1	I/O	Port 4 : 1-bit I/O port. I/O specifiable.
			Timer 0 / timer 2 count input
			Interrupt request pin 2 : at rising edge ⌐
P47 / TI1	1	I/O	Port 4 : 1-bit I/O port. I/O specifiable.
			Timer 3 count input
P50 / AN00 to P57 / AN07	8	Input	Port 5 : 8-bit input port.
			Analog input 0 : 8 analog inputs to A/D converter
P60 / AN10 to P63 / AN13	4	I/O	Port 6 : 4-bit I/O port. I/O specifiable in units of bits.
			Analog input 1 : 4 analog inputs to A/D converter
P64 / CAP0 to P67 / CAP3	4	Input	Port 6 : 4-bit input port.
			Servo signal trigger input
PW0	1	Open drain output	Motor control output : PWM0 output
PW1	1	Open drain output	Motor control output : PWM1 output
VREF	1	–	A/D converter reference voltage input
AGND	1	–	Ground pin for A/D converter
CLK	1	Output	Clock Output : Outputs a pulse that is one-fourth the clock oscillating pulse frequency. Pulled up during reset.

Table 2.2 (1) Pin Names and Functions (3/3)

Pin name	Number of pins	I/O or 3-state	Function
TEST *	1	–	Test pin (use by fix to "H" level externally)
$\overline{RESET}$	1	Input	Reset : Initializes the TMP91P642A. (Built-in pull-up registor)
X_1 / X_2	2	I/O	Crystal oscillator connector pin
VSS (GND)	2	–	GND pin (0V)
VCC	1	–	Power supply pin (+ 5V)

(Note) * TMP91C642A is pulled up internally, but TMP91P642 is not pulled up. Therefore, TMP91P642 use by fix to "H" level externally.

(2) Functions and Pin Setting of PROM mode

Table 2.2 (2)

Pin Name	No. of pins	I/O	Functions	Pin Name (MCU mode)
D7 to D0	8	I/O	Data Input / Output	P07 to P00
A3 to A0 A11 to A4 A12, A13	4 8 2	Input	Address inputs	P13 to P10 P27 to P20 P40, P41
$\overline{OE}$	1	Input	Output Enable Input	P30
$\overline{CE}$	1	Input	Chip Enable Input	P31
VPP	1	Power supply	12.5 V / 5 V (Program supply voltage)	TEST
VCC	1	Power supply	5 V	VCC
VSS	2	Power supply	0 V	VSS

Pin Name	No. of pins	I/O	Pin Setting
P34 to P32	3	I/O	Be fixed to "L" level
P35, P36	2	Input	Be fixed to "L" level
P37	1	Output	Open
P47 to P42	6	I/O	Be fixed to "L" level
P57 to P50	8	Input	Be fixed to "L" level
P63 to P60	4	I/O	Be fixed to "L" level
P67 to P64	4	Input	Be fixed to "L" level
PW0, PW1	2	Output	Open
VREF	1		Be fixed to "L" level
AGND	1		Be fixed to "L" level
$\overline{RESET}$	1	Input	Be fixed to "L" level
CLK	1	Input	Be fixed to "L" level
X1	1	Input	Resonator connection pin
X2	1	Output	

3. OPERATION

The following is an explanation of hardware configuration and operation in relation to the TMP91P642. The TMP91P642 is same as the TMP91C642A except that an PROM is used instead of a built-in mask ROM. (However, the CLK pin of the TMP91C642A is always pulled up.) Therefore, for the function which is not described here, refer to the users manual of the TMP91C642A.

The TMP91P642 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status). Operation in the MCU mode is the same as for the TMP91C642A.

(2) Memory Map

Memory map is same as that of TMP91C642A.

Figure 3.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

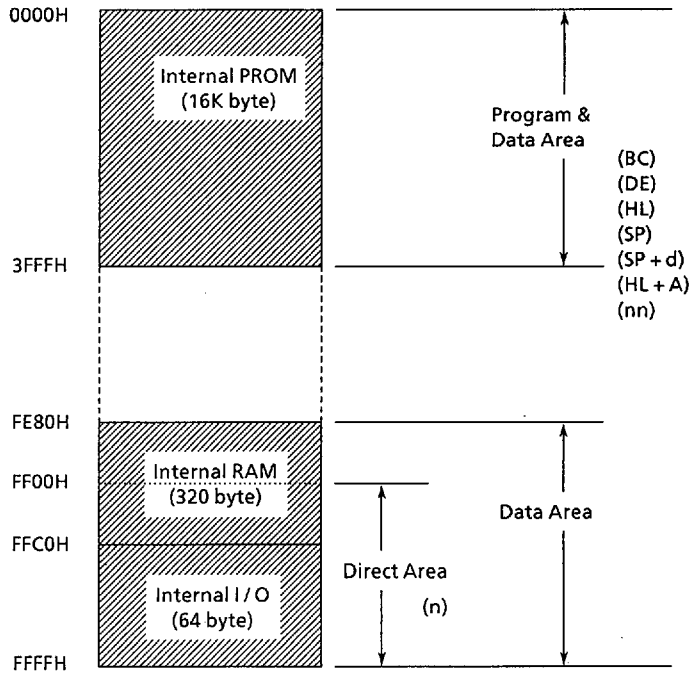


Figure 3.1 Memory Map

3.2 PROM Mode

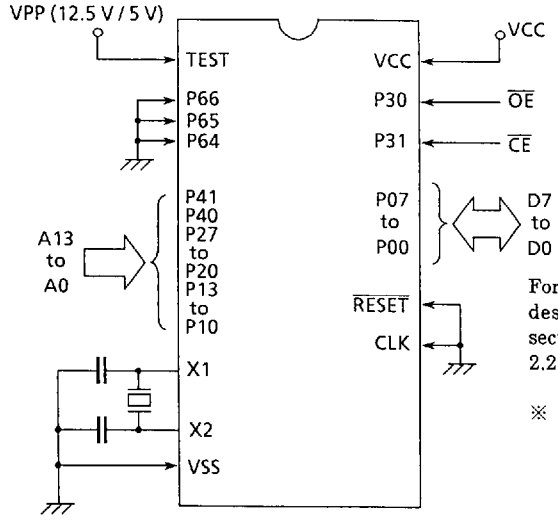
(1) Mode Setting and Function

The PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level.

In the PROM mode the programming and verification for the internal PROM is achieved by using a general EPROM programmer. The device selection (ROM Type) should be "27256" with following conditions.

Size : 256K bit (32K×8 bit) VPP : 12.5 V TPW : 1 ms

Setting for PROM mode is shown in Figure 3.2.



For other pins (which are not described here), refer to the section on pin functions (Table 2.2 (2)).

※ Use the 10 MHz resonator in case of programming and verification by a general EPROM programmer.

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Figure 3.2 PROM Mode Pin Setting

(2) Cautions for Electric signature

TMP91P642 does not support the electric signature mode (hereinafter referred to as "signature"). If PROM programmer uses the signature, the device is damaged because of applying voltage of 12±0.5V to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program Mode

All bits of TMP91P642 are "1" when delivered (the erase state). Data "0" is written in the necessary bit location during program operating.

Writing function can be operated at VPP = 12.5 V, $\overline{OE} = V_{IH}$, $\overline{CE} = V_{IL}$. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adapter Socket (BM1144, BM1145)

BM1144, BM1145 are the adapter sockets to write data into TMP91P642N, TMP91P642F built-in one time PROM using a general EPROM programmer.

(5) Program Storing Area of PROM Mode

TMP91P642 has the program space (0000H to 3FFFH) of 16K bytes.

The address 0000H to 3FFFH of PROM mode equals to the address 0000H to 3FFFH of MCU mode.

The program starts from the address 0000H after reset. Please write the program from the start address.

(6) Program Write Setting Method using a general-purpose PROM programmer

PROM to be prepared should equal to TMM27256AD functions.

1. Set the switch (SW1) of BM1144, BM1145 (hereinafter referred to as "adaptor") to the program side (NOR). (Note 1)
2. Connect MCU to the adapter. (Note 2)
3. Connect the adapter to PROM programmer. (Note 2)
4. Set the PROM type of PROM programmer to TMM27256AD.
5. Set the start address for writing PROM to 0000H, and the end address to 3FFFH. (Note 3)
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

(Note 1) If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

(Note 2) Please set the first pin of the adapter to that of PROM programmer. If not, MCU (or PROM programmer) would be damaged.

(Note 3) If data "0" is written in the address that exceeds 3FFFH, the program written in the address between 0000H and 3FFFH might be destroyed.

(7) Programming Flow Chart

The programming mode is set by applying 12.5 V (programming voltage) to the VPP pin when the following pins are set as follows,

$$\begin{pmatrix} \text{Vcc} & : 6.0\ \text{V} \\ \overline{\text{RESET}} & : \text{"L" level} \\ \text{CLK} & : \text{"L" level} \end{pmatrix}$$

* These conditions can be obtained by using adaptor socket.

After the address and input data have been fixed, a data on the Data Bus is programmed when the $\overline{CE}$ pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1 ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writting is performed by using threetimes longer programming pulse width (1ms×programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp=Vcc=5 V after all data were written.

Figure 3.3 shows the programming flow chart.

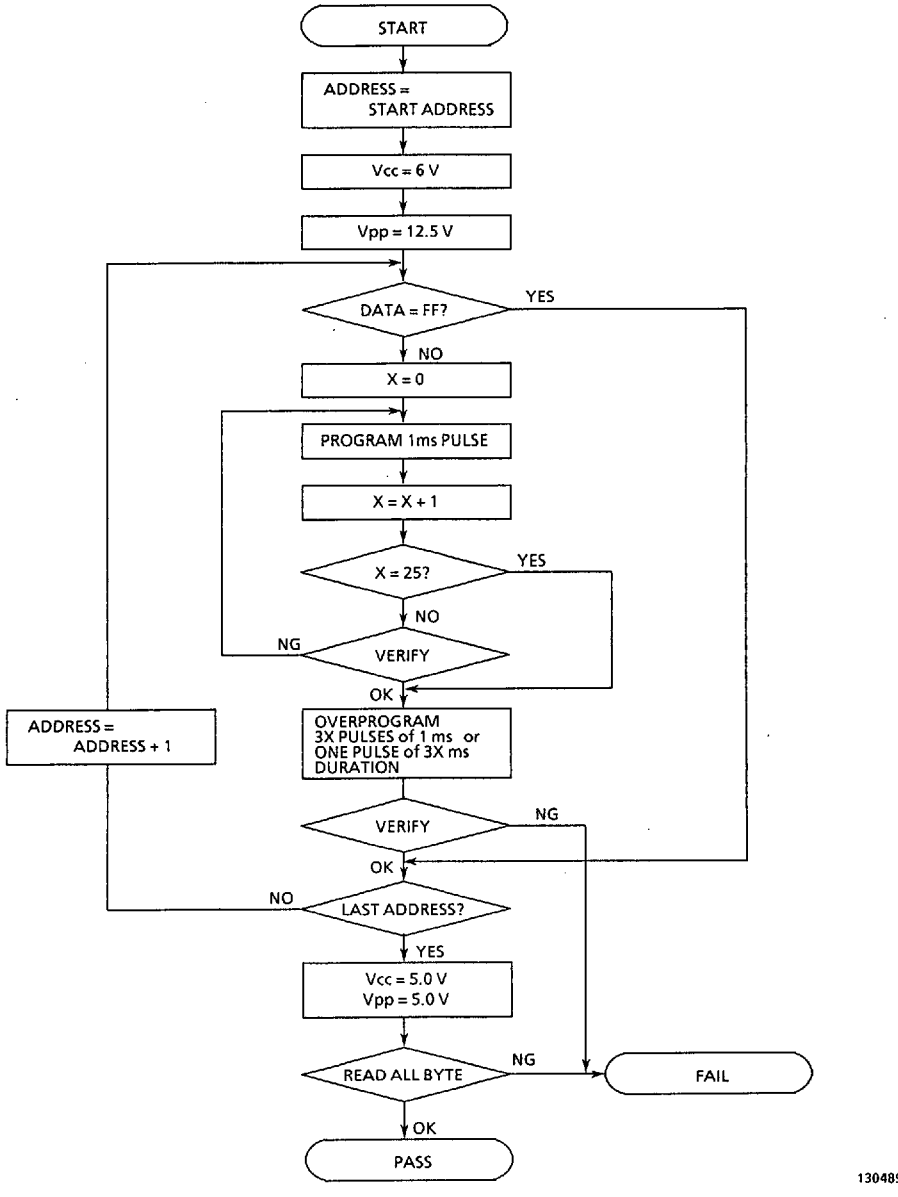

Figure 3.3 Flow Chart

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameter	Symbol	Pins	Rating	Unit
Power supply voltage	V_{CC}		− 0.5 to + 7	V
Input voltage	V_{IN}		− 0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT1}	except sink open drain pin	− 0.5 to V_{CC} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to + 10	
Output current (per 1 pin)	I_{OUT1}	P20	− 20	mA
	I_{OUT2}	P00 to P03, P10 to P13, P30 to P34, P40 to P47, P60 to P63, CLK	− 3	
	I_{OUT3}	P04~P07, P24~P27, PW0, PW1	30	
	I_{OUT4}	P20	20	
	I_{OUT5}	P21 to P23	10	
	I_{OUT6}	P00 to P03, P10 to P13, P30 to P34, P37, P40 to P47, P60 to P63, CLK	2	
Total Input/Output current (all pins)	ΣI_{OUT1}	Total current for I_{OUT1} and I_{OUT2}.	− 60	mA
	ΣI_{OUT2}	Total current for I_{OUT3} to I_{OUT6}.	120	
Power dissipation (T_{OPR} = 70°C)	P_{DF}	Flat package	500	mW
	P_{DS}	Shrink DIP package	600	
Soldering temperature (time)	T_{SOLDER}		260 (10 s)	°C
Storage temperature	T_{STG}		− 65 to + 150	°C
Operating temperature	T_{OPR}		− 20 to + 70	°C

4.2 DC Electrical Characteristics

V_{CC} = 5 V ± 10% Ta = − 20 to 70°C f_{OSC} = 10 MHz
Typical values are for V_{CC} = 5 V and Ta = 25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	− 0.3		0.3V_{CC}	V	
	V_{IL1}	− 0.3		0.25V_{CC}	V	Schmitt input circuit P33 to P35, P64 to P67, $\overline{RESET}$
	V_{IL2}	− 0.3		0.2V_{CC}	V	X1
Input High Voltage	V_{IH}	0.7V_{CC}		V_{CC} + 0.3	V	
	V_{IH1}	0.75V_{CC}		V_{CC} + 0.3	V	Schmitt input circuit P33 to P35, P64 to P67, $\overline{RESET}$
	V_{IH2}	0.8V_{CC}		V_{CC} + 0.3	V	X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = − 200 μA
	V_{OH1}	0.9V_{CC}			V	I_{OH} = − 20 μA
Output Low Current (open drain ports)	I_{OL1}		2		mA	V_{OL} = 0.45 V / P37
	I_{OL2}		20		mA	V_{OL} = 1.0 V / P04 to P07, P24 to P27, PW0, PW1
	I_{OL3}		5		mA	V_{OL} = 0.45 V / P21 to P23
Output Low Current	I_{OLC}	10	15		mA	V_{OL} = 1.0 V / P20
Output High Current	I_{OHC}		− 15	− 10	mA	V_{OH} = 2.4 V / P20
Hysteresis Voltage	V_{HS}		0.7		V	V_{CC} = 5 V, Ta = 25°C
Input Leakage Current	I_{LI}		0.02	± 10	μA	0.2 ≦ Vin ≦ VCC − 0.2
Output Leakage Current	I_{LO}		0.05	± 20	μA	0.2 ≦ Vin ≦ VCC − 0.2
Power Down Voltage	V_{STOP}	2 RAM BACK UP		6	V	at STOP Mode
$\overline{RESET}$ pull-up current	I_{RST}	30		110	μA	
Operating Current	I_{CC1}		25	50	mA	f_{OSC} = 10 MHz

4.3 AC Characteristics

V_{CC} = 5V ± 10% Ta = − 20 to 70°C CL = 50pF

Symbol	Parameter	10MHz Clock		Unit
		Min	Max	
t_{OSC}	OSC. Period	100		ns
t_{CYC}	CLK Period	400		ns
t_{WL}	CLK Low Width	160		ns
t_{WH}	CLK High Width	160		ns
t_{CPW}	CLK to Data Output		200	ns
t_{PRC}	Port Data Setup to CLK	200		ns
t_{CPR}	Port Data Hold After CLK	100		ns
t_{CGW}	CLK to TPG Data Output		400	ns

- AC output level High 2.2 V / Low 0.8 V
- AC input level High 0.8 V_{CC} / Low 0.2 V_{CC}

4.4 8 bit Event Counter

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C

Symbol	Parameter	12.5 MHz Clock		Unit
		Min	Max	
t_{VCK}	External input clock cycle (TI0, TI1, C-FG, PCTL)	900		ns
t_{VCKL}	External input Low clock pulse width	440		ns
t_{VCKH}	External input High clock pulse width	440		ns

4.5 Serial Channel Timing

V_{CC} = 5 V ± 10 % Ta = − 20 to 70 °C C_L = 50 pF

Symbol	Parameter	Condition	10 MHz Clock		Unit
			Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	@TBC2 (8/fc) Internal	800		ns
		@TBC6 (128/fc)	12800		
		External	1600		
t_{SCL}	SCLK Low Width	@TBC2 (8/fc) Internal	350		ns
		@TBC6 (128/fc)	6350		
		External	750		
t_{SCH}	SCLK High Width	@TBC2 (8/fc) Internal	350		ns
		@TBC6 (128/fc)	6350		
		External	750		
t_{SKDO}	SCLK → TxD (Output Data) delay time	Internal	150		ns
		External	700		
t_{SRD}	SCLK Rising Edge to Input DATA Valid	Internal	640		ns
		External	1900		
t_{HSR}	Input Data Hold After SCLK Rising Edge	Internal	200		ns
		External	700		

4.6 A/D Conversion Characteristics

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C, f_{OSC} = 10 MHz

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	Vcc − 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	V_{SS}	V_{SS}	Vss	
V_{AIN}	Allowable analog input voltage	V_{SS}		Vcc	
I_{REF}	Supply current for analog reference voltage		0.6	1.0	mA
Error	Total error (Ta = 25 °C, Vcc = V_{REF} = 5V)			3	LSB

4.7 Interrupt Operation

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C

Symbol	Parameter	10 MHz Clock		Unit
		Min	Max	
t_{INTAL}	INT0 Low-level pulse width (⌐‾¬)	400		ns
t_{INTAH}	INT0 High-level pulse width (_⌐¬_)	400		ns
t_{INTBL}	INT1, INT2 Low-level pulse width (⌐‾¬)	900		ns
t_{INTBH}	INT1, INT2 High-level pulse width (_⌐¬_)	900		ns

4.8 Read Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = − 20 to 70 °C Vcc = 5 V ± 10 %

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	−	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A13, $\overline{CE}$, $\overline{OE}$)	−	0.7 × V_{CC}	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A13, $\overline{CE}$, $\overline{OE}$)	−	− 0.3	0.3 × V_{CC}	V
t_{ACC}	Address to Output Delay	C_L = 50 pF	−	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

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4.9 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = 25 ± 5 °C Vcc = 6 V ± 0.25 V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programing Algorithm	−	12.25	12.50	12.75	V
V_{IH}	Input High Voltage (D0 to D7)	−	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 to D7)	−	− 0.3		0.2V_{CC}-0.1	V
V_{IH1}	Input High Voltage (A0 to A13, $\overline{CE}$, $\overline{OE}$)	−	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A13, $\overline{CE}$, $\overline{OE}$)	−	− 0.3		0.3V_{CC}	V
I_{CC}	V_{CC} Supply Current	t_{OSC} = 10 MHz	−		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00 V	−		50	mA
t_{PW}	$\overline{CE}$ Program Pulse Width	C_L = 50 pF	0.95	1.00	1.05	ms

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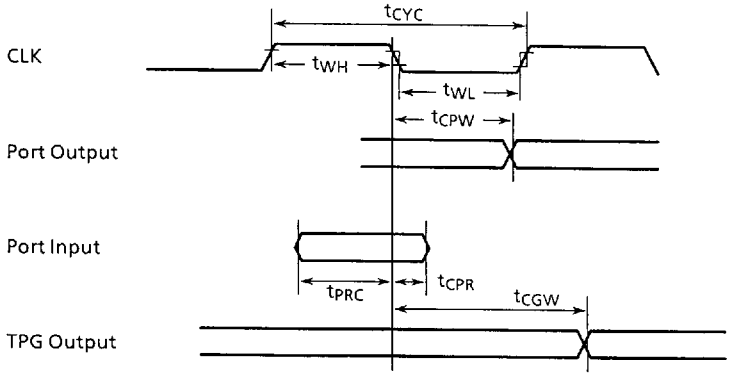
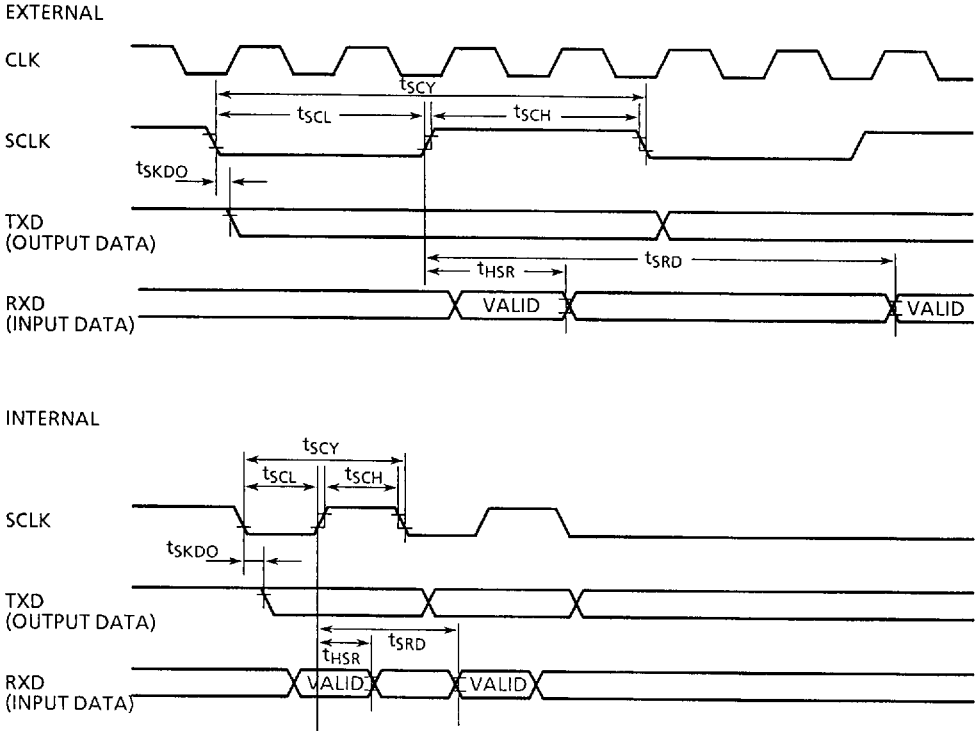
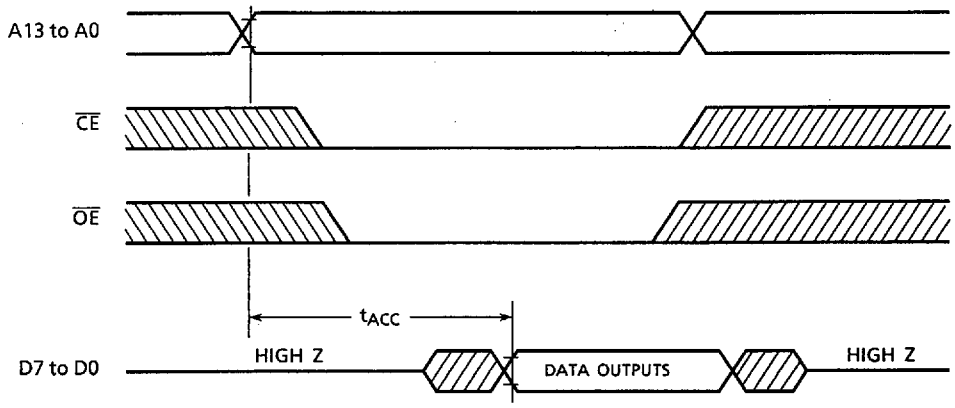
4.10 Timing Chart



4.11 Serial Channel Timing Chart



4.12 Read Operation Timing Chart (PROM Mode)



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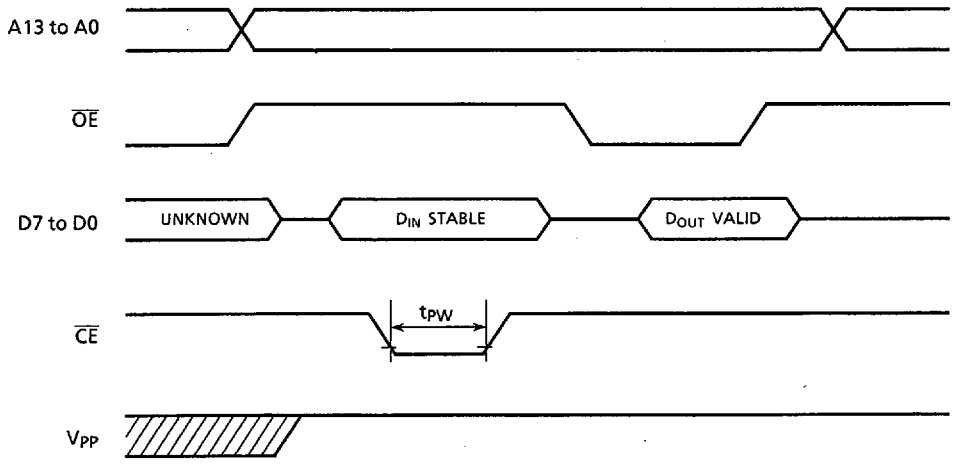
4.13 Programming Operation Timing Chart (PROM Mode)



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