

0.4Ω Ultra Low ON-Resistance, Dual, SPDT Analog Switch

UM2268 QFN10 1.8×1.4
UM2268A QFN10 2.1×1.6

General Description

The UM2268/UM2268A is a dual, low-power single-pole/ double-throw (SPDT) analog switch that operates from a single +1.8V to +4.4V supply.

The UM2268/UM2268A features guaranteed on-resistance matching (0.04Ω TYP) between switches and guaranteed on resistance flatness over the signal range (0.08Ω TYP), as well as high off-isolation and low crosstalk. This ensures excellent linearity and low distortion when switching audio signals.

The UM2268 is available in Pb-free QFN10 package (1.8mm×1.4mm×0.55mm), while the UM2268A is available in Pb-free QFN10 package (2.1mm×1.6mm×0.55mm).

Applications

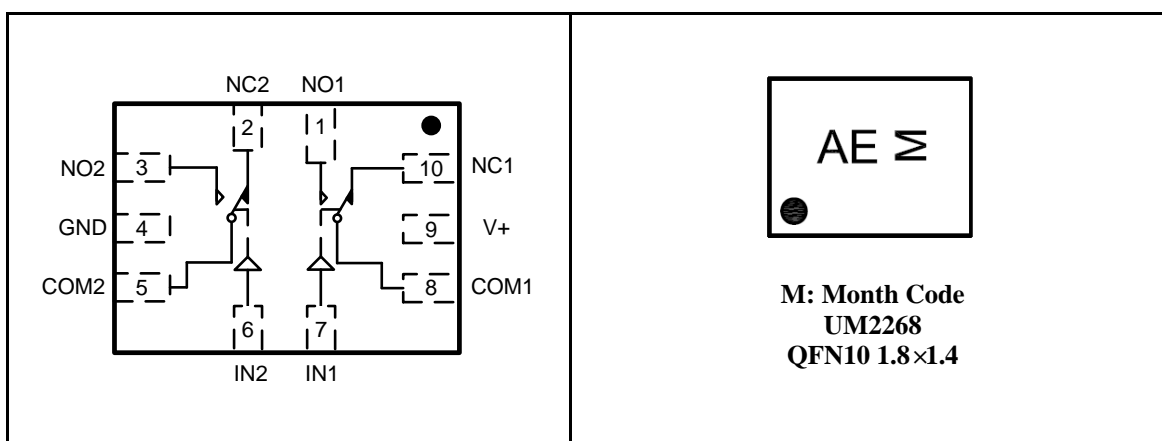
- Portable Instrumentation
- Battery-Operated Equipment
- Computer Peripherals
- Speaker and Earphone Switching
- Medical Equipment
- Audio and Video Switching

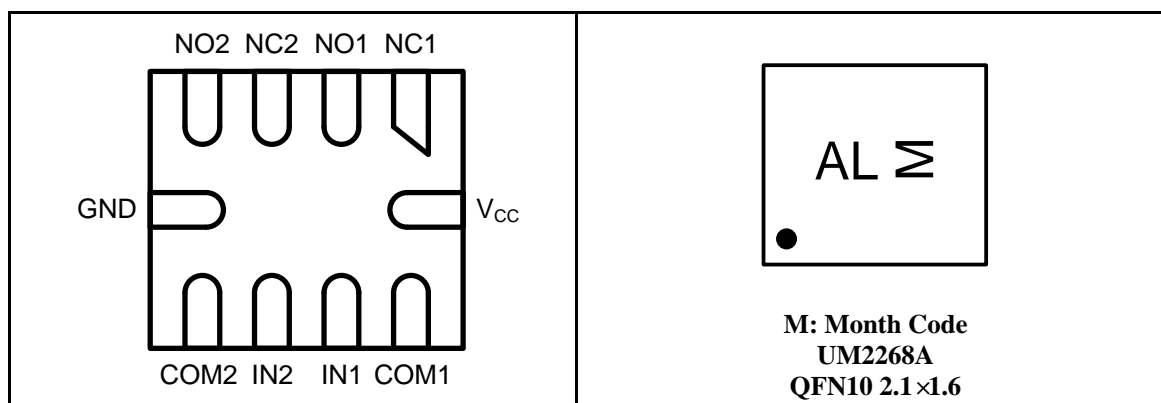
Features

- V_{CC} Operating Range: +1.8V to +4.4V
- Low On-Resistance: 0.4Ω(TYP) at +4.4V
- On-Resistance Matching: (0.04Ω TYP)
- On-Resistance Flatness: (0.08Ω TYP)
- -3dB Bandwidth:80MHz
- Low Off-Isolation: -78dB (100kHz)
- Low Crosstalk: -93dB (100kHz)
- TTL/CMOS Compatible
- Break-Before-Make Switching
- Rail-to-Rail Input and Output Operation
- Lead (Pb) Free QFN10 Package

Pin Configurations

Top View





Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM2268	QFN10 1.8mm×1.4mm	AE	3000pcs/7 Inch Tape & Reel
UM2268A	QFN10 2.1mm×1.6mm	AL	

Pin Description

UM2268	UM2268A	Name	Function
1,3	2,4	NO1,NO2	Normally-open terminal
10,2	1,3	NC1,NC2	Normally-closed terminal
4	5	GND	Ground
8,5	9,6	COM1,COM2	Common terminal
7,6	8,7	IN1,IN2	Digital control pin to connect the COM terminal to the NO or NC terminals
9	10	V+	Power Supply

Function Table

LOGIC	NO	NC
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
V ₊	Supply Voltage	0 to +4.6	V
V _{IS}	Analog Switch Input Voltage	-0.3 to (V _{CC} + 0.3)	
V _{IN}	Digital Select Input Voltage	0 to +4.6	
I _D	Continuous DC Current	250	mA
I _P	Peak Current	350	mA
T _O	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	
ESD	HBM	4000	

Electrical Characteristics

V₊ = +4.4V, GND = 0V, T_A = -40 °C to +85 °C. Unless otherwise noted.

Symbol	Parameter	Test Conditions	V _{CC} (V)	Temp	Limits (-40 to 85 °C)			Unit
					Min	Typ (Note1)	Max	
V ₊	Power Supply Range			Full	1.8		4.4	V
I _{CC}	Quiescent Supply Current	V _{IN} = V ₊ or 0	4.4	Full			1.0	μA
I _{IN}	Input Leakage Current	V _{IN} =0V/4.4V	4.4	Full			1.0	μA
I _{OFF}	Power Off Leakage Current	V _{NO} /V _{NC} =3.3V/0.3V, V _{COM} =0.3V/3.3V	4.4	Full			1.0	μA
I _{ON}	Channel ON Leakage Current	V _{COM} =0.3V/3.3V V _{NO} or V _{NC} =0.3V/3.3V, or floating	4.4	Full			1.0	μA
R _{ON}	On-Resistance (Note2)	V _{NO} , V _{NC} or V _{COM} =1.0V, I _{COM} =-100mA	4.4	Room Full		0.4	0.75 0.85	Ω
ΔR _{ON}	On Resistance Match Between Channels (Note2,3,4)	V _{NO} , V _{NC} or V _{COM} =1.0V, I _{COM} =-100mA	4.4	Room Full		0.04	0.15 0.20	Ω
R _{FLAT}	On Resistance Flatness (Note2,3,5)	V _{NO} , V _{NC} or V _{COM} =1.0V, 2.5V I _{COM} =-100mA	4.4	Room Full		0.08	0.12 0.20	Ω
V _{IH}	Input High Voltage		4.4	Full	2.0			V
V _{IL}	Input Low Voltage		4.4	Full			0.5	V
t _{ON}	Turn On Time	V _{IN} = 2.1V to 0V, R _L =50Ω, C _L =35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} =2.1V, Test Circuit1	4.4	Room		88		ns
t _{OFF}	Turn Off Time	V _{IN} = 2.1V to 0V, R _L =50Ω, C _L =35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} =2.1V, Test Circuit1	4.4	Room		16		ns
t _{BBM}	Break Before Make Time (Note 6)	V _{IN} = 2.1V to 0V, R _L =50Ω, C _L =35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} =2.1V, Test Circuit2	4.4	Room		6		ns
O _{IRR}	Off Isolation (Note 7)	V _{BIAS} =2.1V, Signal=0dBm, Test Circuit3	4.4	Room		-78		dB
				Room		-58		dB
X _{TALK}	Crosstalk	V _{BIAS} =2.1V, Signal =0dBm, Test Circuit4	4.4	Room		-93		dB
				Room		-90		dB
BW	-3dB Bandwidth	V _{BIAS} =2.1V, Signal = 0dBm, Test Circuit5	4.4	Room		80		MHz
Q	Charge Injection Select Input to Common I/O	V _G =0V, R _S =0Ω, C _L =1.0nF, Test Circuit6	4.4	Room		4.0		pC
C _{ON}	HSD+ HSD- ON Capacitance (Note8)		4.4	Room		56		pF

1: Typically values are at V₊=4.4V and T_A=+25°C.

2: Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

3: Parameter is characterized but not tested in production.

4: ΔR_{ON} = | R_{ON(N01/NC1)} - R_{ON(N02/NC2)} | measured at identical V_{CC}, temperature and voltage levels.

5: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

6: Guaranteed by Design.

7: Off Isolation = 20 log₁₀ [V_{COM}/V_{NO/NC}].

8: T_A = +25, f = 1 MHz, Capacitance is characterized but not tested in production.

Electrical Characteristics

V+ = +2.7V to +3.6V, T_A = -40 °C to + 85 °C. Unless otherwise noted.

Symbol	Parameter	Test Conditions	V _{cc} (V)	Temp	Limits (-40 to 85 °C)			Unit
					Min	Typ (Note1)	Max	
V _{NO} , V _{NC} , V _{COM}	Analog Signal Range			Full	0		V+	V
I _{IN}	Input Leakage Current	V _{IN} =0V/2.7V	2.7	Full			1.0	µA
I _{OFF}	Power Off Leakage Current	V _{NO} /V _{NC} =3.3V/0.3V, V _{COM} =0.3V/3.3V	3.6	Full			1.0	µA
I _{ON}	Channel ON Leakage Current	V _{COM} =0.3V/3.3V V _{NO} or V _{NC} =0.3V/3.3V, or floating	3.6	Full			1.0	µA
R _{ON}	On-Resistance (Note2)	V _{NO} , V _{NC} or V _{COM} =1.0V, I _{COM} =-100mA	2.7	Room Full		0.75	1.10 1.20	Ω
ΔR _{ON}	On Resistance Match Between Channels (Note2,3,4)	V _{NO} , V _{NC} or V _{COM} =1.0V, I _{COM} =-100mA	2.7	Room Full		0.03	0.15 0.20	Ω
R _{FLAT}	On Resistance Flatness (Note2,3,5)	V _{NO} , V _{NC} or V _{COM} =1.0V, 2.5V I _{COM} =-100mA	2.7	Room Full		0.10	0.18 0.20	Ω
V _{IH}	Input High Voltage		3.0	Full	1.5			V
V _{IL}	Input Low Voltage		3.0	Full			0.4	V
t _{ON}	Turn On Time	V _{IN} = 1.5V to 0V, R _L = 50Ω, C _L = 35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} = 1.5V, Test Circuit1	3.0	Room		100		ns
t _{OFF}	Turn Off Time	V _{IN} = 1.5V to 0V, R _L = 50Ω, C _L = 35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} = 1.5V, Test Circuit1	3.0	Room		20		ns
t _{BBM}	Break Before Make Time (Note 6)	V _{IN} = 1.5V to 0V, R _L = 50Ω, C _L = 35pF, V _{NO1} , or V _{NC1} = V _{NO2} , or V _{NC2} = 1.5V, Test Circuit2	3.0	Room		9.2		ns
O _{IRR}	Off Isolation (Note 7)	V _{BIAS} =2.1V, Signal = 0dBm, Test Circuit3	3.0	Room		-78		dB
				Room		-58		dB
X _{TALK}	Crosstalk	V _{BIAS} =2.1V, Signal = 0dBm, Test Circuit4	3.0	Room		-93		dB
				Room		-90		dB
BW	-3dB Bandwidth	V _{BIAS} =2.1V, Signal=0dBm, Test Circuit5	3.0	Room		80		MHz
Q	Charge Injection Select Input to Common I/O	V _G =0V, R _S =0Ω, C _L =1.0nF, Test Circuit6	3.0	Room		3.0		pC
C _{ON}	HSD+ HSD- ON Capacitance (Note8)		3.0	Room		56		pF

1: T_A=+25 °C.

2: Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

3: Parameter is characterized but not tested in production.

4: ΔR_{ON} = | R_{ON(NO1/NC1)} - R_{ON(NO2/NC2)} | measured at identical V_{CC}, temperature and voltage levels.

5: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

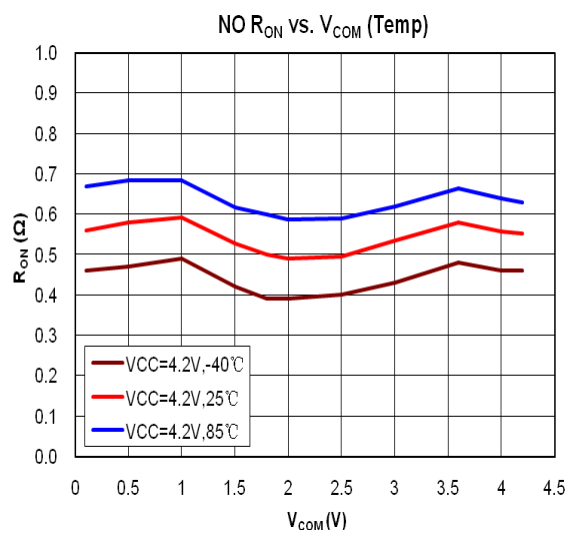
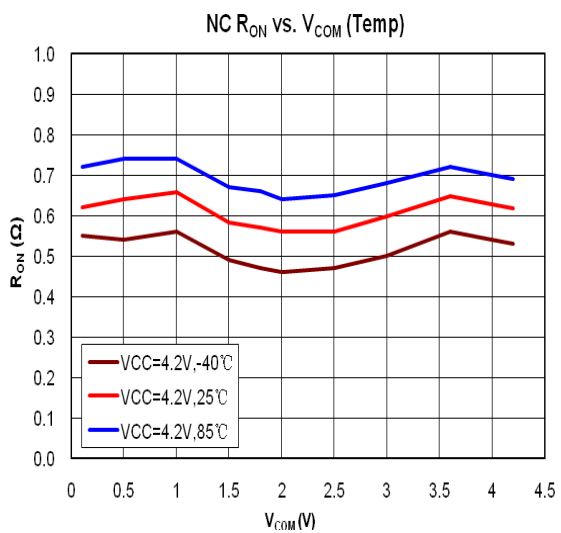
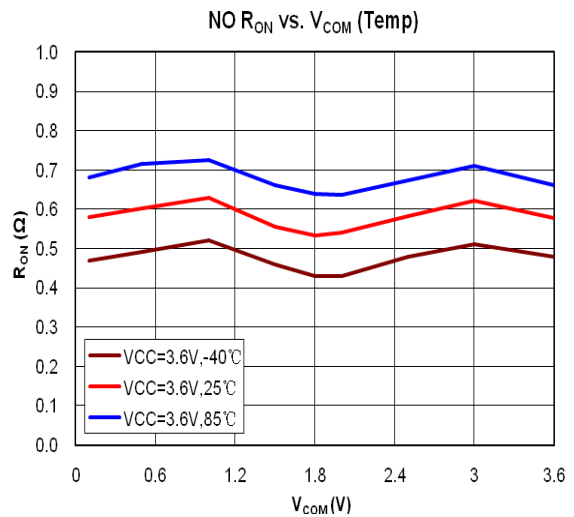
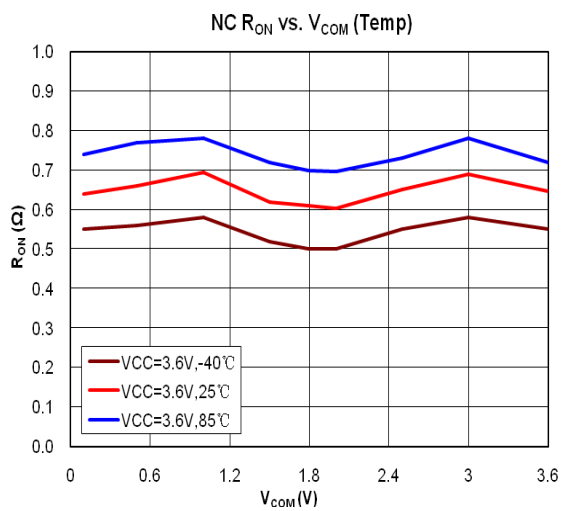
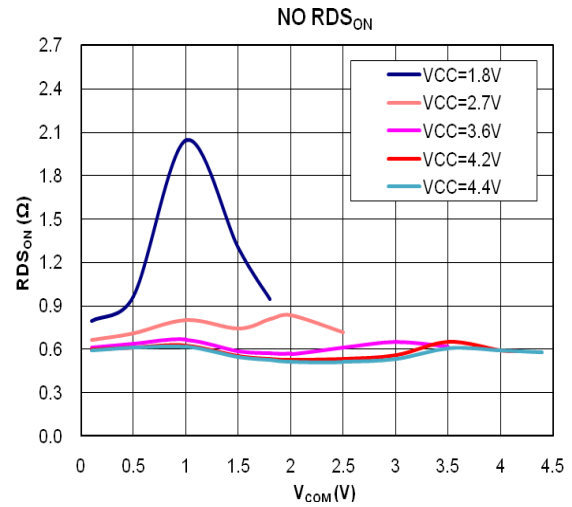
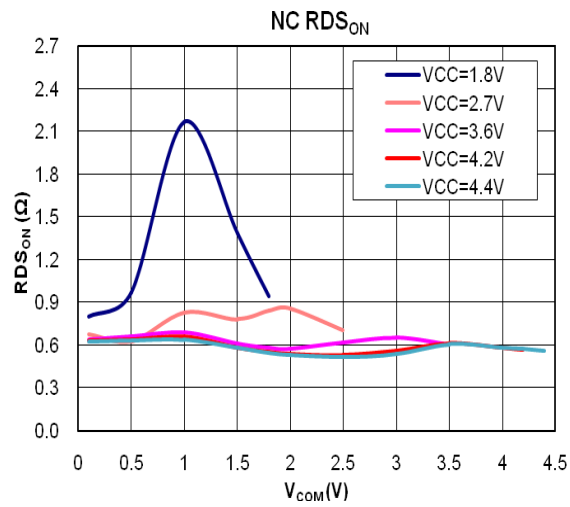
6: Guaranteed by Design.

7: Off Isolation = 20 log₁₀ [V_{COM}/V_{NO/NC}].

8: T_A = +25, f = 1 MHz, Capacitance is characterized but not tested in production.

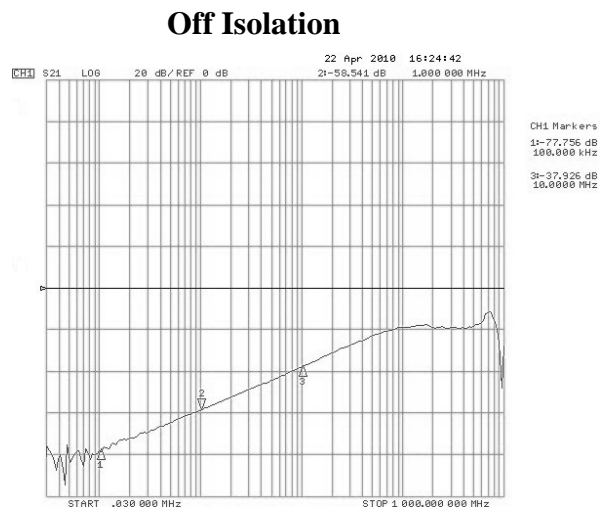
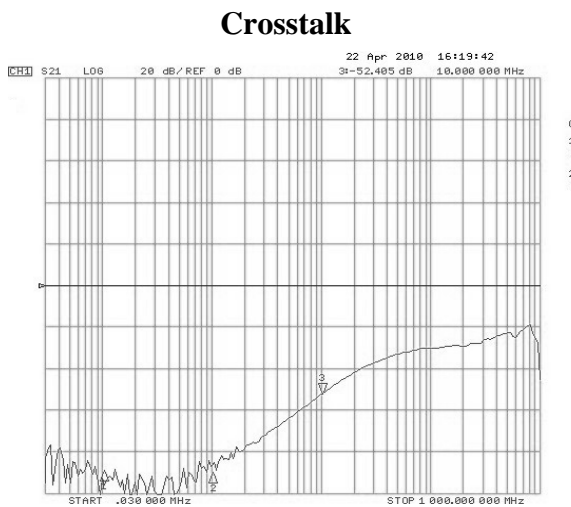
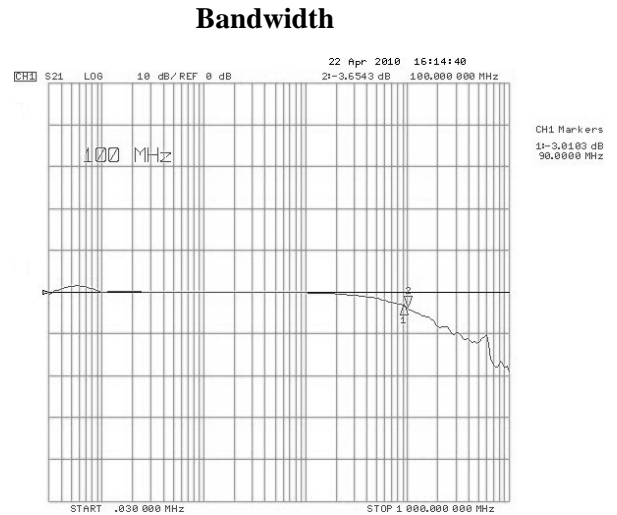
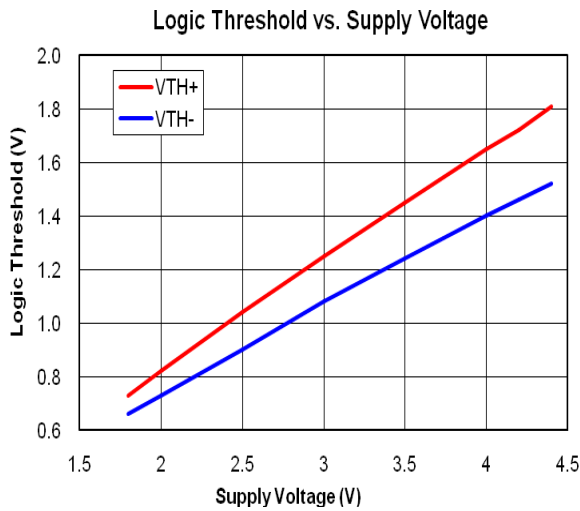
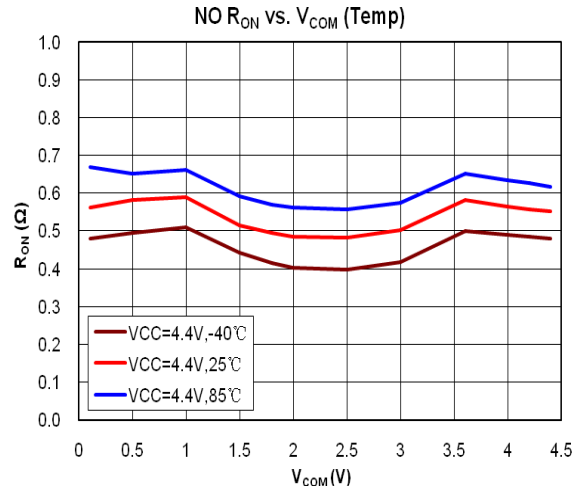
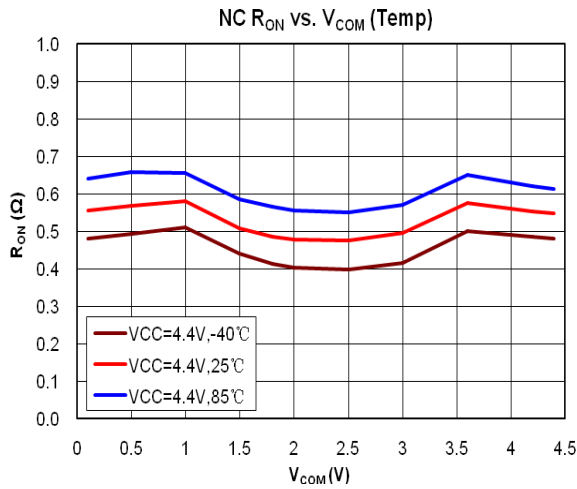
Typical Operating Characteristics

($T_A=+25^\circ\text{C}$. Unless otherwise noted.)

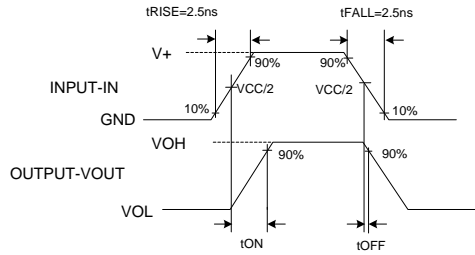
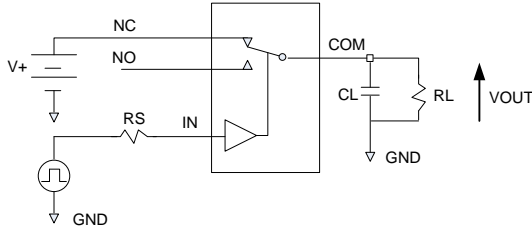


Typical Operating Characteristics (Continued)

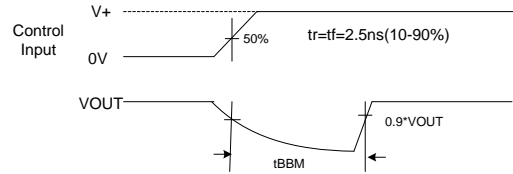
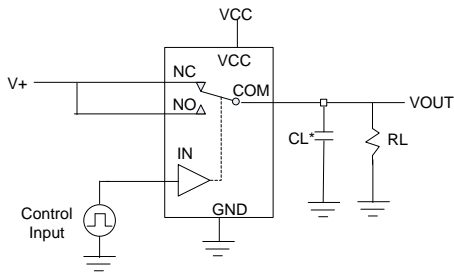
($T_A=+25^\circ\text{C}$. Unless otherwise noted.)



Test Circuits

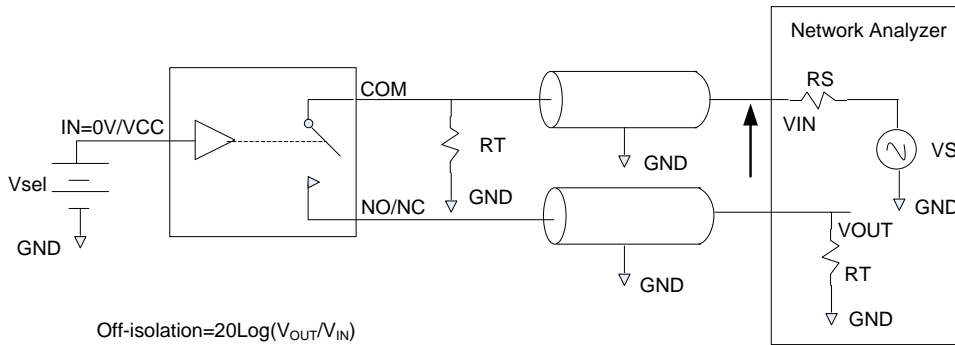


Test Circuit 1. Switching Timing (ton, toff)



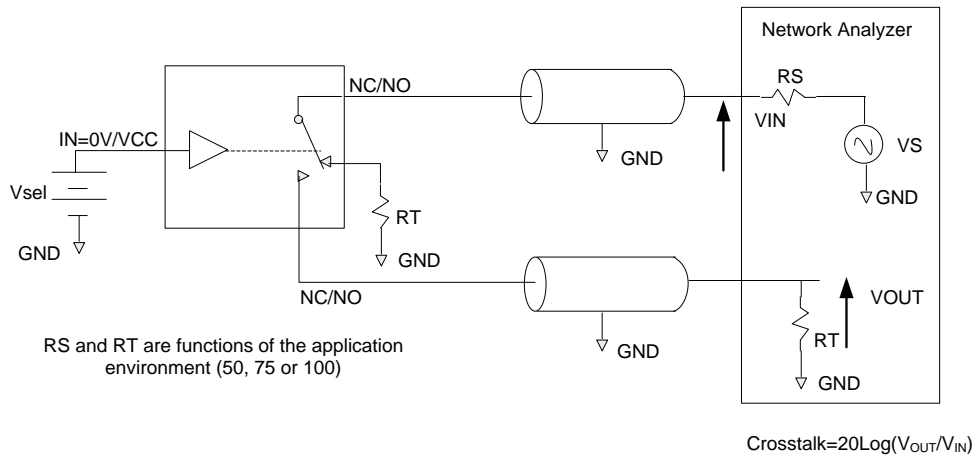
CL* includes fixture and stray capacitance

Test Circuit 2. Break-Before-Make Timing

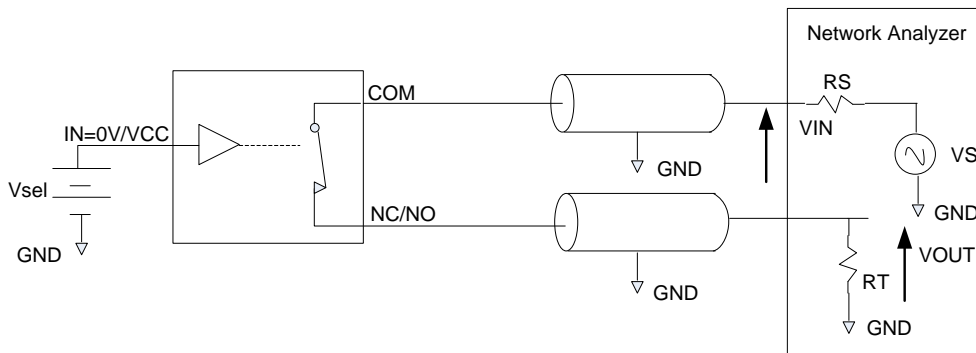


Off-isolation=20Log(V_{OUT}/V_{IN})

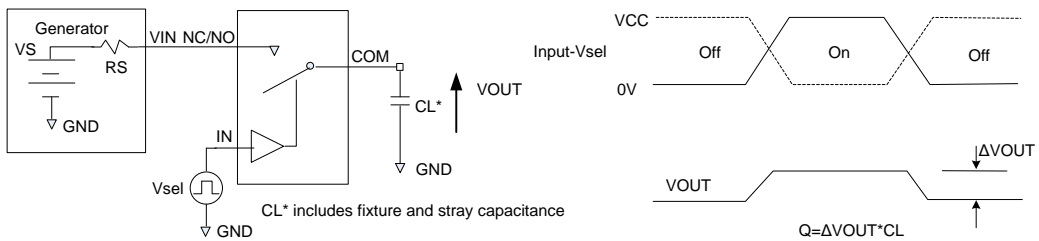
Test Circuit 3. Off-Isolation



Test Circuit 4. Channel-to-Channel Crosstalk



Test Circuit 5. Bandwidth

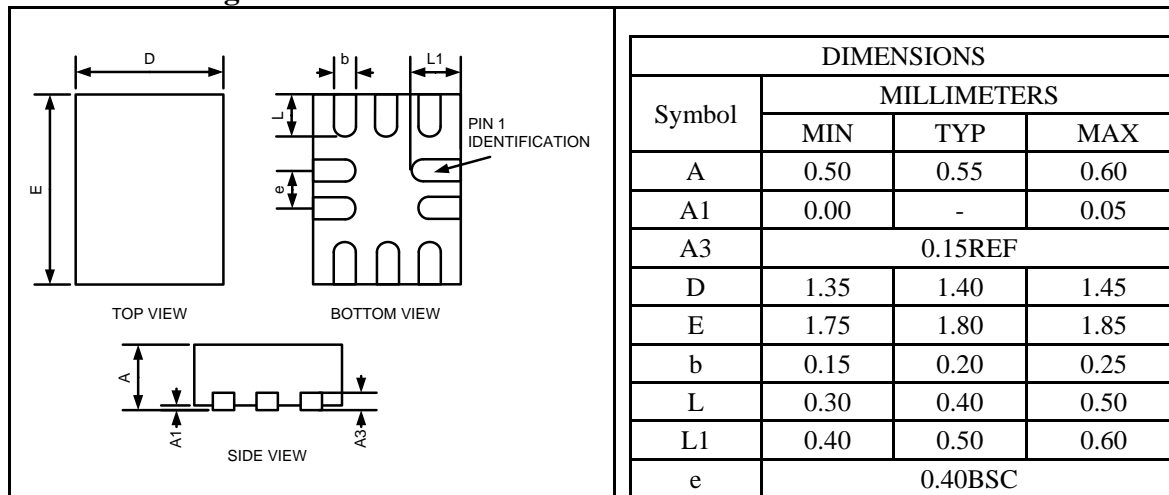


Test Circuit 6. Charge Injection Test

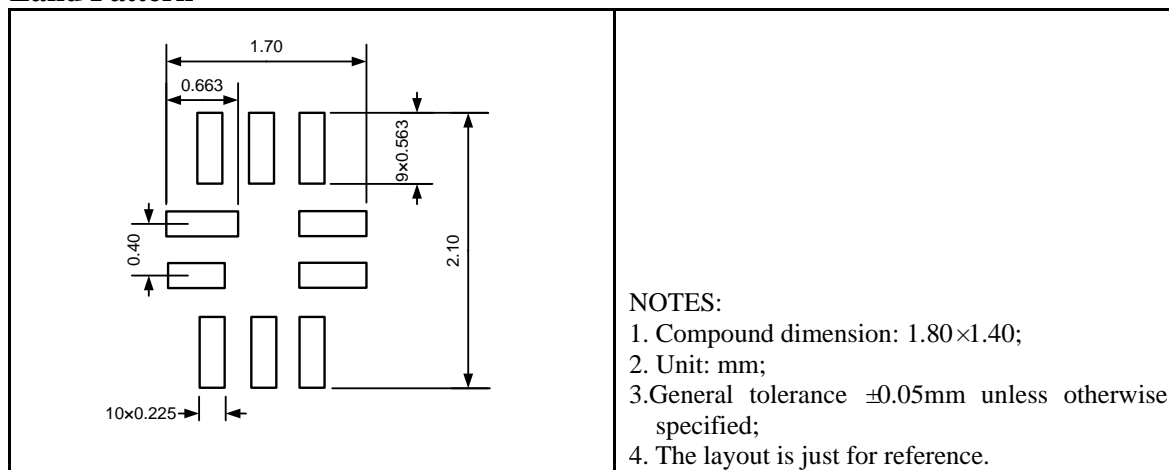
Package Information

UM2268 QFN10 1.8×1.4

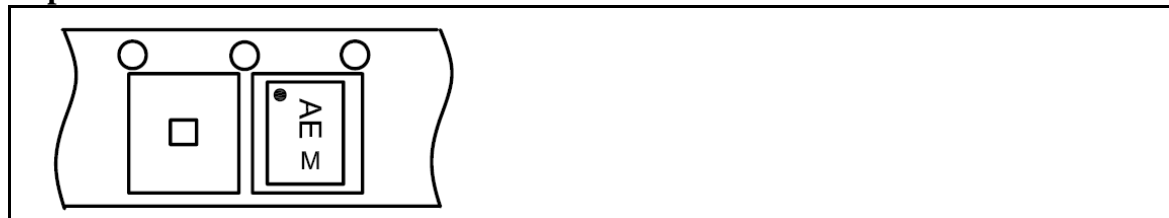
Outline Drawing



Land Pattern

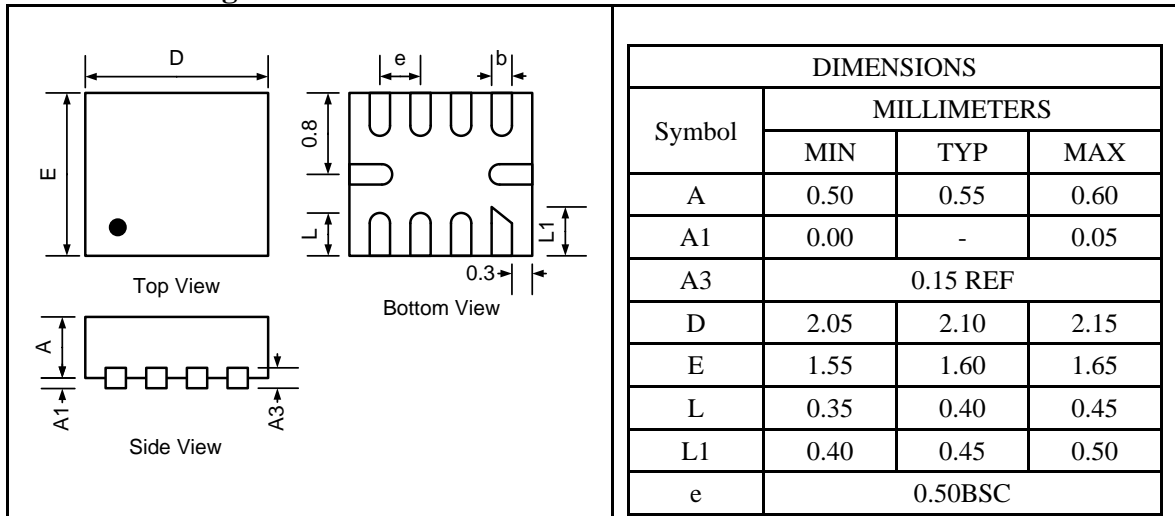


Tape and Reel Orientation

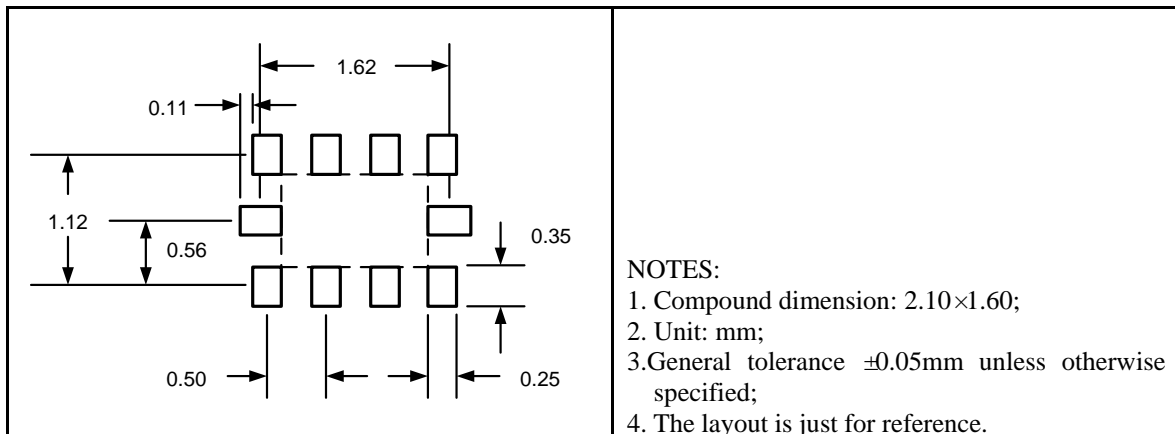


UM2268A QFN10 2.1x1.6

Outline Drawing



Land Pattern



Tape and Reel Orientation



IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Union assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. Union reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.



Union Semiconductor, Inc

Add: 2F, No. 3, Lane647 Songtao Road, Shanghai 201203

Tel: 021-51093966

Fax: 021-51026018

Website: www.union-ic.com