W536Q020/Q030/Q060/Q090/Q120

Winbond
Electronics Corp.

VOICE/MELODY/LCD CONTROLLER
(*ViewTalk* TM Series)

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1. GENERAL DESCRIPTION

The W536QXXX, a member of *ViewTalk*^TM family, is a high-performance 4-bit micro-controller (uC) with built-in speech unit, melody unit and 40seg * 16 com LCD driver unit which includes internal regulator pump circuit and dedicated one pages LCD RAM. The 4-bit uC core contains dual clock source, 4-bit ALU, two 8-bit timers, one 14 bits divider, 12 pads for input or output, 7 interrupt sources and 8-level nesting for subroutine/interrupt applications. Speech unit, integrated as a single chip with maximum 128 seconds (based on 6.4K sample rate with 5 bits MDPCM), is capable of expanding to 512 seconds speech addressed by external memory W55XXX with serial bus interface.

It can be implemented with Winbond Power Speech using MDPCM algorithm. Melody unit provides dual tone output and can store up to 1k notes. Power reduction mode is also built in to minimize power dissipation. It is ideal for games, educational toys, remote controllers, watches, clocks and other application products that incorporate both LCD display and speech.

PART NO	W536Q020	W536Q030	W536Q060	W536Q090	W536Q120
Voice	20 sec	30 sec	60 sec	90 sec	120 sec
I/O pad	8I/O, 4I (RA/RB/RD)	8I/O, 4I (RA/RB/RD)	8I/O, 8I (RA/RB/RC/RD)	8I/O, 8I, 8O (RA/RB/RC/RD/ RE/RF)	8I/O, 8I, 8O (RA/RB/RC/RD/ RE/RF)
WDT disable/Enable (Mask Option)	Y	Y	Y	Y	Y
Sub-clock RC/XTAL Mode (Mask Option)	Y	Y	Y	Y	Y
RD port shared as serial bus (Mask Option)	Y(1)	Y(1)	Y(1)	N	N
Tri-state serial bus (Mask Option) (3)	Y	Y	Y	N	N
Cascaded Voice ROM through serial bus (2)	N	N	Y(1)	N	Y

Notes:

1. Share 3 pads of RD port (RD1/ADDR, RD2/DATA and RD3/CLK)

2. Dedicate serial bus 3 pads (ADDR, DATA and CLK) to interface with W55XXX. Cascaded Voice ROM can help to expand voice up to 512 sec by W55XXX chip.

3. Tri-state serial bus mask option can float serial bus while voice playing is no active. Let this mask option is disabled to get minimum power consumption in general.

2. FEATURES

- Operating voltage: 2.4 volt ~ 5.5 volt
- Watch dog disabled/enabled by mask option
- Dual clock operating system
  - Main clock with Ring/Crystal (400 KHz to 4 MHz)
  - Sub-clock with 32.768 KHz RC/Crystal by mask option
- Memory
  - Program ROM (P-ROM): 16K × 20 (ROM Bank0)
  - Data RAM (W-RAM): 1K × 4 bit
    (RAM Bank 0 is 512 nibbles from 0:000~0:1FF and 0:380~0:3FF are mapped to special register.
    RAM Bank F is 512 nibbles from F: 200~F: 3FF either data RAM or dedicated to script kernel)
  - LCD RAM (L-RAM): 160× 4 bit × 1 pages (RAM Bank1 from **260~2FF**)
- Maximum 24 input/output pads
  - Ports for input only: 8 pads (RC, RD port; RD1~3 can share as serial bus for external memory W55XXX interface @W536Q020/Q030/Q060)
  - Ports for output only: 8 pads (RE & RF port; W536Q090/Q120 available only)
  - Ports for Input/output: 8 pads (RA and RB port)
- Power-down mode
  - Hold mode (except for 32kHz oscillator)
  - Stop mode (including 32kHz oscillator and release by RD or RC port)
- Seven types of interrupts
  - Five internal interrupts (Divider, Timer 0, Timer 1, Speech, Melody)
  - Two external interrupts (RD, RA)
- One built-in 14-bit clock frequency divider circuit
- Two built-in 8-bit programmable countdown timers
  - Timer 0: one of two clock sources (FOSC/4 or FOSC/1024) can be selected
  - Timer 1: built-in auto-reload function includes internal timer
- Built-in 18/14-bit watchdog timer for system reset.
- Powerful instruction sets
- 8-level subroutine (including interrupt) nesting
- LCD driver unit capability
  - VLCD higher than (V_{DD} -0.5V)
  - Built-in voltage regulator to V2 pad
  - 40 seg × 16 com (seg: 24~63; com: 0~15)
  - 1/16 or 1/8 duty, 1/5 or 1/4 bias, internal pump circuit option by special register
  - COM 8~15 and SEG40~63 can be shared as general input/output by special register
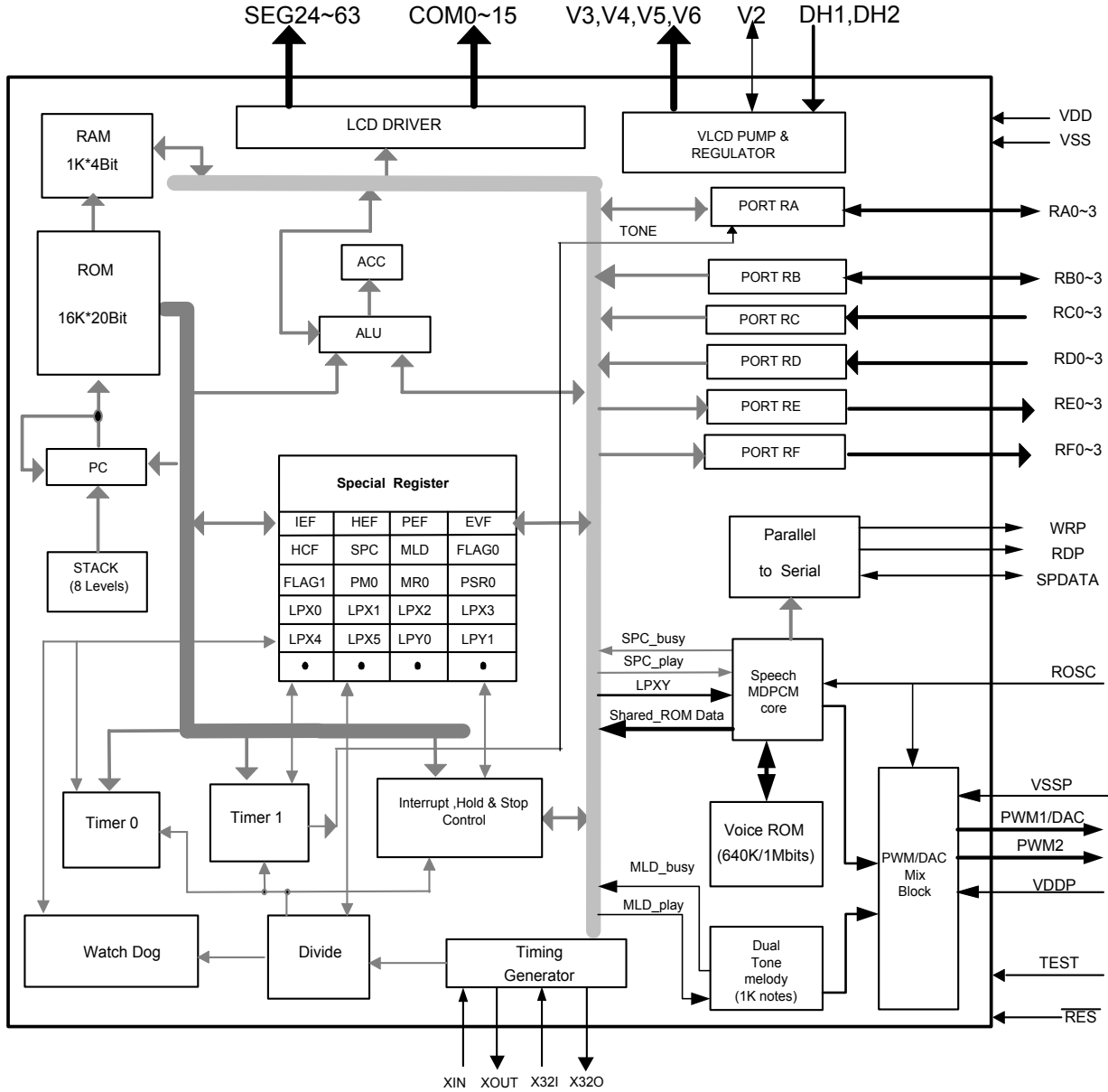 - Either uC ROM or voice ROM used as LCD picture

- Speech function
  - Provided 640K/ 1M/ 2M/ 3M/ 4M bits Voice ROM for W536Q020/ Q030/ Q060/ Q090/ Q120 based on 5 bits MDPCM algorithm
  - Voice ROM (V-ROM) available for uC data or LCD picture data.
  - Maximum 8*256 Label/Interrupt vector (voice section number) available
  - Provide two types of speech busy flag to either each GO or each trigger
  - Maximum up to 16M bits speech address capability interface with external memory W55XXX through serial bus.
- Melody function
  - Provide 1K notes (22bits/note) dedicated melody ROM
  - Provide two types of melody busy flag to uC either each note or each song
  - Provide 6 kinds of beat, 16 kinds of tempo, and pitch range from G3# to C7
  - Tremolo, triple frequency and 3 kinds of percussion available
  - Maximum 31 songs available
- Can mix speech with melody
- Multi-engine controller
- Direct driving speaker/buzzer or DAC output
- Chip On Board available

W536Q020/Q030/Q060/Q090/Q120

3. BLOCK DIAGRAM

4. PAD DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN/RXIN	I	Input pad for main clock oscillator. It can be connected to crystal when crystal mode is selected (SCR0.2=1), otherwise connect a resistor to VDD to generate main system clock while Ring mode is selected (SCR0.2=0 and default). Oscillator can be enabled or stopped by set SCR0.1 to 1 or clear to 0 separately. External capacitor connects to start oscillation and get more accurate clock when while crystal mode
XOUT	O	Output pad for oscillator that is connected to another crystal pad when in crystal mode. External capacitor connects to start oscillation when in crystal mode.
X32I/RSUB1	I	32.768 KHz crystal input pad or external resistor node 1 **by mask option**. External 15~20pF capacitor connects to start oscillation and get more accurate clock when in crystal mode.
X32O/RSUB2	O	32.768 KHz crystal output pad or external resistor node 2 **by mask option.** External 15~20pF capacitor connects to start oscillation and get more accurate clock when in crystal mode.
RA0 ~ RA3/TONE (8)	I/O	General Input/Output port specified by PM1 register. If output mode is selected, PM0 register bit 0 can be used to specify CMOS/NMOS driving capability option (7). Initial state is input mode. RA3 may be uses as TONE if bit 0 of MR0 special register is set to logic 1. An interrupt source.
RB0 ~ RB3 (8)	I/O	General Input/Output port specified by PM2 register. If output mode is selected, PM0 register bit 1 can be used to specify CMOS/NMOS driving capability option (7). Initial state is input mode.
RC0 ~ RC3	I	4-bit schmitter input with internal pull high option specified by PM3 register bit 2. Each pad has an independent interrupt capability specified by PEFL special register. Interrupt and STOP mode wake up source. RC0 is also the external event counter source of Timer1.
RD0 RD1/ADDR RD2/DATA RD3/CLK (4)	I	4-bit schmitter input port with internal pull high option specified by PM3 register bit 3. Each pad has an independent interrupt capability specified by PEFH special register. Interrupt and STOP mode wake up source. RD1~3 will be shared as the external memory W55XXX interface pads while RD port shared as serial bus mask option is enabled. "Tri-state serial bus" mask option can use to float CLK/ADDR/SPDATD while "RD port shared as serial bus" mask option is enabled.
RE0~RE3 (8)	O	Output port only. PM3 register bit 0 can be used to specify CMOS/NMOS driving capability option. (W536Q090/Q120 only)
RF0~RF3 (8)	O	Output port only. PM3 register bit 1 can be used to specify CMOS/NMOS driving capability option. (W536Q090/Q120 only)
$\overline{\text{RES}}$	I	System reset pad, active low with internal pull-high resistor.
TEST	I	Test pad. Active high with internal pull low resistor.

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PAD Description, continued

SYMBOL	I/O	FUNCTION
ROSC	I	Connect resistor to V_{DD} pad to generate speech or melody playing clock source.
PWM1/DAC	O	While speech or melody is active, PWM1/DAC is speaker direct driving output or DAC output controlled by voice output file.
PWM2	O	While speech or melody is active, PWM2 is another speaker direct driving output.
ADDR (5)	O	External serial memory address write clock for voice extension (W536Q120 only).
CLK (5)	O	External serial memory address read clock for voice extension. (W536Q120 only).
DATA (5)	I/O	External serial memory data in/out for voice extension (W536Q120 only).
SEG24−SEG39	O	Dedicated LCD segment output pads.
SEG40/PORTN.0 | SEG43/PORTN.3	O/O	LCD segment output pads, and can be shared as general output by register LCDM3 bit 1. Default function is segment pad.
SEG44/PORTM.0 | SEG47/PORTM.3	O/I	LCD segment output pads, and can be shared as general input by register LCDM3 bit 0. Default function is segment pad and PM5.1=0 to inhibit LCD waveform abnormal.
SEG48/PORTL.0 | SEG51/PORTL.3	O/O	LCD segment output pads, and can be shared as general output by register LCDM2 bit 3. Default function is segment pad.
SEG52/PORTK.0 | SEG55/PORTK.3	O/I	LCD segment output pads, and can be shared as general input by register LCDM2 bit 2. Default function is segment pad and PM5.0 = 0 to inhibit LCD waveform abnormal.
SEG56/PORTJ.0 | SEG59/PORTJ.3	O/IO	LCD segment output pads, and can be shared as general input/output by register LCDM2 bit 1. PM4 register is used to select input or output while shared I/O function is active. Default function is segment pad and PM4.3 = 0 to inhibit LCD waveform abnormal.
SEG60/PORTI.0 | SEG63/PORTI.3	O/IO	LCD segment output pads, and can be shared as general input/output by register LCDM2 bit 0. PM4 register is used to select input or output while shared I/O function is active. Default function is segment pad and PM4.2 = 0 to inhibit LCD waveform abnormal.

PAD Description, continued

SYMBOL	I/O	FUNCTION
COM0–COM7	O	LCD common signal output pads either 1/16 duty or 1/8 duty. The LCD frame rate is controlled by LCDM1 register, and default value LCDM1 = 0111b with 64Hz frame rate.
COM8 / PORTP.0 | COM11/PORTP.3	O/O	LCD common signal output pads, or shared as general output by register LCDM3.2 when in 1/8 duty mode. Default function is common function.
COM12/PORTO.0 | COM15/PORTO.3	O/I	LCD common signal output pads, or shared as general input by register LCDM3.2 when in 1/8 duty mode. Default function is common function and PM5.2 = 0 to inhibit LCD waveform abnormal.
DH1, DH2 (6)	O	Connection terminal for voltage double capacitor with 0.1uF. The DH2 connects to capacitor positive node and DH1 negative node if polar capacitor is used.
V3 ~ V6 (6)	O	LCD COM/SEG output driving voltage. Need an external 0.1uF capacitor to every pad terminal.
V2 (6)	I/O	Voltage regulator output pad. An external capacitor is a must. Output level can be controlled from 0~Fh by LCDM4 register. If internal pump is enabled (LCDM3.3 = 0 and default value), LCD operating voltage (VLCD) will be 4*V2 or 5*V2 depending on 1/4 bias or 1/5 bias. A limitation should be noted that VLCD must be higher than (V_{DD} -0.5v) to avoid chip leakage current. While external reference voltage is selected (LCDM3.3 = 1), V2 pad input voltage cannot be over 1.5 Volt to inhibit chip damage.
V_{SSP} (7)	I	Power ground for PWM or DAC playing output.
V_{SS} (7)	I	Power ground
V_{DDP} (7)	I	Power source for PWM or DAC playing output.
V_{DD} (7)	I	Power source.

Notes:

(4)   RD1~3 are shared as ADDR/DATA/CLK to interface with W55XXX

(5)   W536Q120 only

(6)   0.1uF is default value, and capacitor value should be larger than 0.1uF if LCD dot size over 0.5mm * 0.5mm.

(7)   External application circuit should connect together, please refer to APPLICATION CIRCUIT. To sure chip operation properly, please bond all V_{DD}, V_{DDP}, V_{SS} and V_{SSP} pads and connect V_{SS} and V_{SSP} from chip outside PCB circuit.

(8)   When working at NMOS open drain mode, external pull high voltage can't higher than VDD to avoid leakage current.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 DC Characteristics

(V_{DD}–V_{SS} = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD panel on with dot size 0.5mm*0.5mm; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Op. Voltage	V_{DD}		2.4		5.5	V
Op. Current (No Load, no Voice, no Melody)	I_{OP1}	Dual clock with crystal	-	600	700	μA
		Dual clock with RC type		600	700	
		Sub-clock only, LCD off		40	50	
		Sub-clock only, LCD on		70	90	
Hold Mode Current (No Load, LCD OFF)	I_{OP2}	Sub-clock active only		6	10	μA
Hold Mode Current (No load, LCD ON)	I_{OP3}	Sub-clock active only			70	μA
Stop Mode Current	I_{OP4}	LCD auto off			1	μA
ADDR/CLK Output High Current	I_{OH1}	Vout = 2.7V			-0.8	mA
ADDR/CLK Output low Current	I_{OL1}	Vout = 0.4V			0.8	mA
Input Low Voltage	V_{IL}	-	V_{SS}	-	0.3	V_{DD}
Input High Voltage	V_{IH}	-	0.7	-	1	V_{DD}
Port RA, RB, RE, RF Output Low Voltage	V_{ABL}	IOL = 2.0 mA	-	-	0.4	V
Port RA, RB, RE, RF Output High Voltage	V_{ABH}	IOH = -2.0 mA	2.4	-	-	V

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Ports (I, J, L, N, P) Output Sink Current	I_{OL3}	V_{OL} = 0.4V	-300			μA
Pull-up Resistor	R_D	Port RD	200	300	400	KΩ
RES Pull-up Resistor	R_{RES}	-	50	100	200	KΩ
PWM1/2 Source Current (9) (R_{LOAD} = 8Ω between PWM1 And PWM2)	I_{SPH}	Volume Option = 00		-20		mA
		Volume Option = 01		-70		
		Volume Option = 10		-110		
		Volume Option = 11		-135		
PWM1/2 Sink Current (9) (R_{LOAD} = 8Ω between PWM1 And PWM2)	I_{SPL}	Volume Option = 00		20		mA
		Volume Option = 01		70		
		Volume Option = 10		110		
		Volume Option = 11		135		
DAC output Current	I_{DAC}	V_{DD} = 3v, RL = 100ohm	-4	-5	-6	mA
LCD Supply Current	I_{LCD}	No Load, All Seg. ON	-	50	-	μA
COM/SEG On Resistor	R_{ON}	IOH = $\pm$50 μA		5K	10K	Ω
V2 Pad Output Voltage	V_{RR}	Depended on LCDM4	0.7		1.45	V
V2 Pad Output Deviation (10)	V_{D1}	No Load			$\pm$ 5	%
V2 Pad Voltage Step	V_{R2}	LCDM4 increased 1		50		mV
V6 Pad Output Voltage (LCD's VLCD depended on LCDM4 register) (10)	V_{LCD}	1/4 Bias & no load	3.8 * V2	3.85 * V2	3.9 * V2	V
		1/5 Bias & no load	4.75 * V2	4.8 * V2	4.85 * V2	
V2 input voltage	V_{EXT}	LCDM3.3 = 1			1.5	V

Notes:

(9)   PWM current deviation will be $\pm$20%.

(10)   Deviation is governed by LCD dot size. More larger LCD dot will get larger deviation..

5.3 AC Characteristics

(V_{DD}–V_{SS} = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD on with dot size 0.5mm*0.5mm; unless otherwise specified)

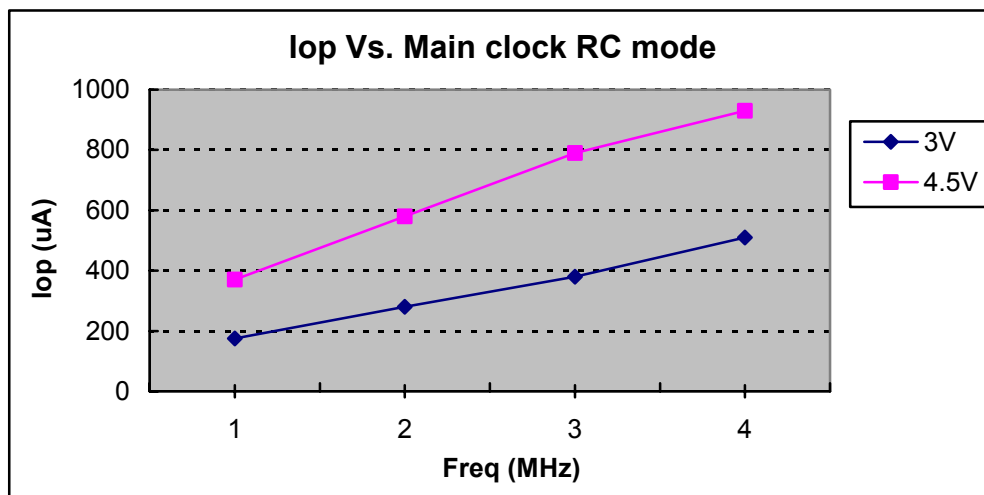| PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	F_{SUB}	Crystal type and X32IN and X32O with 17pF external cap.		32768		Hz
Main-clock Frequency	F_M	RC type/Crystal type	400K	-	4M	Hz
Chip Operation Frequency	F_{OSC}	SCR0.0 = 1, F_{SYS} = F_{SUB}		32768		Hz
		SCR0.0 = 0; F_{SYS} = F_{MAIN}	400K	-	4M	
Instruction Cycle Time	T_{CYC}	One machine cycle	-	4/F_{OSC}	-	S
Reset Active Width	T_{RAW}	FOSC = 32.768 KHz	1	-	-	μS
Interrupt Active Width	T_{IAW}	FOSC = 32.768 KHz	1	-	-	μS
Main clock RC Frequency (11)	F_{RXIN}	RXIN = 680KΩ		1M		Hz
		RXIN = 330K Ω		2M		
		RXIN = 200KΩ		3M		
		RXIN = 150KΩ		4M		
Sub-Clock Ring Oscillator	F_{RSUB}	RSUB = 680KΩ		32		KHz
Sub-Clock Oscillation Stable Time @ Cold Start	F_{STOP}	RSUB = 680KΩ	0.8		1	S
Frequency Deviation of main-clock F_{RXIN} $\leq$ 2MHz	$\dfrac{\Delta f}{f}$	$\dfrac{f(3V) - f(2.4V)}{f(3V)}$			10	%
Frequency Deviation of main-clock F_{RXIN} = 3 MHz	$\dfrac{\Delta f}{f}$	$\dfrac{f(3V) - f(2.4V)}{f(3V)}$			15	%
Frequency Deviation of main-clock F_{RXIN} = 4 MHz	$\dfrac{\Delta f}{f}$	$\dfrac{f(3V) - f(2.4V)}{f(3V)}$			20	%
ROSC Frequency	F_{ROSC}	ROSC = 680KΩ		3		MHz
Frequency Deviation of F_{ROSC} = 3 MHz	$\dfrac{\Delta f}{f}$	$\dfrac{f(3V) - f(2.4V)}{f(3V)}$			7.5	%
Frame frequency	F_{LCD}	LCDM1 = 0111b(default)		64		Hz

Notes:

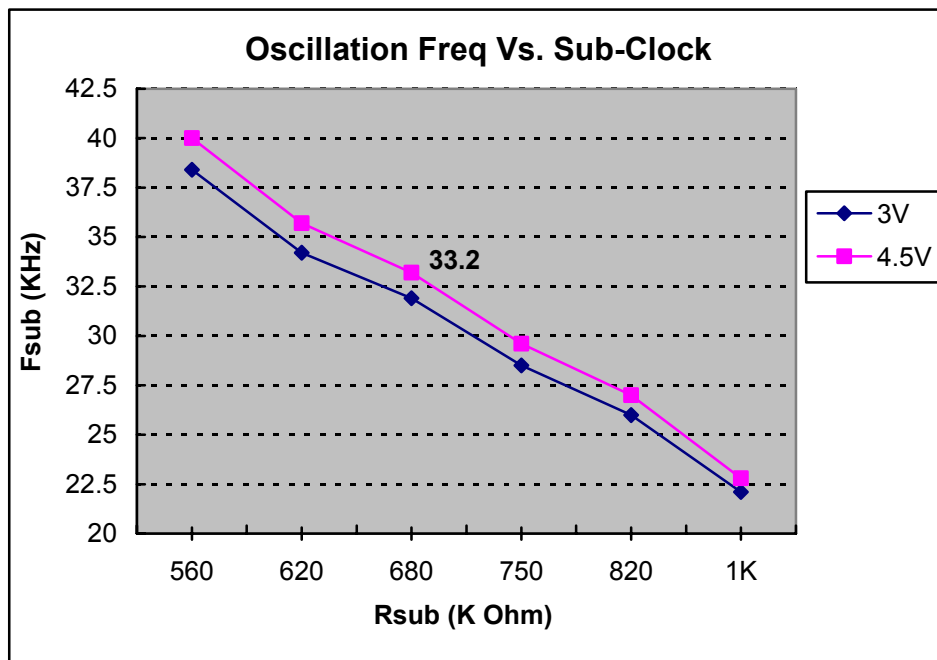(11) The deviation will be +20% while VDD drops from 5.5V to 2.4V based on same resistor
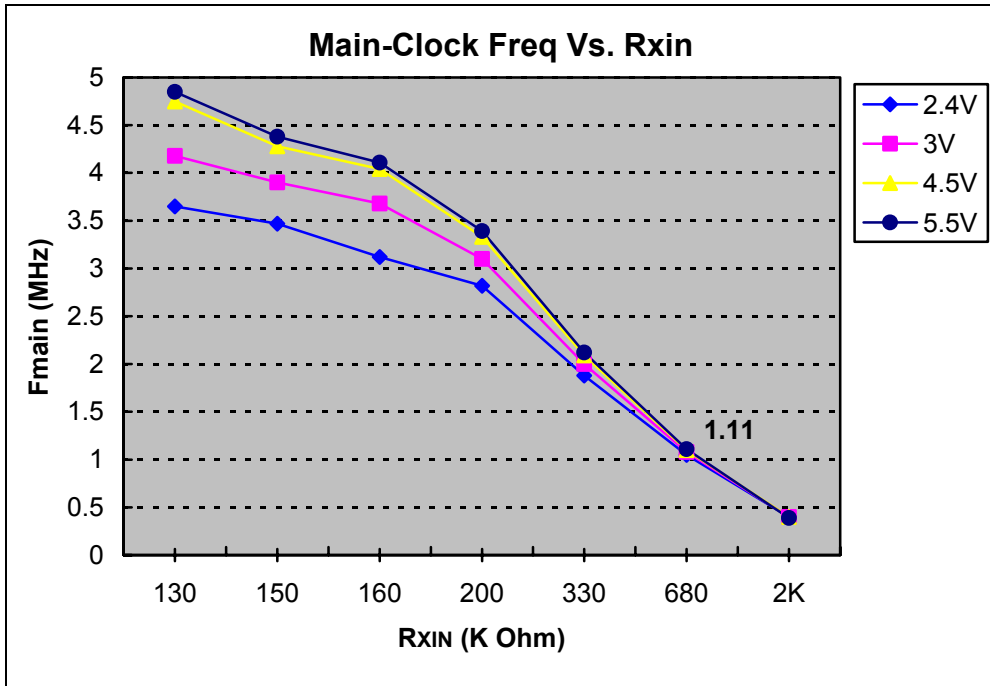
Operating Current Vs. Main clock (RC Mode)

Iop Vs. Main clock RC mode

Sub-Clock oscillation Freq Vs. Resistor

Oscillation Freq Vs. Sub-Clock

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Main-Clock oscillation Freq Vs. Resistor

Main-Clock Freq Vs. Rxin

- 2.4V
- 3V
- 4.5V
- 5.5V

Fmain (MHz) / Rxin (K Ohm)

1.11

Voice Operating Freq Vs. Resistor (ROSC)

Voice Operating Freq. Vs. ROSC

- 3V
- 4.5V

Freq (MHz) / ROSC (K Ohm)
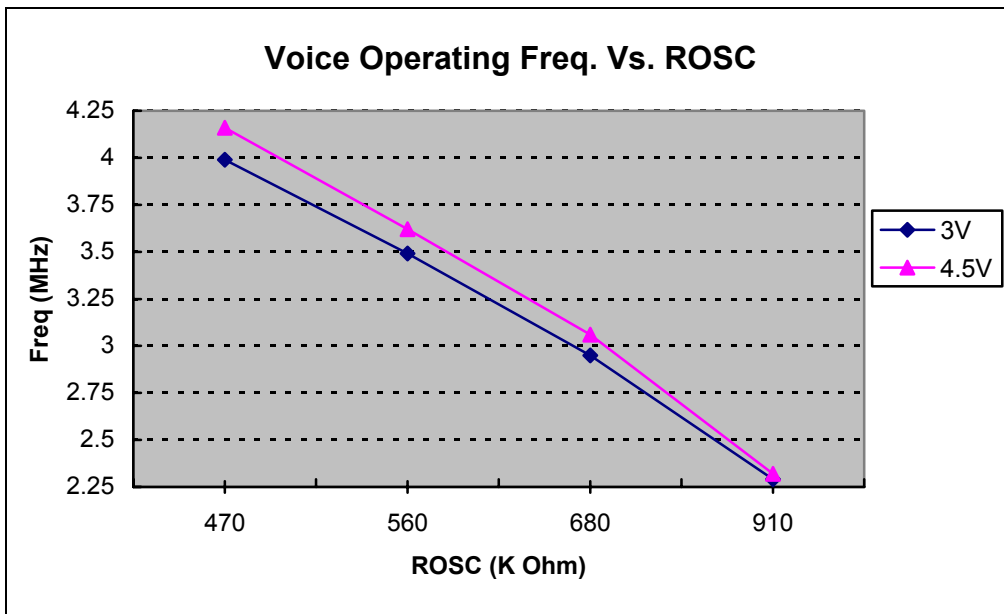
6. TYPICAL APPLICATION CIRCUITS

6.1 Sub Clock with RC Mode
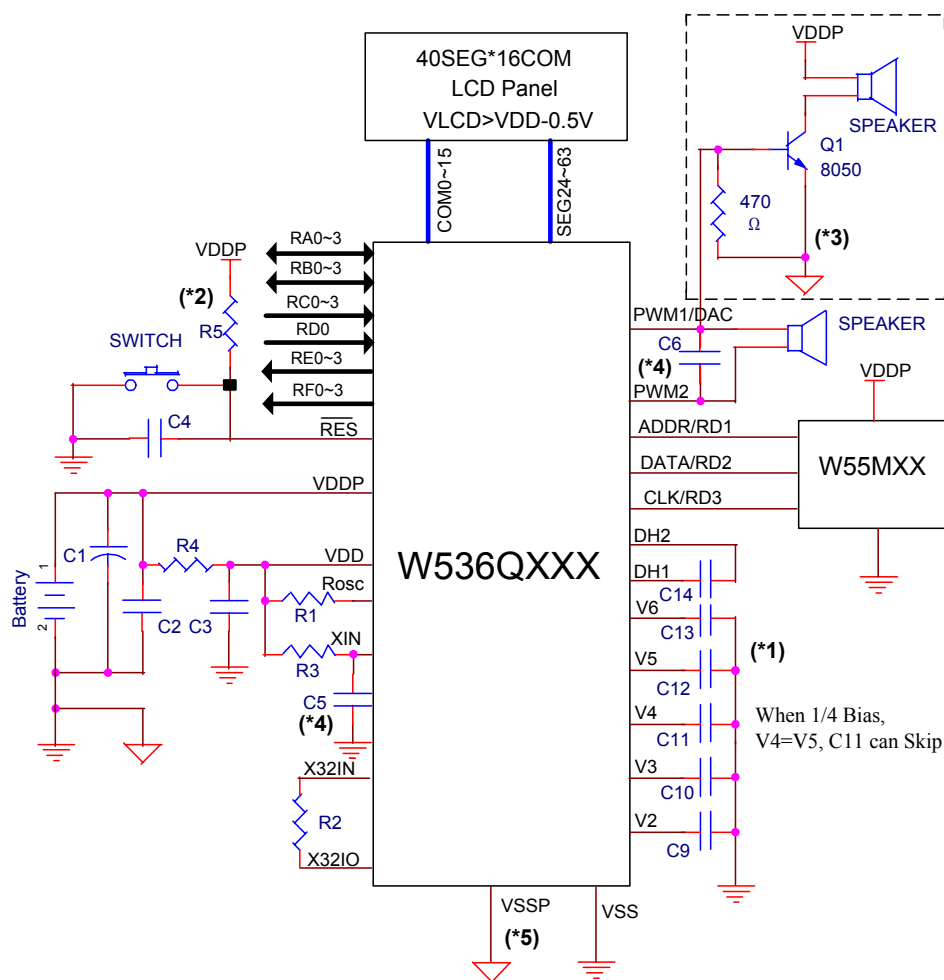
COMPONENT	C1	C2~C4	C5, C6	C7, C8	C9~C14	R1	R2	R3	R4
Value	4.7uF	0.1uF	100pF	15~ 30pF	0.1~1uF	680KΩ	680KΩ	650KΩ/1MHz 350KΩ/2MHz 225KΩ/3MHz 160KΩ/4MHz	100Ω

Notes:

1. C9~C14 depends on LCD panel dot size.
2. Option R5 equals to 100Ω if high noise immunity is needed.
3. For DAC option application.
4. To ensure that three batteries function well in W536F20 demo board. C_6 should stay close to pad PWM/PWM2 at its best. Under the mask ROM version, C_5 and C_6 can be skipped.
5. Sure chip operation properly, please bond all V_{DDP}, V_{DD}, V_{SSP} and V_{SS}; and connect V_{SSP} pad to V_{SS} from external PCB circuit.
6. Main clock with Ring type, the frequency deviation is depended on VDD and resistor

6.2 Sub Clock with Crystal Mode

40SEG*8COM
LCD Panel
VLCD>VDD-0.5V

COM0~7   SEG24~63

VDDP   SPEAKER   Q1 8050   470Ω   (*3)

VDDP
(*2)
SWITCH   R5
C4
RA0~3
RB0~3
RC0~3
RD0
RE0~3
RF0~3
RES

PWM1/DAC   SPEAKER
C6
(*4)
PWM2   VDDP
ADDR/RD1
DATA/RD2   W55MXX
CLK/RD3
DH2
DH1
V6   C14
C13
V5   (*1)
C12
V4   When 1/4 Bias,
C11   V4=V5, C11 can Skip
V3
C10
V2
C9

VDDP
Battery   C1   R4   VDD
Rosc
C2 C3   R1
XIN
R3
C5
(*4)
X32IN
C7
32K
X32IO
C8

W536QXXX

VSSP   VSS
(*5)
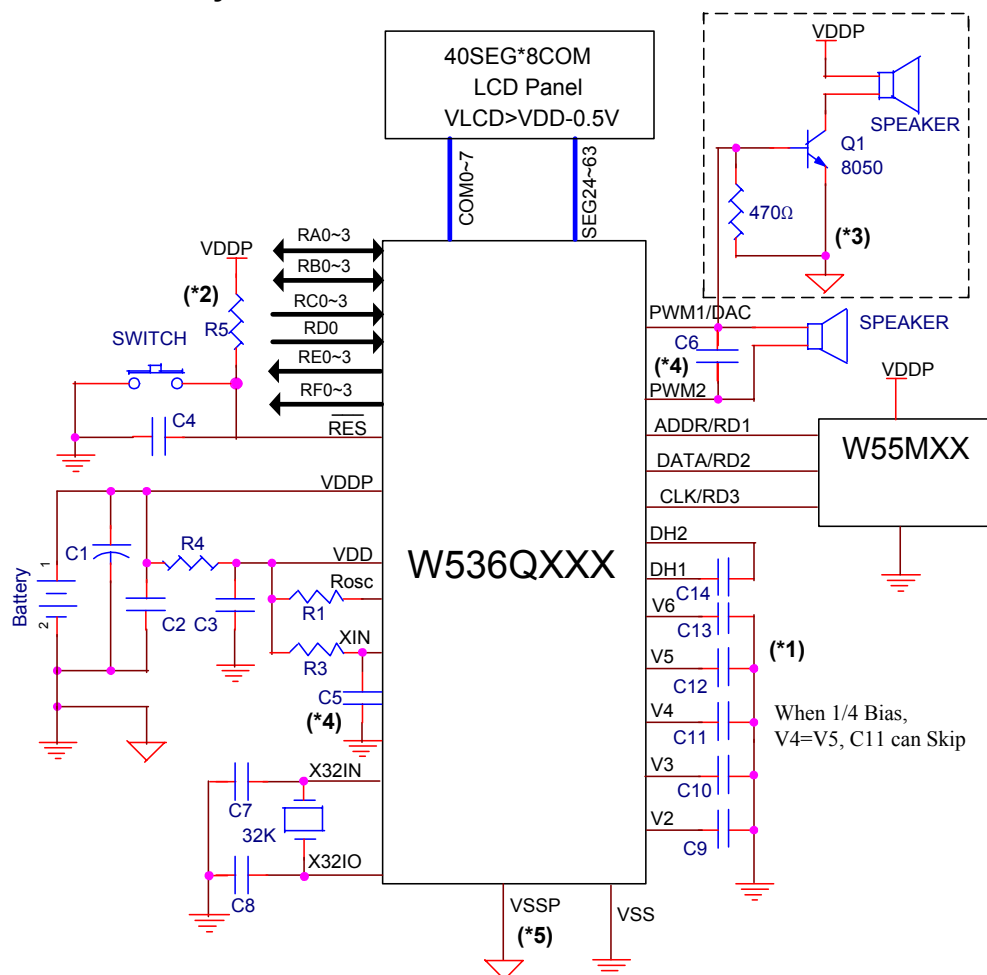
COMPONENT	C1	C2~C4	C5, C6	C7, C8	C9~C14	R1	R2	R3	R4
Value	4.7uF	0.1uF	100pF	15~ 30pF	0.1~1uF	680KΩ	-	650KΩ/1MHz 350KΩ/2MHz 225KΩ/3MHz 160KΩ/4MHz	100Ω

Note:

1. C9~C14 depends on LCD panel dot size.
2. Option R5 equals to 100Ω if high noise immunity is needed.
3. For DAC option application.
4. To ensure that three batteries function well in W536F20 demo board. C_6 should stay close to pad PWM/PWM2 at its best. Under the mask ROM version, C_5 and C_6 can be skipped.
5. Sure chip operation properly, please bond all V_{DDP}, V_{DD}, V_{SSP} and V_{SS}; and connect V_{SSP} pad to V_{SS} from external PCB circuit.
6. Main clock with Ring type, the frequency deviation is depended on V_{DD} and resistor

7. REVISION HISTORY

VERSION	DATE	WRITER	DESCRIPTION
A1	Sep. 7, 2001	WTChu	• Establish
A2	May 20, 2003	WTChu	• Integrate for Q060/Q090/Q120