4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation 24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	−40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

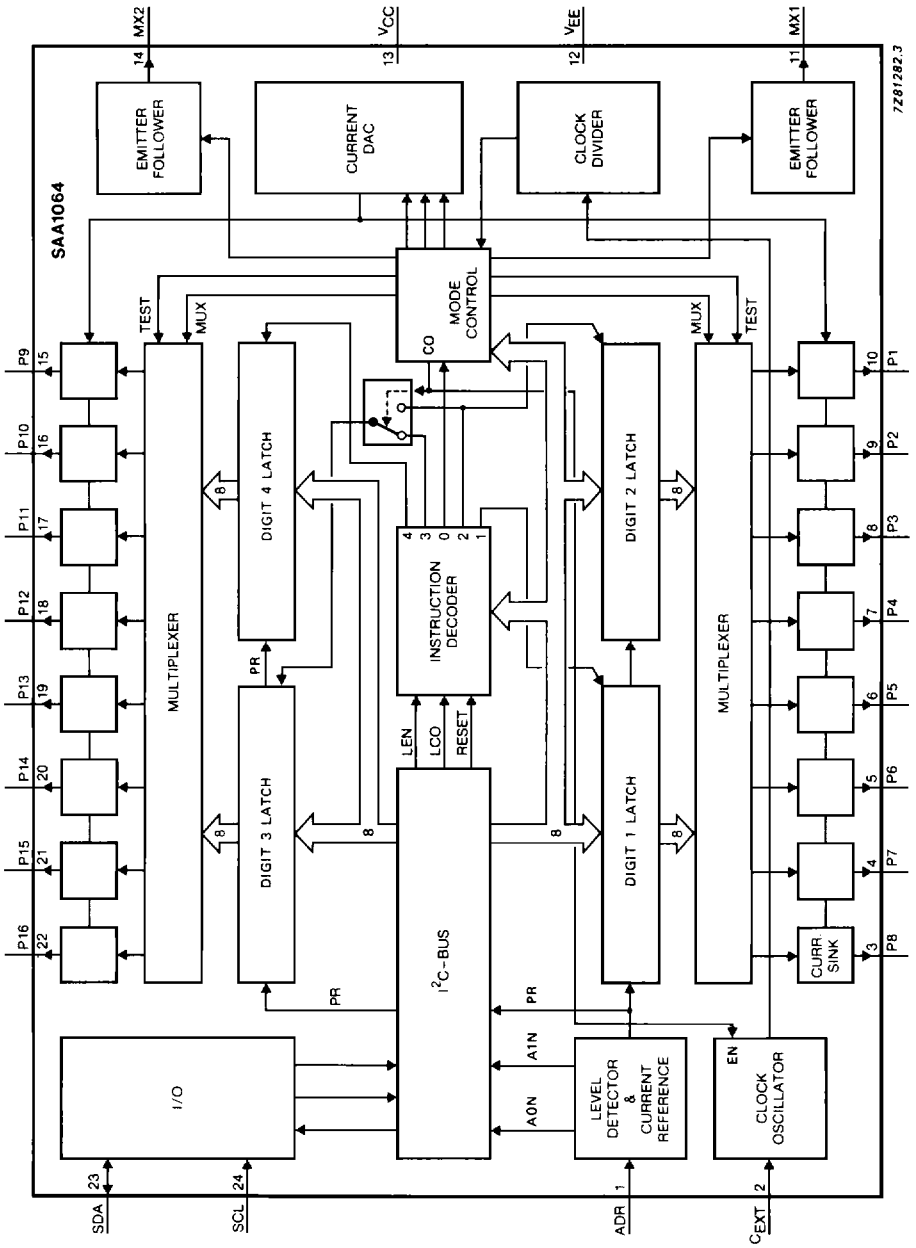


Fig. 1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

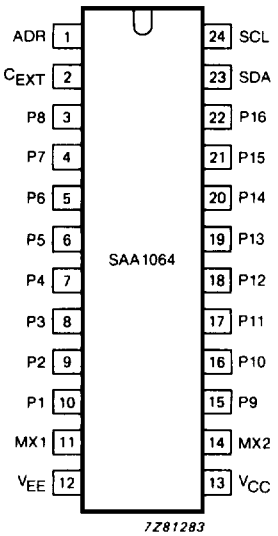


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

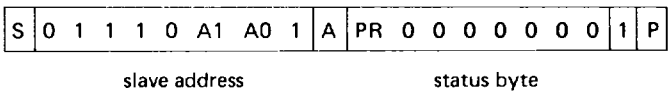


Fig. 3a I²C-Bus format; READ mode.

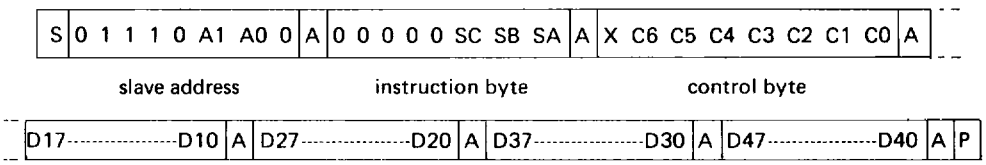


Fig. 3b I²C-Bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)	V_{EE} = 0 V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	V_{EE} = 0 V	$V_{23,24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	V_{EE} = 0 V	$V_{1\text{-}11}$, $V_{14\text{-}22}$	−0.5	V_{CC} + 0.5	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	−	10	mA
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\,j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\,j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\,j\text{-}a}$	105 K/W

CHARACTERISTICS

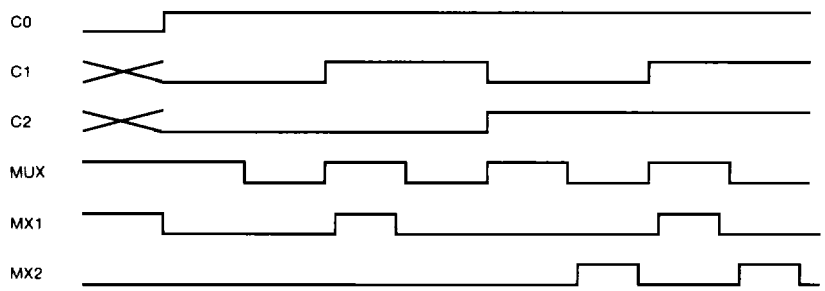
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	3/16V_{CC}	V
A0 = 1; A1 = 0		V_1	5/16V_{CC}	3/8V_{CC}	7/16V_{CC}	V
A0 = 0; A1 = 1		V_1	9/16V_{CC}	5/8V_{CC}	11/16V_{CC}	V
A0 = 1; A1 = 1		V_1	13/16V_{CC}	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	μA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}–3,3	V
Input voltage HIGH		V_{IH}	V_{CC}–1,5	–	–	V
Input current	V_2 = 2 V	I_2	–140	–160	–180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5 and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage (when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	$V_{CC}-1.5$	–	–	V
Maximum output current HIGH (when ON)	V_{MPX} = 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW (when OFF)	V_O = 2 V	$+I_{MPX}$	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.



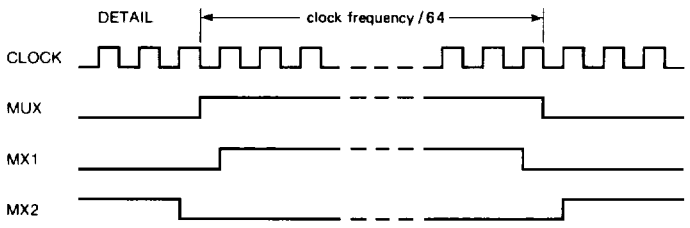


Fig. 4 Timing diagram.

APPLICATION INFORMATION

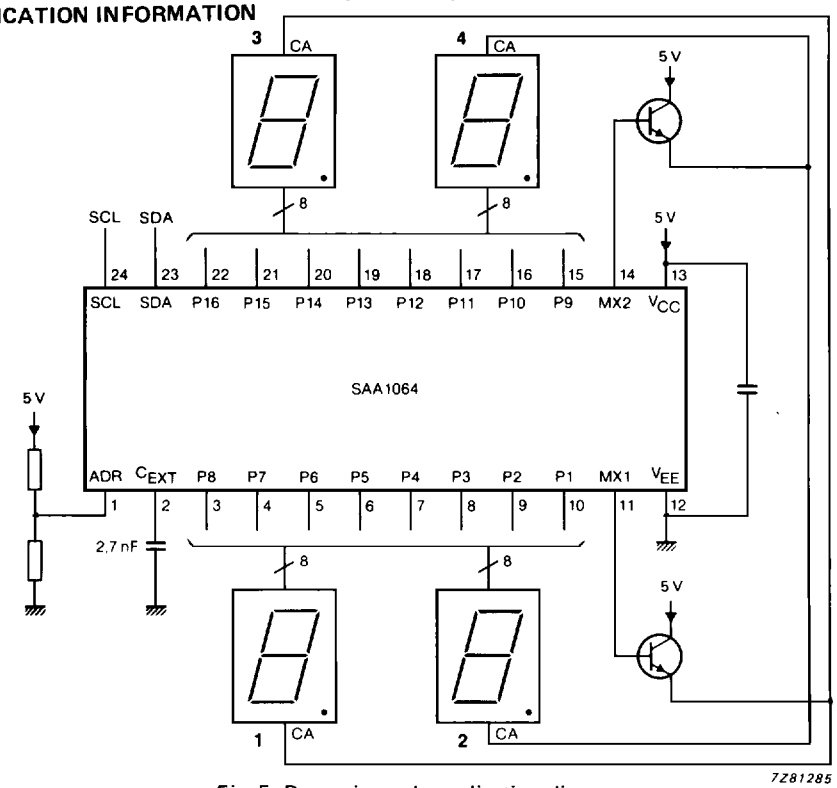


Fig. 5 Dynamic mode application diagram.

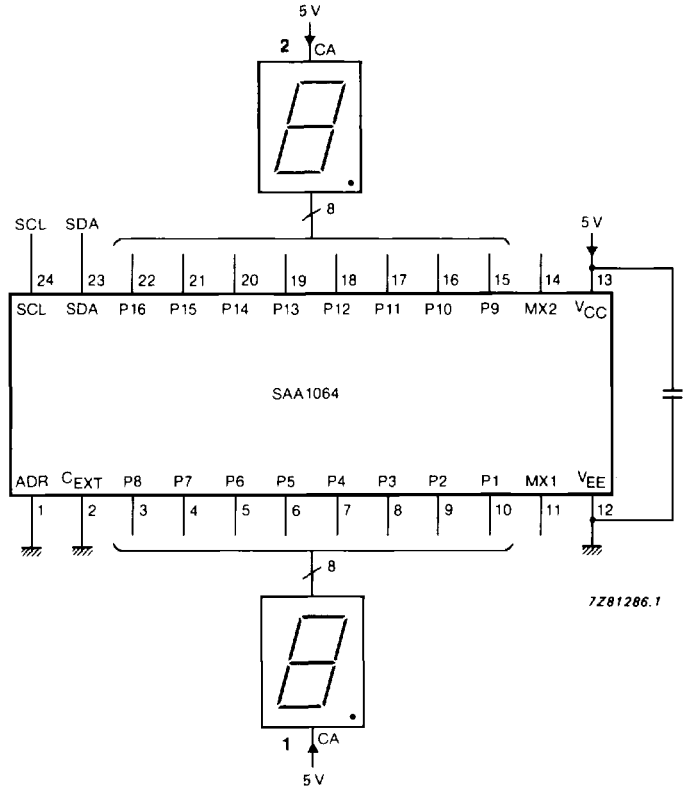


Fig. 6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_o \times I_o \times N$.

Where: P_{add} = The additional power dissipation of the segment drivers

V_o = The low state segment driver output voltage

I_o = The programmed segment output current

N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{cc} = 5 V

V_o = 0.25 V

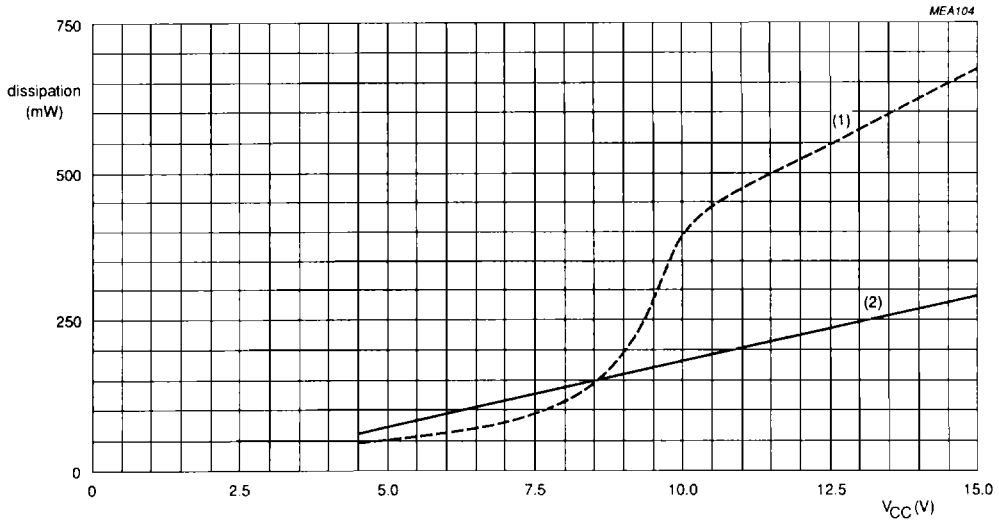
I_o = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).

(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.