Bitstream continuous calibration filter-DAC with headphone driver and DSP

TDA1548T

FEATURESPRODUCT SPECIFICATION

Easy application

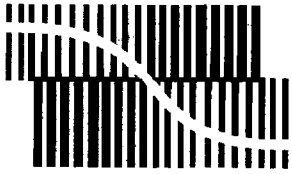
- Only first-order analog post-filtering required
- Headphone amplifiers and digital filter integrated
- Component saving common headphone output
- Selectable system clock (SYSCLK) $64f_s$, $256f_s$ or $384f_s$
- 16, 18 or 20 bits I^2S-bus or LSB justified serial input format
- Input pins suitable with 5 V low supply voltage interfacing
- Small package (SSOP28)
- Single rail supply (3 V).

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

Features

- Low power dissipation
- Digital volume control
- Soft mute
- Digital tone control (Bass Boost and Treble)
- Digital de-emphasis
- Analog control of digital sound control functions.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1548T is a dual CMOS digital-to-analog converter (DAC) with up-sampling filter and noise shaper and integrated headphone driver featuring unique signal processing functions. The digital processing features are of high sound processing quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1548T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB justified serial data input format with word lengths of 16, 18 or 20 bits. The clock system is selectable ($64f_s$, $256f_s$ or $384f_s$) by means of selection pins. Two cascaded half band filters, linear interpolator and a sample-and-hold function increase the oversampling rate from $1f_s$ to $64f_s$.
A second-order noise shaper converts this oversampled data into a bitstream for the 5-bit continuous calibration DACs.

On board amplifiers convert the output current to a voltage signal capable of driving a headphone or line output. The common operational amplifier application eliminates the need for capacitors.

The TDA1548T has some sound processing functions which are controllable by a potentiometer. These functions are volume, bass boost and treble. The flat/min/max switch can also be controlled by a potentiometer.
The analog values are converted to a digital code, which is then further translated internally to a set of coefficients for either volume, bass boost or treble.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1548T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA1548TZ	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.7	3.0	4.0	V
I_{DD}	supply current	note 2	–	15	–	mA
$V_{oFS(rms)}$	full-scale output voltage	V_{DD} = 3 V	0.57	0.64	0.71	V
(THD+N)/S	total harmonic distortion plus noise as a function of signal	0 dB signal	–	–65	–60	dB
			–	0.056	0.1	%
		0 dB signal; R_{OL} = 5 kΩ	–	–85	–78	dB
			–	0.006	0.013	%
		–60 dB signal; R_{OL} = 32 Ω or R_{OL} = 5 kΩ	–	–35	–30	dBA
			–	1.778	3.162	%
S/N	signal-to-noise ratio	A-weighted; at code 00000H	90	95	–	dBA
BR	input bit rate at data input	$f_{sys} = 384f_s$	–	$48f_s$	–	
		$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 64f_s$	–	$64f_s$	–	
f_{sys}	system clock frequency		2.048	–	18.432	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 3 V.

BLOCK DIAGRAM

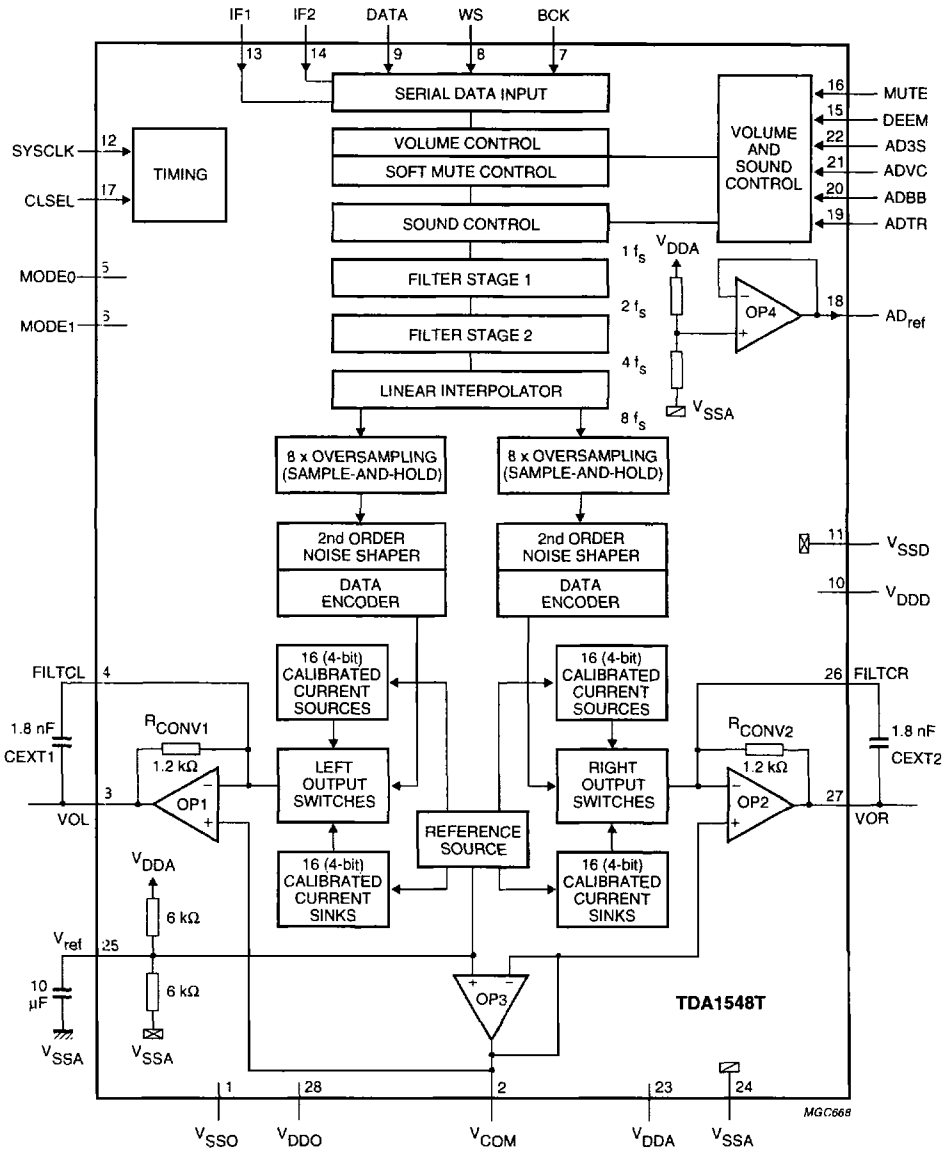


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSO}	1	operational amplifier ground
V_{COM}	2	common output pin
VOL	3	left channel audio voltage output
FILTCL	4	capacitor for left channel first-order filter function should be connected between this pin and VOL (pin 3)
MODE0	5	mode 0 selection pin
MODE1	6	mode 1 selection pin
BCK	7	bit clock input
WS	8	word select input
DATA	9	data input
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock $64f_s$, $256f_s$ or $384f_s$
IF1	13	input format selection 1
IF2	14	input format selection 2
DEEM	15	de-emphasis input (f_s = 44.1 kHz) (active HIGH)
MUTE	16	soft-mute input (active HIGH)
CLSEL	17	system clock selection input
AD_{ref}	18	reference voltage output to external potentiometer
ADTR	19	analog sense input for treble setting
ADBB	20	analog sense input for bass boost setting
ADVC	21	analog sense input for volume control setting
AD3S	22	3-position switch input for flat/min/max setting
V_{DDA}	23	analog supply voltage
V_{SSA}	24	analog ground
V_{ref}	25	internal reference voltage ($0.5V_{DDA}$ typ)
FILTCR	26	capacitor for right channel first-order filter function should be connected between this pin and VOR (pin 27)
VOR	27	right channel audio voltage output
V_{DDO}	28	operational amplifier supply voltage

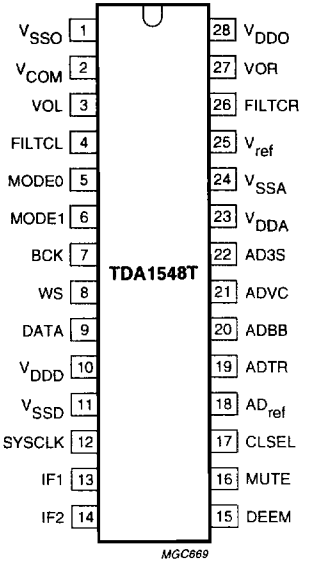


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1548T CMOS DAC incorporates an up-sampling digital filter, a linear interpolator, a noise shaper, continuous calibrated current sources and headphone amplifiers. The $1f_s$ input data is increased to an oversampling rate of $64f_s$. This high-rate oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple first-order analog post-filtering.

System clock and data input format

The TDA1548T accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable at pins CLSEL, MODE0 and MODE1 (see Table 1).

The TDA1548T supports the following data input modes (see Table 2):

I^2S-bus with data word length of up to 20 bits

LSB justified serial format with data word length of 16, 18 or 20 bits.

The input formats are illustrated in Fig.4. Left and right data-channel words are time multiplexed.

Analog control of digital sound processing features

Digital sound processing settings are controlled via analog sense inputs that translate an analog voltage from, for example, a potentiometer wiper to a digital code, which is then further translated internally to a set of coefficients for either treble, bass boost or volume.

The analog input value is acquired by an internal 6-bit ADC, sampling the three input pins ADVC, ADBB and ADTR and the three-mode selection pin ADS3 (see Section "Single pin three mode selection") in a multiplexed fashion. Sampling of the input voltage is performed by a straight forward technique of linear approximation; from the starting value of 0 V, an internal linear approximation voltage is incremented periodically in steps of 1/66th of the scale, with an internal comparator detecting when the approximation value oversteps the input value. Tolerance is built in at the top and bottom end of the scale by dimensioning the resistive elements at the top and bottom of the ladder equals 1R. Thus the ladder is built up of 64 elements of value R, two of value R, making a typical quantization step size of approximately 1.5 V (AD_{ref}) divided-by-66 (amount of Rs), equals 22.7 mV.

For each multiplexed timeslot the full approximation cycle is completed, immediately after which the next input will start being sampled.

The time slot for one input lasts 64 steps at a step advance rate of $8 \times f_s$, which amounts to 181 µs at f_s = 44.1 kHz. Because four inputs are multiplexed, the sample rate for each analog input is 1.38 kHz.

A buffered version of an internally generated reference voltage is available at output pin AD_{ref}. Because the internal AD derives from the same reference voltage, this allows for optimum mapping of the external analog control value onto the useful AD input voltage range. The idea is to bias a potentiometer to AD_{ref}, using a wiper to control the input voltage between 0 V and AD_{ref}. Hysteresis is implemented to improve noise immunity of the AD in order to prevent a stable setting of the potentiometer, to a point near a quantization threshold, from producing two alternating digital codes which could give rise to audible volume or boost changes. An hysteresis of 1 LSB is implemented digital. A shift in code must be at least 2 LSB either up or down from the current value, otherwise the internal digital code will remain at the current value.

SINGLE PIN THREE MODE SELECTION

A special input pin AD3S (pin 22), controls the mode in which the sound processing block operates. Not between two but three modes; whether the DSP should follow the AD inputs applying maximum effect, the minimum effect or overrule the boost effects thereby resulting in a flat frequency characteristic in the treble and bass boost sections.

Internally the same AD is used to detect the input level present at this pin as is used for the three sound control pins. An internal bias circuit containing of two MOSTs supplies a mid-range voltage so that this input can be operated with a minimum of external components. A HIGH or LOW input level is created by tying the pin to AD_{ref} or ground respectively, the intermediate value is achieved by leaving the pin open-circuit.

Volume control

Since there is no headroom included into the sound control section, the volume control precedes the sound control. Full volume and neutral setting (flat) of the sound control results in a full-scale output. Any tone boost will immediately cause clipping, which can be avoided by reducing the volume setting.

Soft mute

Soft mute is controlled by MUTE (pin 16). When the input is active HIGH the value of the sample is decreased smoothly to zero following a raised cosine curve. 32 coefficients are used to step down the value of the data, each one being used 32 times before stepping on to the next. This amounts to a mute transition time of 23 ms at f_s = 44.1 kHz. When MUTE is released (LOW), the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in the reverse order. Mute is synchronized to the sample clock, so that the operation always takes place on complete samples.

Digital sound processing features

BASS BOOST

A strong bass boost effect, which is useful in compensating for poor bass response of portable headphone sets, is implemented digitally in the TDA1548T and can be controlled by ADBB (pin 20) and AD3S (pin 22). Table 3 shows the bass boost values at different input voltages. Table 4 shows the selection mode status (flat/min/max) at different input voltages. Valid settings range from "flat" (no influence on audio) to +18 dB with step sizes of 2 dB in "minimum" and to +24 dB with step sizes of 2 dB in "maximum". The programmable bass boost filter is a second-order shelving type with a fixed corner frequency of 130 Hz for the "minimum" setting and a fixed corner frequency of 230 Hz for the "maximum" setting and has a Butterworth characteristic. Because of the exceptional amount of programmable gain, bass boost should be used in conjunction with adequate prior attenuation, using the volume control.

TREBLE

A treble effect is implemented digitally in the TDA1548T and can be controlled by ADTR (pin 19) and AD3S (pin 22). Table 3 shows the treble values at different input voltages. Table 4 shows the selection mode status (flat/min/max) at different input voltages. Valid settings range from "flat" (no influence on audio) to +6 dB with step sizes of 2 dB in "minimum" and to +6 dB with a step size of 2 dB in "maximum". The programmable treble filter is a first-order shelving type with a fixed corner frequency of 2.8 kHz for the "minimum" setting and a fixed corner frequency of 5.0 kHz for the "maximum" setting.

DE-EMPHASIS

De-emphasis is controlled by DEEM (pin 15). The digital de-emphasis filter is dimensioned to produce the de-emphasis frequency characteristics for the sample rate 44.1 kHz. With its 18-bit dynamic range, the digital de-emphasis of the TDA1548T is a convenient and component-saving alternative to analog de-emphasis.

When the DEEM pin is active HIGH, de-emphasis is enabled. De-emphasis is synchronized to the sample clock, so that operation always takes place on complete samples.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter. It consists of two sections which each increase the sample rate by 2.

The second order noise shaper operates at 64f_s. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique, used in combination with a sign-magnitude coding, enables high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit PDM bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1548T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is converted to a sign-magnitude code so that no current is switched to the output during digital silence (input 00000H). In this way very high signal-to-noise performance is achieved.

Component-saving stereo headphone driver

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a line output or headphone. The voltage is available at VOL and VOR (0.64 V RMS typical).

A major component saving feature of the TDA1548T is that no DC-blocking capacitors are needed in the application, despite the asymmetrical supply. The V_{COM} output, pin 2, is biased to the same voltage that the right and left channel voltage outputs are, V_{ref}, and is capable of sinking the sum of left and right channel load currents. Therefore, connecting a load between one of the outputs and V_{COM} only gives rise to a negligible amount of DC current through the load.

Table 1 System clock selection

PINS			DESCRIPTION
CLSEL	MODE0	MODE1	
0	0	0	$256f_s$
0	0	1	$64f_s$
0	1	X	reserved 1
1	0	0	$384f_s$
1	0	1	reserved 2
1	1	X	reserved 3

Table 2 Data input formats

PINS		FORMAT
IF1	IF2	
0	0	I^2S-bus
0	1	LSB justified, 16 bits
1	0	LSB justified, 18 bits
1	1	LSB justified, 20 bits

Table 3 Relationship between VC, BB and TR

ANALOG INPUT VALUES (V); PINS ADTR, ADBB AND ADVC	VOLUME (ADVC)	BASS BOOST (ADBB)		TREBLE (ADTR)	
		MAX.	MIN.	MAX.	MIN.
$AD_{ref} \times 65/66$	−0	0	0	0	0
$AD_{ref} \times 64/66$	−0	0	0	0	0
$AD_{ref} \times 63/66$	−1	0	0	0	0
$AD_{ref} \times 62/66$	−2	0	0	0	2
$AD_{ref} \times 61/66$	−3	2	2	2	2
$AD_{ref} \times 60/66$	−4	2	2	2	2
$AD_{ref} \times 59/66$	−5	4	4	2	2
$AD_{ref} \times 58/66$	−6	4	4	2	2
$AD_{ref} \times 57/66$	−7	6	6	4	4
$AD_{ref} \times 56/66$	−8	6	6	4	4
$AD_{ref} \times 55/66$	−9	8	8	4	4
$AD_{ref} \times 54/66$	−10	8	8	4	4
$AD_{ref} \times 53/66$	−11	10	10	6	6
$AD_{ref} \times 52/66$	−12	10	10	6	6
$AD_{ref} \times 51/66$	−13	12	12	6	6
$AD_{ref} \times 50/66$	−14	12	12	6	6
$AD_{ref} \times 49/66$	−15	14	14	....	....
$AD_{ref} \times 48/66$	−16	14	14	....	....
$AD_{ref} \times 47/66$	−17	16	16	....	....
$AD_{ref} \times 46/66$	−18	16	16	....	....
$AD_{ref} \times 45/66$	−19	18	18	....	....
$AD_{ref} \times 44/66$	−20	18	18	....	....
$AD_{ref} \times /4366$	−21	20	18	....	....
$AD_{ref} \times 42/66$	−22	20	18	....	....
$AD_{ref} \times 41/66$	−23	22	....	....	....
$AD_{ref} \times 40/66$	−24	22	....	....	....
$AD_{ref} \times 39/66$	−25	24	....	....	....

ANALOG INPUT VALUES (V); PINS ADTR, ADBB AND ADVC	VOLUME (ADVC)	BASS BOOST (ADBB)		TREBLE (ADTR)	
		MAX.	MIN.	MAX.	MIN.
$AD_{ref} \times 38/66$	−26	24	....	....	....
$AD_{ref} \times 37/66$	−27	....	....	....	....
$AD_{ref} \times 36/66$	−28	....	....	....	....
....	....	....	....	....	....
....	....	....	....	....	....
$AD_{ref} \times 5/66$	−59	24	18	6	6
$AD_{ref} \times 4/66$	−60	24	18	6	6
$AD_{ref} \times 3/66$	$-\infty$	24	18	6	6
$AD_{ref} \times 2/66$	$-\infty$	24	18	6	6

Table 4 Relationship mode selection

ANALOG INPUT VALUE (V); PIN AD3S	FLAT, MINIMUM OR MAXIMUM
$AD_{ref} \times 65/66$	flat
$AD_{ref} \times 64/66$	flat
....	....
....	....
$AD_{ref} \times 51/66$	flat
$AD_{ref} \times 50/66$	flat
$AD_{ref} \times 49/66$	minimum
$AD_{ref} \times 48/66$	minimum
....	....
....	....
$AD_{ref} \times 19/66$	minimum
$AD_{ref} \times 18/66$	minimum
$AD_{ref} \times 17/66$	maximum
$AD_{ref} \times 16/66$	maximum
....	....
....	....
$AD_{ref} \times 3/66$	maximum
$AD_{ref} \times 2/66$	maximum

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.5	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	note 2	−3000	+3000	V
		note 3	−300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor. Pin 18 = −1500 V (min) and +1500 V (max).
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO28	60	K/W
	SSOP28	80	K/W

QUALITY SPECIFICATION

In accordance with UZW-BO/FQ-0601. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The Handbook can be ordered using the code 9397 750 00192.

DC CHARACTERISTICS

All voltages referenced to ground (pins 1, 11 and 24); $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C, $R_L = 32\ \Omega$ (note 1); common operational amplifier application; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage pin 10	note 2	2.7	3.0	4.0	V
V_{DDA}	analog supply voltage pin 23	note 2	2.7	3.0	4.0	V
V_{DDO}	opamp supply voltage pin 28	note 2	2.7	3.0	4.0	V
I_{DDD}	digital supply current	at digital silence	–	4.5	–	mA
I_{DDA}	analog supply current	at digital silence	–	4.5	–	mA
I_{DDO}	opamp supply current	at digital silence; note 3	–	6.0	–	mA
P_{tot}	total power dissipation	note 3	–	50	–	mW
Digital inputs						
V_{IH}	HIGH level input voltage on pins 5 to 9 and 12 to 17		$0.7V_{DDD}$	–	–	V
V_{IL}	LOW level input voltage on pins 5 to 9 and 12 to 17		–	–	$0.3V_{DDD}$	V
$\lvert I_{LI}\rvert$	input leakage current on pins 7 to 9 and 12 to 17		–	–	10	µA
C_I	input capacitance on pins 5 to 9 and 12 to 17		–	–	10	pF
Analog inputs pins ADVC, ADBB, ADTR and AD3S						
RES	input resolution		–	–	6	bit
C_I	input capacitance		–	10	–	pF
R_I	input resistance	pins ADBB, ADTR and ADVC	1	–	–	MΩ
		pin AD3S	–	20	–	kΩ
Analog reference pin AD_{ref}						
V_{ADref}	reference voltage pin 18		$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{L(ADref)}$	reference output load pin 18		3.0	–	–	kΩ
Analog audio pins						
V_{ref}	reference voltage pin 25	with respect to V_{SSO}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
R_O	output resistance pin 25		–	3	–	kΩ
R_{CONV}	current-to-voltage conversion resistor		–	1.2	–	kΩ
$I_{O(max)}$	maximum output current	(THD + N)/S < 0.1%	–	35	–	mA
C_L	output load capacitance	note 4	–	–	50	pF

Notes

1. R_L is the AC impedance of the external circuitry connected to the audio outputs of the application circuit.
2. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
3. No operational amplifier load resistor.
4. Load capacitance greater than 50 pF, an inductor of 22 µH connected in parallel with a resistor of 270 Ω must be inserted between the load and the operational amplifier output.

AC CHARACTERISTICS (ANALOG)

All voltages referenced to ground (pins 2, 9 and 23); $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C, $R_L = 32\ \Omega$ (note 1); common operational amplifier application; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES	input resolution		–	–	18	bit
f_{sAD}	AD sample frequency		–	$f_s/32$	–	kHz
V_{ADref}	input voltage range		0	–	V_{ADref}	V
$V_{FS(rms)}$	output voltage swing (RMS value) (pins 3 and 27)		0.57	0.64	0.71	V
$V_{DC(os)}$	DC offset output voltage w.r.t. reference voltage level V_{ref}		–	20	–	mV
TC_{FS}	full scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	$C_{25} = 10\ \mu F$; $f_{ripple} = 1$ kHz; $V_{ripple} = 100$ mV (peak)	–	40	–	dB
UNBAL	unbalance between the 2 DAC voltage outputs (pins 3 and 27)	maximum volume	–	0.1	–	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs (pins 3 and 27)	one output digital silence the other maximum volume	–	50	–	dB
		one output digital silence the other maximum volume $R_L = 5\ k\Omega$	–	90	–	dB
	crosstalk between the 2 DAC voltage outputs (pins 3 and 27) with R_L connected to ground	one output digital silence the other maximum volume	–	70	–	dB
		one output digital silence the other maximum volume $R_L = 5\ k\Omega$	–	100	–	dB
(THD+N)/S	total harmonic distortion plus noise as a function of signal	0 dB signal	–	–65	–60	dB
			–	0.056	0.1	%
		0 dB signal; $R_L = 5\ k\Omega$	–	–85	–78	dB
			–	0.006	0.013	%
		–60 dB signal; $R_L = 32\ \Omega$ or $R_L = 5\ k\Omega$	–	–35	–30	dBA
			–	1.778	3.162	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 00000H	90	95	–	dBA

Note

1. R_L is the AC impedance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (DIGITAL)

All voltages referenced to ground (pins 2, 9 and 23); $V_{DDD} = V_{DDA} = V_{DDO} = 2.7$ to 4.0 V; $T_{amb} = +70$ °C, $R_L = 32\ \Omega$ (note 1); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{cy}	clock cycle	$f_{sys} = 384f_s$	54.2	59.1	81.3	ns
		$f_{sys} = 256f_s$	81.3	88.6	122	ns
		$f_{sys} = 64f_s$	325.5	354.3	488.3	ns
$t_{CW(L)}$	f_{sys} LOW level pulse width		22	–	–	ns
$t_{CW(H)}$	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.3)						
BR	clock input = data input rate	$f_{sys} = 384f_s$	–	$48f_s$	–	
		$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 64f_s$	–	$64f_s$	–	
f_{sys}	system clock frequency		2.048	–	18.432	MHz
f_{WS}	word select input frequency		–	44.1	48.0	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		20	–	–	ns
$t_{h;DAT}$	data hold time		10	–	–	ns
$t_{s;WS}$	word select set-up time		20	–	–	ns
$t_{h;WS}$	word select hold time		10	–	–	ns

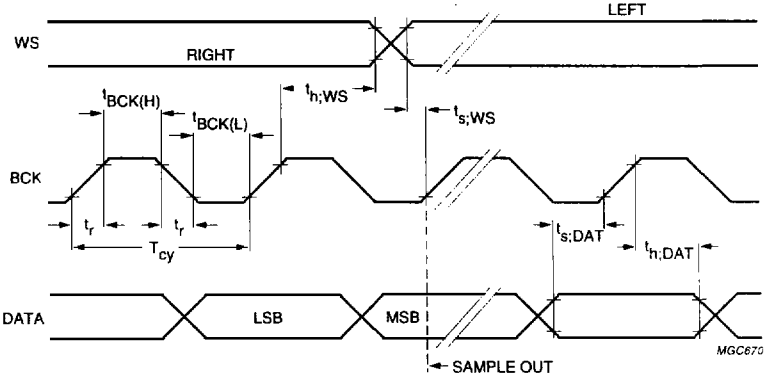


Fig.3 Timing of input signals.

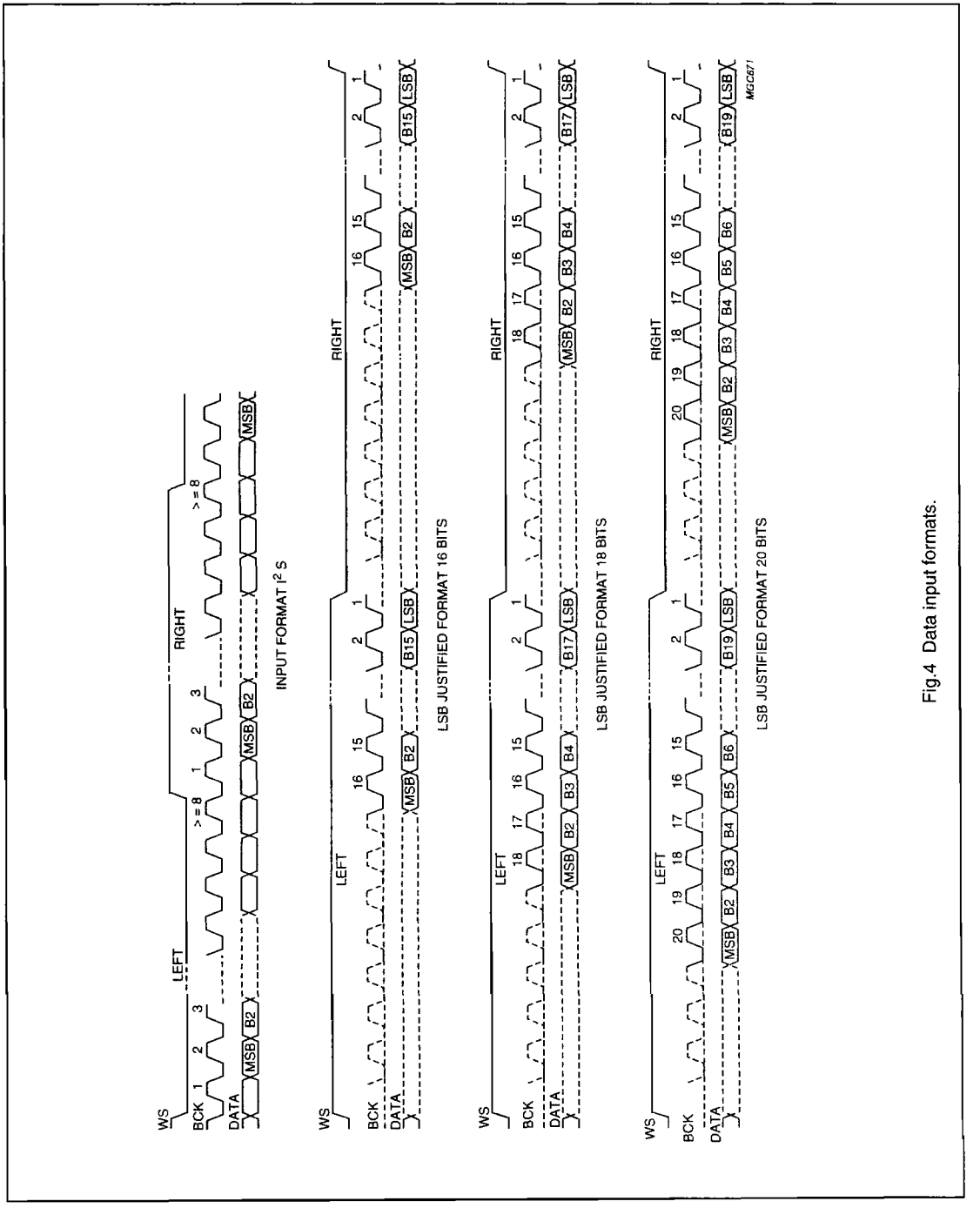


Fig.4 Data input formats.

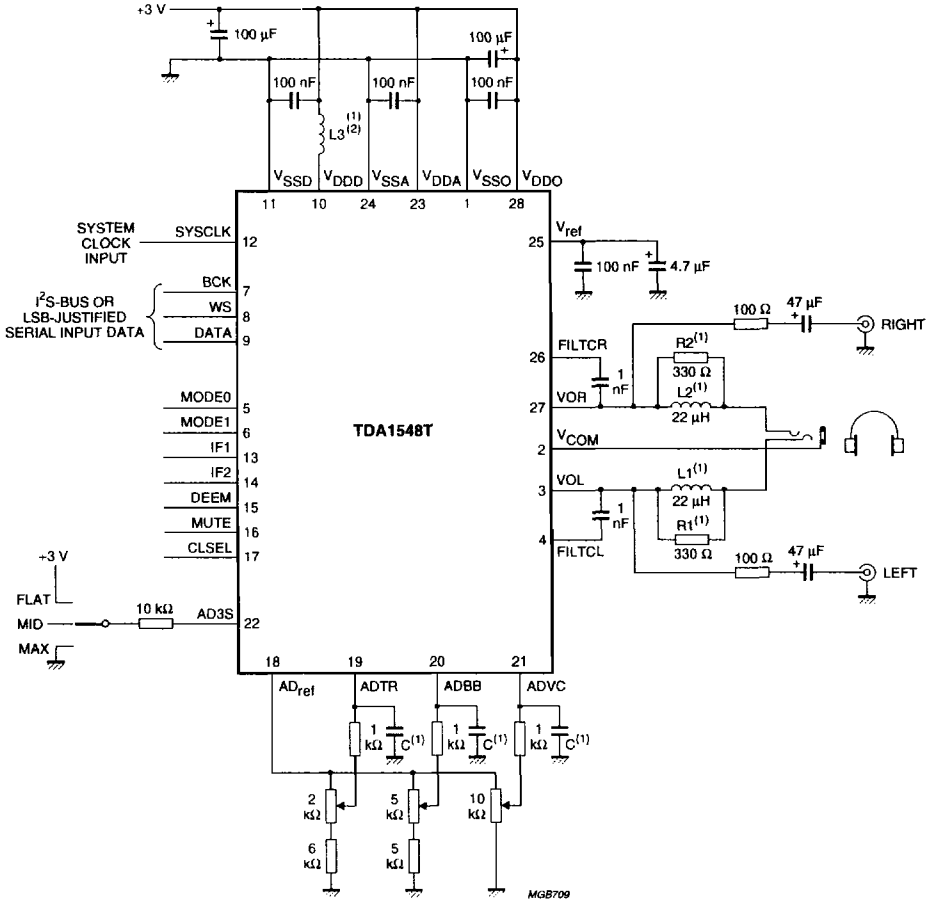
TEST AND APPLICATION INFORMATION

Filter characteristics

Table 5 Digital filter characteristics (f_s = 44.1 kHz)

The band frequencies scale with the sample frequency.

BAND	ATTENUATION
0 to 20 kHz	< 0.001 dB
24 to 64 kHz	> 39 dB
64 to 69 kHz	> 33 dB
69 to 88 kHz	> 37 dB



(1) Optional.

(2) Chip inductor BLM32A07.

Fig.5 Application diagram.