ML9477

1/3 or 1/4 Duty, 32-Output LCD Driver

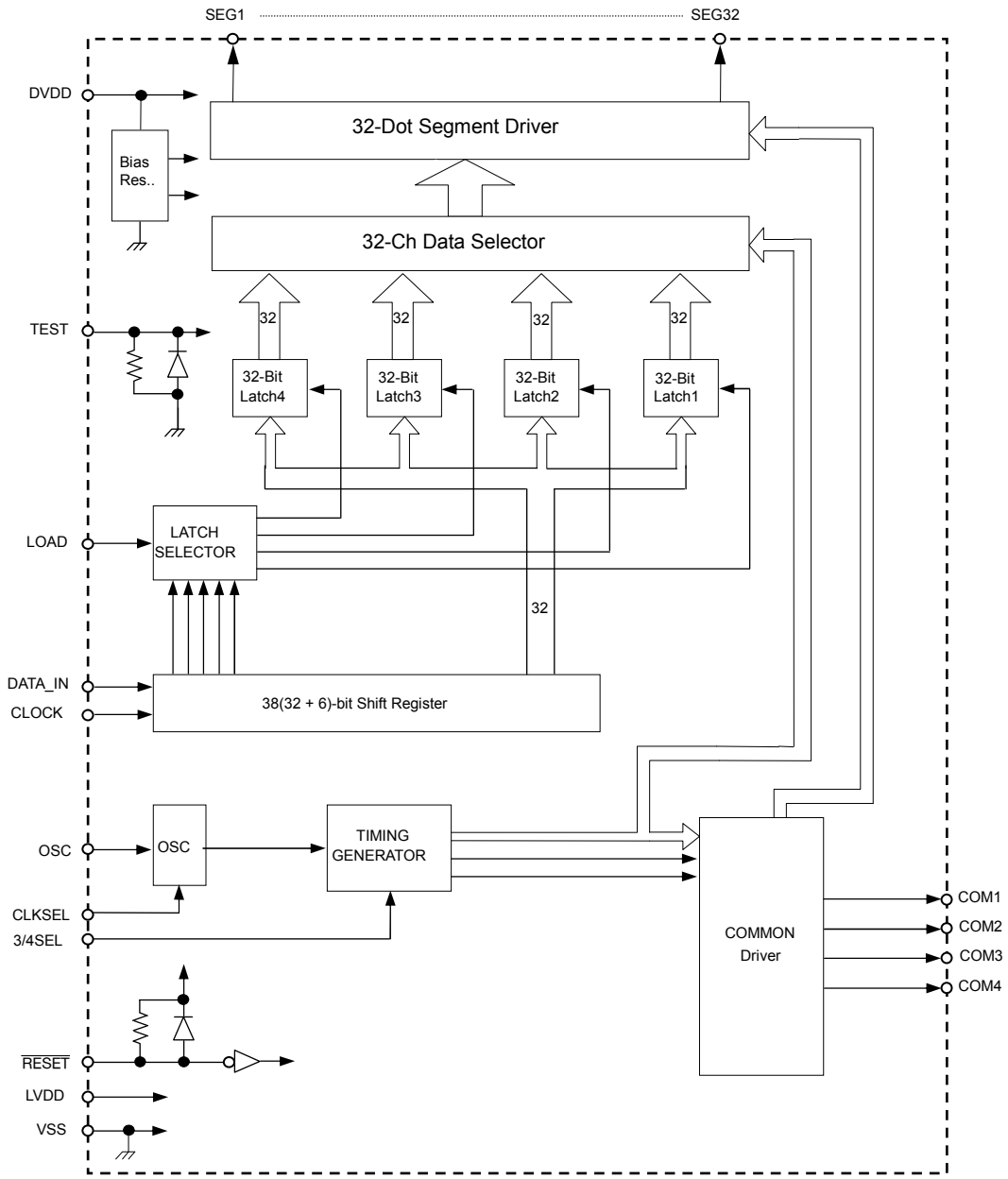
GENERAL DESCRIPTION

The ML9477 is an LCD driver for dynamic display. It has a function to switch between 1/3 and 1/4 duty. When 1/4 duty is selected, an LCD of up to 128 segments can be driven directly; when 1/3 duty is selected, an LCD of up to 96 segments can be driven directly.

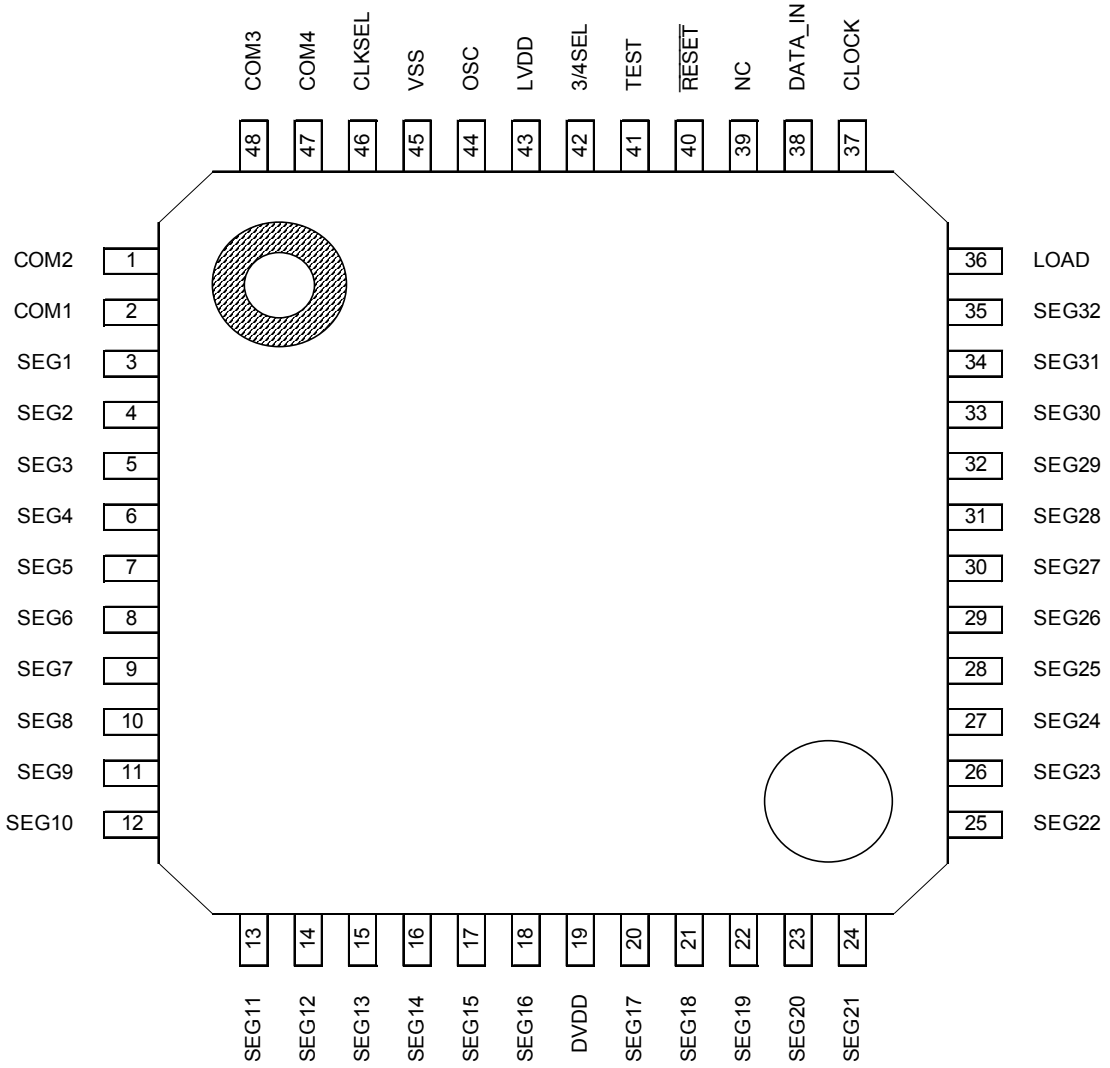
FEATURES

- Logic power supply voltage : 2.7 to 3.6 V, 4.5 to 5.5 V
- Driver power supply voltage : 3.5 to 5.5 V
- Operating temperature : –40 to +105°C
- 32 segment outputs
  1/4 duty : Up to 128 segments can be displayed.
  1/3 duty : Up to 96 segments can be displayed.
- Serially interfaces with the CPU using the three signal lines of LOAD, DATA_IN, and CLOCK
- Built-in RC oscillator circuit for LCD AC drive (the CLKSEL pin allows selecting an external clock input)
- Built-in voltage-dividing resistor for bias voltage generation
- Package : 48-pin plastic TQFP (TQFP48-P-0707-0.50-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

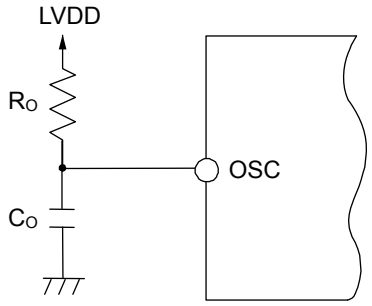


48-Pin Plastic TQFP

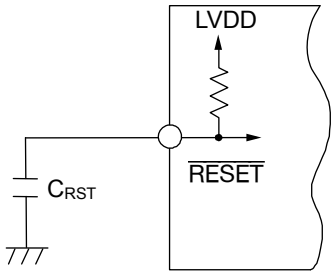
PIN DESCRIPTION

Symbol	I/O	Description
OSC	I/O	Pin for oscillation. Has a Schmitt circuit built in. An oscillator circuit can be configured by connecting one external resistor and one external capacitor. Since an oscillator circuit is susceptible to external noise, make the wiring between this pin and external components as short as possible. An external clock input can be selected by CLKSEL. The relationship between oscillation frequency f_{OSC} and frame frequency f_{FRM} is: $f_{FRM} = f_{OSC}/24$ (*1)
DATA_IN	I	Serial data input pin. Has a Schmitt circuit built in. The LCD display is turned on when the input data signal is at a "H" level and turned off when the input data signal is at a "L" level.
CLOCK	I	Shift clock input pin. Has a Schmitt circuit built in. Data to the DATA_IN pin is shifted in sync with the rising edges of the shift clock pulses.
LOAD	I	Load pulse input pin. Has a Schmitt circuit built in. Used to transfer serially input data to the display latch or write commands.
TEST	I	IC test pin. Has a pull-down resistor built in. Leave this pin open or connect it to VSS when not used.
CLKSEL	I	OSC pin input switching pin. When using the built-in oscillator circuit, set this pin to a "L" level; when inputting an external clock, set this pin to a "H" level. While this pin is at a "H" level, the oscillator circuit connected is disabled.
3/4SEL	I	1/3- or 1/4-duty switching input pin. When "H" level is input, 1/3 duty is selected and when "L" level is input, 1/4 duty is selected.
$\overline{\text{RESET}}$	I	Reset signal input pin for initializing the IC. Has a Schmitt circuit built in. This pin is enabled by setting it to "L" level. This pin has a built-in pull-up resistor. Normally, this pin, when connected with an external capacitor, performs power-on reset. (*2)
COM1 COM2 COM3 COM4	O	Output pins for LCD display. Connect to the common pins of the LCD panel. - When 1/3 duty is selected: Common signals are outputted through the COM1, COM2, and COM3 pins. Leave the COM4 pin open. - When 1/4 duty is selected: Common signals are outputted through the COM1, COM2, COM3, and COM4 pins.
SEG1 to SEG32	O	Output pins for LCD display. Connect to the segment pins of the LCD panel. For the relationship between each output of these pins and data, see the section on "Data Structure."
LVDD	–	Logic power supply pin.
DVDD	–	LCD driver power supply pin.
VSS	–	Ground pin.

*1: Oscillator circuit configuration



*2: Reset circuit configuration



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	LVDD, DVDD	Ta = 25°C	–0.3 to +6.5	V
Input voltage	V_I	Ta = 25°C	–0.3 to LVDD+0.3	V
Power dissipation	P_D	Ta ≤ 105°C	350	mW
Output current	I_O	Ta = 25°C	–2.0 to +2.0	mA
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic power supply voltage	LVDD	VSS= 0 V	2.7 to 3.6, 4.5 to 5.5	V
LCD drive voltage	DVDD	VSS= 0 V	3.5 to 5.5	V
CLOCK frequency	fcp	—	0.01 to 2	MHz
Operating temperature	T_a	—	–40 to +105	°C

Recommended setting range for external parts (for oscillator circuit)

(LVDD = 4.5 to 5.5 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillator resistor	R_O	—	20	82	kΩ
Oscillator capacitor	C_O	—	0.01	0.047	μF
Frame frequency	f_{FRM}	—	14.6	451.0	Hz

The relationship between external oscillator resistor value, external oscillator capacitor value, and frame frequency is as follows:

fFRM = f_{OSC} / 24

f_{OSC} = 1 / (device coefficient × external oscillator resistor value R_O × external oscillator capacitor value C_O)

Device coefficient = 0.6±23%

(LVDD = 2.7 to 3.6 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillator resistor	R_O	—	20	82	kΩ
Oscillator capacitor	C_O	—	0.01	0.047	μF
Frame frequency	f_{FRM}	—	14.6	451.0	Hz

The relationship between external oscillator resistor value, external oscillator capacitor value, and frame frequency is as follows:

fFRM = f_{OSC} / 24

f_{OSC} = 1 / (device coefficient × external oscillator resistor value R_O × external oscillator capacitor value C_O)

Device coefficient = 0.6±23%

ELECTRICAL CHARACTERISTICS

DC Characteristics

(LVDD = 2.7 to 3.6 V, 4.5 to 5.5 V, DVDD = 3.5 to 5.5, Ta = –40 to +105°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Applicable pin
"H" input voltage	V_{IH}	LVDD = 4.5 to 5.5V	0.8LVDD	LVDD	V	*1
		LVDD = 2.7 to 3.6V	0.85LVDD			
	V_{IHOSC}	LVDD = 4.5 to 5.5V CLKSEL = "H"	0.8LVDD			OSC
		LVDD = 2.7 to 3.6V CLKSEL = "H"	0.85LVDD			
"L" input voltage	V_{IL}	LVDD = 4.5 to 5.5V	0	0.2LVDD	V	*1
		LVDD = 2.7 to 3.6V		0.15LVDD		
	V_{ILOSC}	LVDD = 4.5 to 5.5V CLKSEL = "H"		0.2LVDD		OSC
		LVDD = 2.7 to 3.6V CLKSEL = "H"		0.15LVDD		
"H" input current	I_{IH1}	V_I = LVDD	—	1	μA	*2
	I_{IHOSC}	V_I = LVDD CLKSEL = "H"	—	1	μA	OSC
"L" input current	I_{IL1}	V_I = 0V	–1	—	μA	*2
	I_{IL2}	LVDD = 5V V_I = 0V	–0.009	–0.045	mA	$\overline{\text{RESET}}$
		LVDD = 3V V_I = 0V	–0.004	–0.030	mA	
	I_{ILOSC}	V_I = 0V CLKSEL = "H"	–1	—	μA	OSC
Segment output voltage	V_{OS0}	DVDD = 4.5V I_O = –10μA	DVDD – 0.8	—	V	SEG1 to SEG32
	V_{OS1}	DVDD = 4.5V I_O = ±10μA	2/3DVDD – 0.8	2/3DVDD + 0.8	V	
	V_{OS2}	DVDD = 4.5V I_O = ±10μA	1/3DVDD – 0.8	1/3DVDD + 0.8	V	
	V_{OS3}	DVDD = 4.5V I_O = 10μA	—	0.8	V	
Common output voltage	V_{OC0}	DVDD = 4.5V I_O = –10μA	DVDD – 0.77	—	V	COM1 to COM4
	V_{OC1}	DVDD = 4.5V I_O = ±10μA	2/3DVDD – 0.77	2/3DVDD+0.77	V	
	V_{OC2}	DVDD = 4.5V I_O = ±10μA	1/3DVDD – 0.77	1/3DVDD+0.77	V	
	V_{OC3}	DVDD = 4.5V I_O = 10μA	—	0.77	V	
Dynamic supply current	$I_{DVDD+I_{LVDD}}$	*3	—	0.5	mA	LVDD, DVDD

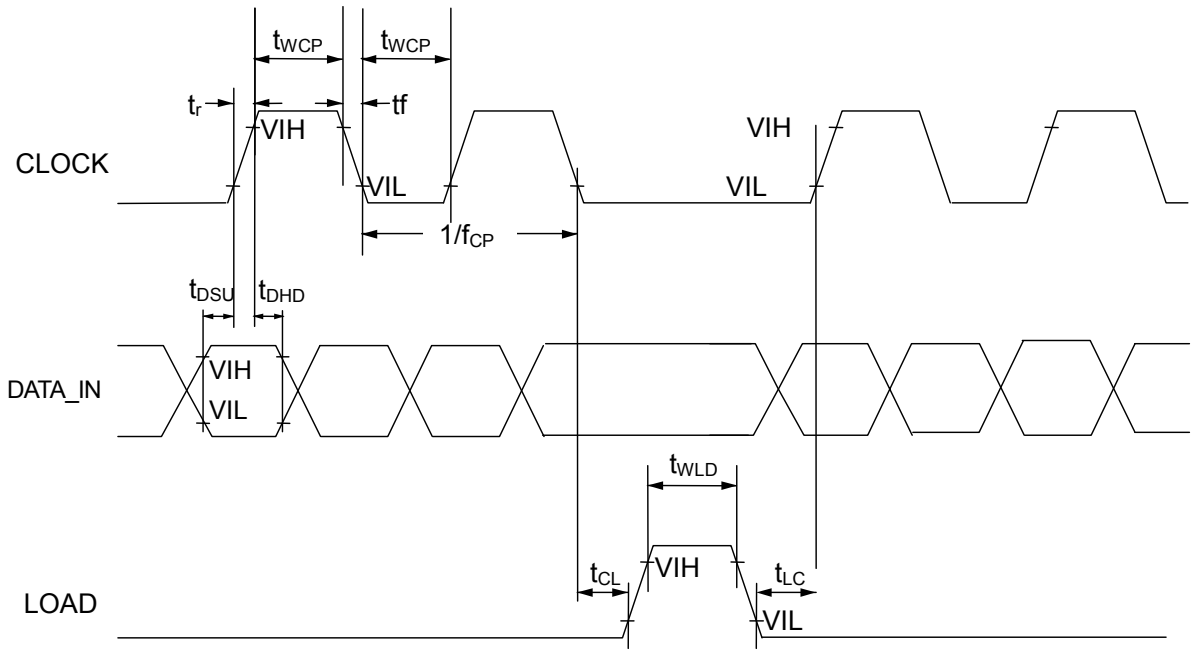
*1 CLOCK, LOAD, DATA_IN, $\overline{\text{RESET}}$, 3/4SEL, and CLKSEL
*2 CLOCK, LOAD, DATA_IN, 3/4SEL, and CLKSEL
*3 C_O = 0.022 μF, R_O = 33 kΩ, no load

Switching Characteristics (Serial Interface)

(LVDD = 2.7 to 3.6 V, 4.5 to 5.5 V, DVDD = 3.5 to 5.5 V, Ta = –40 to +105°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	f_{CP}	—	0.01	2.0	MHz
Clock pulse width	t_{WCP}	—	70	—	ns
Rise time, Fall time *4	t_r, t_f	—	—	3	μs
Data setup time	t_{DSU}	—	50	—	ns
Data hold time	t_{DHD}	—	50	—	ns
Load pulse width	t_{WLD}	—	100	—	ns
Clock to load time	t_{CL}	—	100	—	ns
Load to clock time	t_{LC}	—	100	—	ns

*4 Applied to CLOCK pin

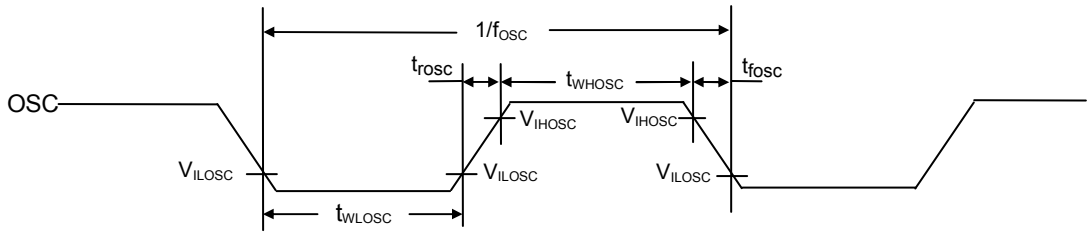


Switching Characteristics (External Clock Input to OSC)

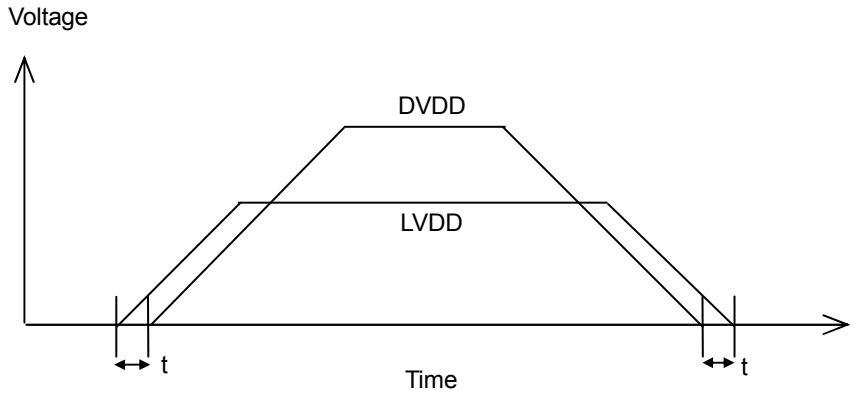
(LVDD = 2.7 to 3.6 V, 4.5 to 5.5 V, DVDD = 3.5 to 5.5 V, Ta = –40 to +105°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
OSC input frequency	f_{osc}	CLKSEL = ”H”	0.5	10	kHz
OSC rise time, fall time *5	t_{rosc}, t_{fOSC}	CLKSEL = ”H”	—	1	μs
OSC “H” period	t_{WHOSC}	CLKSEL = ”H”	4	—	μs
OSC “L” period	t_{WLOSC}	CLKSEL = ”H”	4	—	μs

*5 Applied to OSC pin

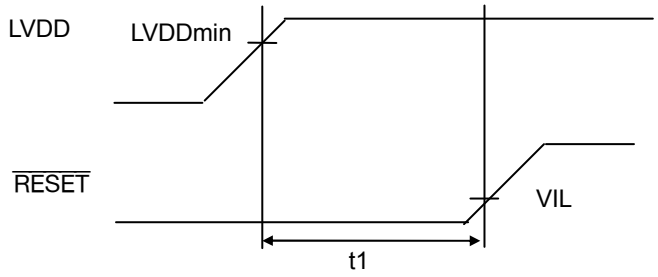


POWER-ON/OFF TIMING



If LVDD is in the range of 0 V to LVDDmin, make sure that LVDD ≥ DVDD and t ≥ 0[ns] are satisfied.
When performing power-on reset with a capacitor connected to the $\overline{\text{RESET}}$ pin, be careful about the relationship between the capacitance value and the rise time of the power supply.

INITIALIZATION TIMING



Drive the $\overline{\text{RESET}}$ pin Low and hold it Low under the condition "t1 ≥ 0[ns]" until LVDD reaches LVDDmin.

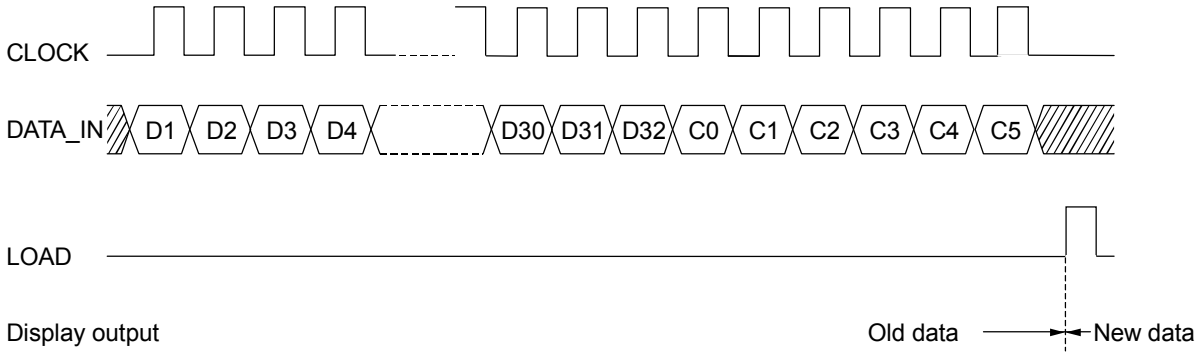
The value of the current of the pull-up resistor is specified for $\overline{\text{RESET}}$ pin.
The customer needs to select an external capacitor that meets the timing requirements shown above.

FUNCTIONAL DESCRIPTION

Description of Operation

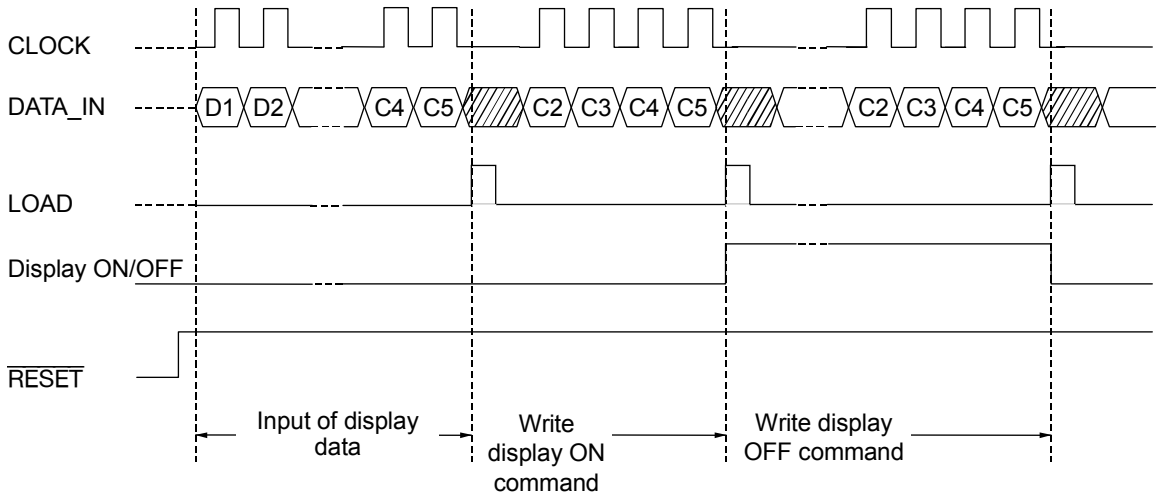
- Display data input

As described in the section on “Data Structure,” display data consists of a data field, which corresponds to the LCD segments ON and OFF, and a command field, which indicates the input of display data.
Set a value in each of bits C0 and C1 in the command field according to the common output that corresponds to the display data, and set a display data input command in the remaining four bits.
Data that has been input to the DATA_IN pin is loaded into the shift register on the rising edges of the CLOCK pulses, transferrred to the display data latch during the “H” level period of the LOAD pulse, and then output via the segment driver.



- Display ON, display OFF

Display goes off when power-on reset is executed; therefore, to turn display on, write the display ON command (F5).
The display OFF command (F4) is a command that makes all segments go off. By writing the display OFF command, the segments go off irrespective of display data.
The display ON command (F5) is a command that clears a display off state. By writing the display ON command, display goes back to the previous state.



List of Commands

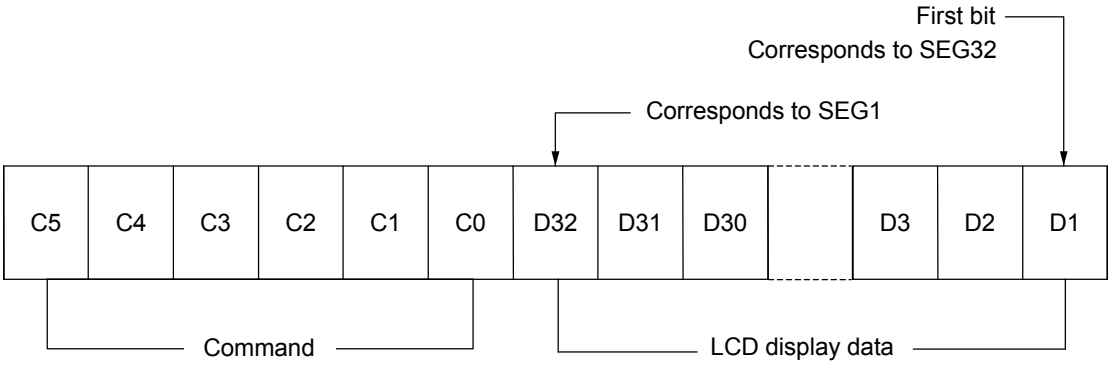
Command name	C5	C4	C3	C2	C1	C0	Description
F0	0	0	0	0	×	×	Disabled
F0’	0	0	0	1	×	×	Disabled
F1	0	0	1	0	0	0	Display data input (corresponds to COM1)
						1	Display data input (corresponds to COM2)
					1	0	Display data input (corresponds to COM3)
						1	Display data input (corresponds to COM4)
F2	0	1	0	×	×	×	Disabled
F3	0	1	1	0	0	0	Disabled
						1	Disabled
					1	0	Disabled
						1	Disabled
F3’	0	1	1	1	×	×	Disabled
F4	1	0	1	0	×	×	Display OFF
F5	1	0	1	1	×	×	Display ON
F6	1	1	0	×	×	×	Disabled
F7	1	0	0	×	×	×	Disabled
F8	1	1	1	×	×	×	Disabled

×: Don't care

If a “Disabled” command is executed, no transfer is carried out from the shift register to the latch; however, data within the shift register will be rewritten. To transfer correct data to the latch, it is necessary to transfer data again using the F1 command.

Data Structure

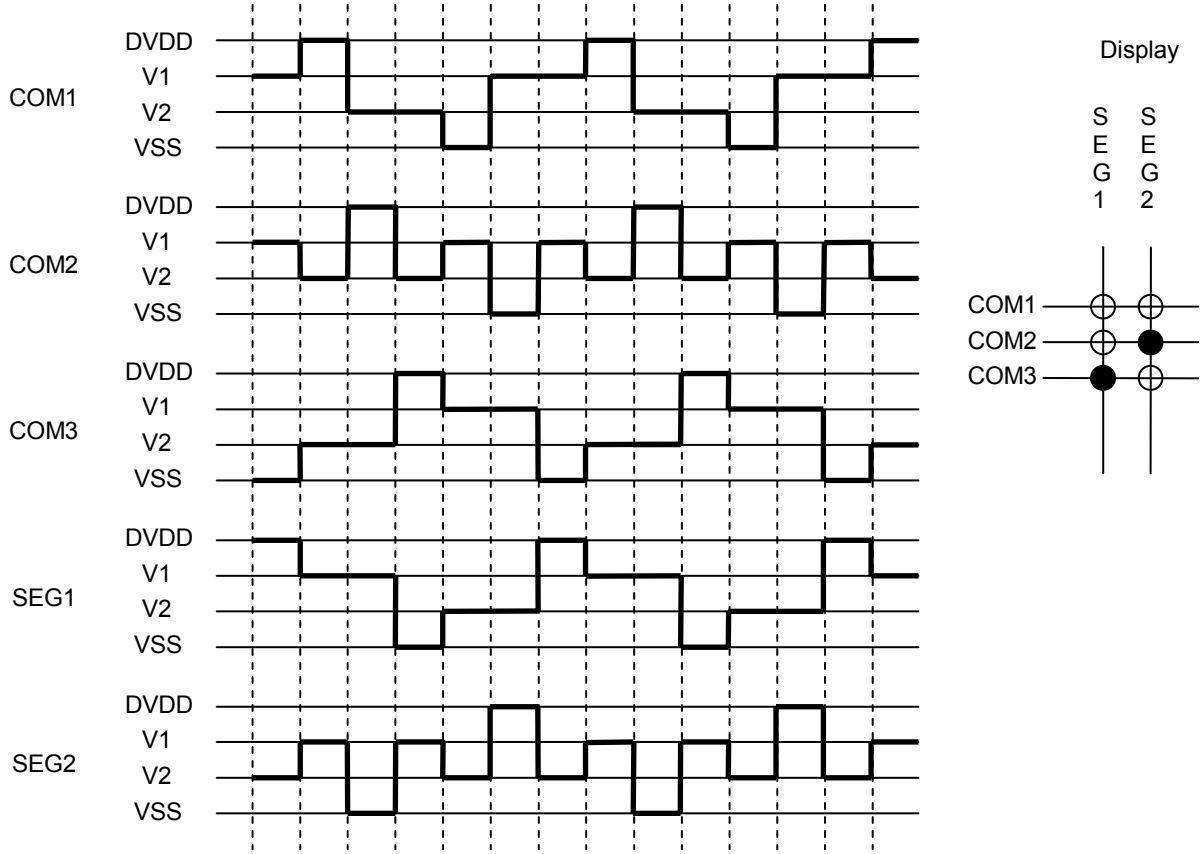
[Input data]



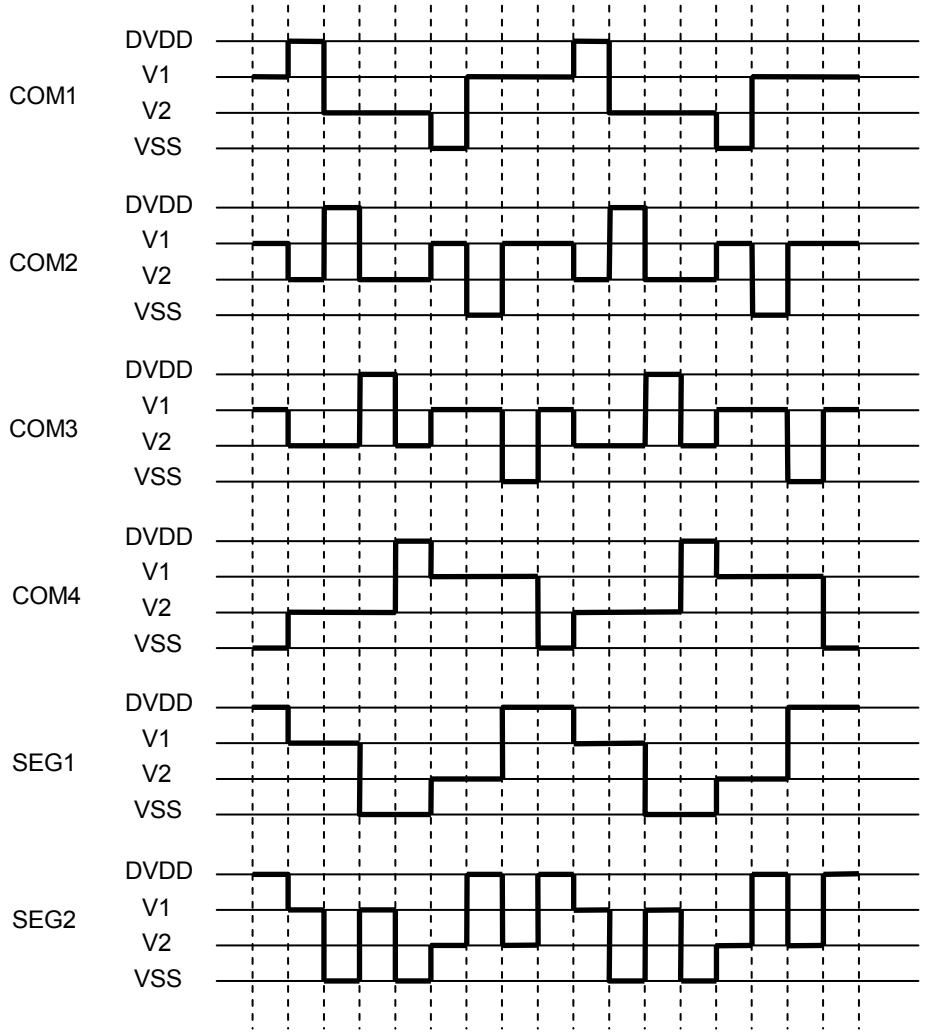
Note 1: The setting of command F4 or F5 becomes enabled by inputting only the four bits of C2 to C5. (No need to input D1 to D32, C0, or C1.)
Note 2: If any dummy bits are required because of the transfer bit count, add them before the first bit.
Note 3: Command execution depends on the value of bits C5 to C0 stored immediately before LOAD goes to a "H" level.

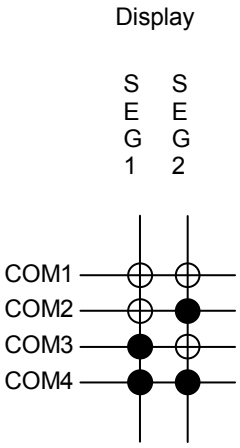
Common and Segment Output Waveforms

・1/3 duty

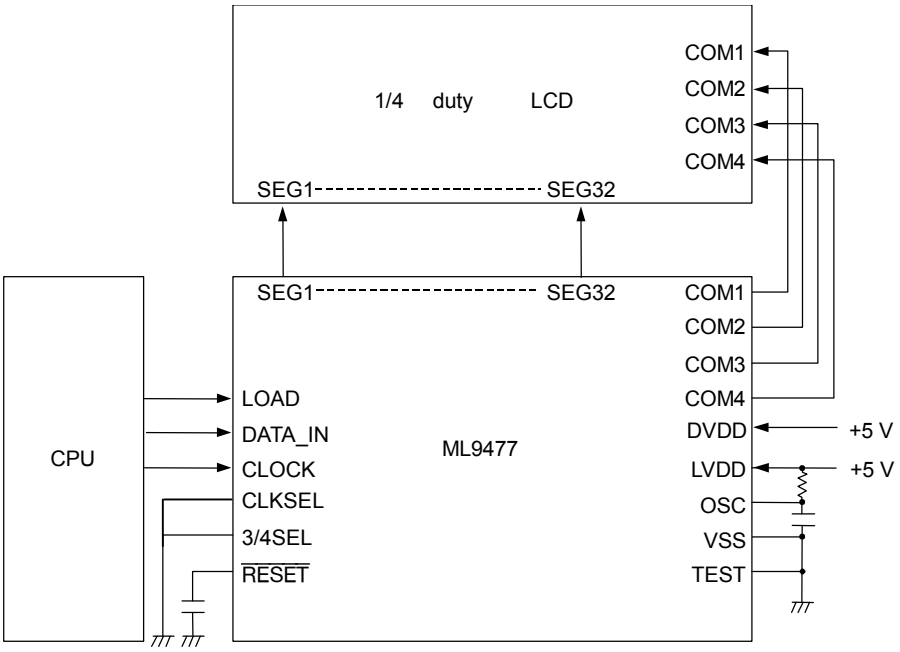


• 1/4 duty


COM1
DVDD
V1
V2
VSS
COM2
DVDD
V1
V2
VSS
COM3
DVDD
V1
V2
VSS
COM4
DVDD
V1
V2
VSS
SEG1
DVDD
V1
V2
VSS
SEG2
DVDD
V1
V2
VSS


Display
SEG1
SEG2
COM1
COM2
COM3
COM4

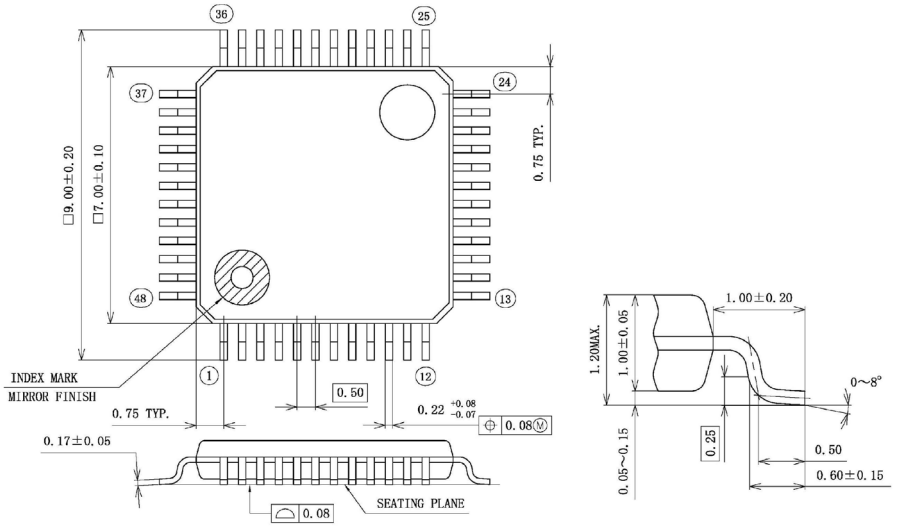
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit: mm)

TQFP48-P-0707-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.13 TYP.
Rev. No./Last Revised	1/Oct. 22, 2007

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9477-01	Mar. 1, 2010	–	–	Final edition 1

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