PIC24FJ256GB110 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GB110 family devices that you have received conform functionally to the current Device Data Sheet (DS39897**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GB110 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet Clarifications and corrections start on page 14, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or to the PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB IDE hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GB110 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3	A5	A6			A3	A5	A6
PIC24FJ256GB110	101Fh	01h	03h	04h	PIC24FJ128GB108	100Bh	01h	03h	04h
PIC24FJ192GB110	1017h				PIC24FJ64GB108	1003h			
PIC24FJ128GB110	100Fh				PIC24FJ256GB106	1019h			
PIC24FJ64GB110	1007h				PIC24FJ192GB106	1011h			
PIC24FJ256GB108	101Bh				PIC24FJ128GB106	1009h			
PIC24FJ192GB108	1013h				PIC24FJ64GB106	1001h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXGA0XX Flash Programming Specification"* (DS39768) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A3	A5	A6
Core	RAM Operation	1.	Repeated register operations entering Doze mode.	X	X	X
Core	BOR	2.	Spontaneous BOR with analog or USB peripherals.	X		
JTAG	Device Programming	3.	Programming lockout during JTAG programming.	X	X	X
UART	—	4.	Framing issues when using two Stop bits.	X		
I/O	PORTB	5.	RB5 remains in high-impedance in Open-Drain mode.	X		
SPI	Master mode	6.	SPIxIF and SPIRBF may be set early in some instances.	X		
CTMU	—	7.	Trigger to IC or OC modules may not work.	X		
USB	—	8.	Issue with Host mode, low-speed operation.	X	X	X
USB	VUSB Regulator	9.	Does not regulate to 3.3V.	X	X	X
USB	—	10.	CRC errors while using external transceiver.	X	X	X
USB	—	11.	ACTIVIF flag functions only during Sleep.	X	X	X
UART	UERIF Interrupt	12.	Interrupt may not function with multiple errors.	X		
UART	FIFO Error	13.	PERR and FERR flags may be incorrect in certain cases.	X		
UART	IrDA®	14.	Payload error in 8-bit mode.	X		
UART	IrDA	15.	Framing error in 9-bit mode.	X		
UART	IrDA	16.	Payload errors in 8-bit mode.	X		
I2C™ Module	Master mode	17.	Master module may Acknowledge its own transmission as a slave.	X		
I2C Module	Slave mode	18.	Module may not respond correctly to reserved addresses.	X		
Memory	PSV	19.	False address error traps.	X		
ICSP™	—	20.	PGEC3/PGED3 not functional.	X		
Core	Instruction Set	21.	Issue with Read-After-Write stalls in `REPEAT` loops.	X	X	X
RTCC	—	22.	Unexpected decrements of Alarm Repeat Counter.	X		
SPI	Enhanced Buffer mode	23.	Issue with early full buffer interrupt.	X		
A/D	—	24.	Disabled voltage references during Debug mode (64-pin devices only).	X		
SPI	Enhanced Buffer mode	25.	Issue with SRMPT bit becoming set early in certain cases.	X		
Core	Code-Protect	26.	GCP disables write access to interrupt vectors.	X		
CTMU	A/D Trigger	27.	Automatic conversion may not function.	X		
Oscillator	LPRC	28.	Failure to restart following BOR events.	X		
Oscillator	Two-Speed Start-up	29.	Feature is not functional.	X	X	X
Output Compare	—	30.	Single missed compare events under certain conditions.	X		
Interrupts	INTx	31.	External interrupts missed when writing to INTCON2.	X	X	X
A/D Converter	—	32.	Module continues to draw current when disabled.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A5	A6
Oscillator	—	33.	POSCEN bit does not work with Primary + PLL modes.	X	X	X
Output Compare	Interrupt	34.	Interrupt flag may precede the output pin change under certain circumstances.	X	X	X
CTMU	—	35.	Disabling module affects band gap.	X	X	X
UART	Transmit	36.	A TX interrupt may occur before the data transmission is complete.	X	X	X
USB	Device Mode	37.	EPSTALL bit behavior differs from previous documentation.	X	X	X
USB	Device and Host Modes	38.	ACTVIF wake-up behavior differs from previous documentation.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Core (RAM Operation)

If a RAM read is performed on the instruction immediately prior to enabling Doze mode, an extra read event may occur when Doze mode is enabled. This has no effect on most SFRs and on user RAM space. However, this could cause registers which also perform some action on a read (such as auto-incrementing a pointer or removing data from a FIFO buffer) to repeat that action, possibly resulting in lost data or unexpected operation.

Work around

Avoid reading registers which perform a secondary action (e.g., UARTx and SPIx's FIFO buffers, and the RTCVAL registers) immediately prior to entering Doze mode.

If this cannot be avoided, execute a NOP instruction before entering Doze mode.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

2. Module: Core (BOR)

When the on-chip regulator is enabled (ENVREG tied to VDD), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and either:
- the internal band gap reference is being used as a reference with the A/D Converter (AD1PCFG2<1> or <0> = 1) or comparators (CMxCON<1:0> = 11); or
- the CTMU or the USB module is enabled.

Work around

Limit the following activities to only those times when the on-chip regulator is not in Tracking mode (LVDIF (IFS4<8>) = 0):

- Enabling the USB or CTMU modules
- Selecting the internal band gap as a reference for the A/D Converter or the comparators

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

3. Module: JTAG (Device Programming)

The JTAGEN Configuration bit can be programmed to '0' while using the JTAG interface for device programming. This may cause a situation where JTAG programming can lock itself out of being able to program the device.

Work around

None.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

4 Module: UART

When the UARTx is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Affected Silicon Revisions

A3	A5	A6					
X							

5. Module: I/O (PORTB)

When RB5 is configured as an open-drain output, it remains in a high-impedance state. The settings of LATB5 and TRISB5 have no effect on the pin's state.

Work around

If open-drain operation is not required, configure RB5 as a regular I/O (ODCB<5> = 0).

If open-drain operation is required, there are two options:

- Select a different I/O pin for the open-drain function
- Place an external transistor on the pin and configure the pin as a regular I/O

Affected Silicon Revisions

A3	A5	A6					
X							

6. Module: SPI (Master Mode)

In Master mode, both the SPIx Interrupt Flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0)
- The module is configured for serial data output changes on transition from clock active to clock Idle state (CKE = 1)

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPIx buffer, check the SCKx pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this. In this example, pin, RD1, functions as the SPIx clock, SCKx, which is configured as Idle low.

Affected Silicon Revisions

A3	A5	A6					
X							

7. Module: CTMU

When the CTMU module is selected as the trigger source (SYNCSEL<4:0> = 11000), the output compare or input capture module triggers may not work.

Work around

Manually trigger the output compare and/or input capture modules after a CTMU event is received. Be certain to compensate for any time latency required by manually triggering the module.

Affected Silicon Revisions

A3	A5	A6					
X							

8. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the PRE signal may not be generated correctly. This will result in not being able to communicate correctly with the low-speed device.

Work around

Connect low-speed devices directly to the application and not through a USB hub.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

9. Module: USB (VUSB Regulator)

The USB internal voltage regulator does not regulate to 3.3V. The USB internal voltage regulator is an optional feature and is not required for USB operation or compliance.

Work around

Disable the USB voltage regulator (DISUVREG Configuration bit set to '1') and supply 3.0V to 3.6V from an external source to the VUSB pin.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

10. Module: USB

When the module is configured to use an external transceiver, the CRC5 value of some packets may be incorrect.

Work around

Use the module's internal transceiver.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPIx CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

11. Module: USB

The Bus Activity Interrupt Flag, ACTVIF, is active only while the device is in Sleep mode. It will not become set when the microcontroller is in a Run mode.

Work around

The type of work around depends on the type of application that the microcontroller is being used for.

For Self-Powered Peripherals: After receiving a Suspend command from the PC, do NOT suspend or disable the USB module. In addition, do not switch to a clock configuration that is incompatible with USB operation (refer to the device data sheet for USB compatible clock settings).

For Bus Powered Peripherals: After receiving a suspend command from the PC (IDLEIF Interrupt Flag = 1):

- Suspend the USB module (U1PWRC<1> = 1)
- Globally enable USB interrupts (IEC5<6> = 1)
- Specifically enable the bus activity interrupt (U1OTGIE<4> = 1)
- Place the microcontroller into Sleep mode as soon as possible

For Embedded Host Devices:

- Issue a suspend command to the peripheral device
- Suspend the USB module (U1PWRC<1> = 1)
- Globally enable USB interrupts (IEC5<6> = 1)
- Place the microcontroller into Sleep mode as soon as possible

As an alternate procedure, do NOT suspend or disable the USB module and do not switch to a clock configuration that is incompatible with USB operation.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

12. Module: UART (UERIF Interrupt)

The UARTx error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UARTx error interrupt fails to occur. For possible exceptions, refer to Errata # 13.

Affected Silicon Revisions

A3	A5	A6					
X							

13. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- The UARTx receive interrupt is set to occur when the FIFO is full or ¾ full (UxSTA<7:6> = 1x)
- More than 2 bytes with an error are received

In these cases, only the first two bytes with a parity or framing error will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Affected Silicon Revisions

A3	A5	A6					
X							

14. Module: UART (IrDA®)

When the UARTx is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA endec (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A3	A5	A6					
X							

15. Module: UART (IrDA)

When the UARTx is operating in 8-bit mode (PDSEL<1:0> = 0x) and using the IrDA endec (IREN = 1), a framing error may occur when transmitting a data payload of 00h.

Work around:

None.

Affected Silicon Revisions

A3	A5	A6					
X							

16. Module: UART (IrDA)

When the UARTx is operating in 9-bit mode (PDSEL<1:0> = 1x) and using the IrDA endec (IREN = 1), the module will incorrectly transmit 10 bits when transmitting data payloads of 00h or 80h.

Work around:

None.

Affected Silicon Revisions

A3	A5	A6					
X							

17. Module: I²C™ Module (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1)
- The I²C Master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module

In these cases, the Master also Acknowledges the address command and generates an erroneous I²C slave interrupt, as well as the I²C master interrupt.

Work around

Several options are available:

- When using 10-Bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSbs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = 0) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I²C interrupt occurs on the master module.

Affected Silicon Revisions

A3	A5	A6					
X							

18. Module: I²C Module (Slave Mode)

Under certain circumstances, a module operating in Slave mode, may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1)
- Bits, A<7:1>, of the slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges: '1111xxx' or '0000xxx'.

In these cases, the Slave module Acknowledges the command and triggers an I²C slave interrupt; it does *not* copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A<7:1>, of the module's slave address equal to '1111xxx' or '0000xxx'.

Affected Silicon Revisions

A3	A5	A6					
X							

19. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit `MOV` instruction is used to read the data at location, 8000h.

Work around

Do not use the first location of the PSV page (address 8000h). The MPLAB C Compiler (v3.11 or later) supports the option, "`-merrata=psv_trap`", to prevent it from generating code that would cause this erratum.

Affected Silicon Revisions

A3	A5	A6					
X							

20. Module: ICSP™

The ICSP/ICD port pair, PGEC3/PGED3 (RB5/RB4), cannot be used to read or program the device.

Work around

Use either PGEC2/PGED2 or PGEC1/PGED1.

Affected Silicon Revisions

A3	A5	A6					
X							

21. Module: Core (Instruction Set)

If an instruction producing a Read-After-Write stall condition is executed inside a `REPEAT` loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 15 times.

Work around

Avoid using `REPEAT` to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches. The MPLAB C Compiler will not generate `REPEAT` loops that cause this erratum.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

22. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR, and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Affected Silicon Revisions

A3	A5	A6					
X							

23. Module: SPI (Enhanced Buffer Modes)

If the SPIx event interrupt is configured to occur when the enhanced FIFO buffer is full (SISEL<2:0> = 111), the interrupt may actually occur when the 7th byte is written to the buffer, instead of the 8th byte. The other enhanced buffer interrupts function as previously described.

Work around

Do not use the Full Buffer Interrupt mode. The SPITBF bit (SPIxSTAT<1>) reliably indicates when the enhanced FIFO buffer is full and can be polled instead of using the Full Buffer Interrupt mode.

Affected Silicon Revisions

A3	A5	A6					
X							

24. Module: A/D Converter

When using PGEC1 and PGED1 to debug an application on any 64-pin devices in this family, all voltage references will be disabled. This includes VREF+, VREF-, AVDD and AVSS. Any A/D conversion will always equal 0x3FF.

Note: This issue only applies to 64-pin devices in this family (PIC24FJ256GB106, PIC24FJ192GB106, and PIC24FJ64GB106).

Work around

Use PGEC2 and PGED2 to debug any A/D functionality.

Affected Silicon Revisions

A3	A5	A6					
X							

25. Module: SPI (Enhanced Buffer Mode)

In Enhanced Master mode, the SRMPT bit (SPIxSTAT<7>) may erroneously become set for several clock cycles in the middle of a FIFO transfer, indicating that the shift register is empty when it is not. This happens when both SPIx clock prescalers are set to values other than their maximum (SPIxCON<4:2> ≠ 000 and SPIxCON<1:0> ≠ 00).

Work around

Set SISEL<2:0> (SPIxSTAT<4:2>) to '101'. This configures the module to generate an SPIx event interrupt whenever the last bit is shifted out of the shift register. When the SPIxIF flag becomes set, the shift register is empty.

Affected Silicon Revisions

A3	A5	A6					
X							

26. Module: Core (Code Protection)

When general segment code protection has been enabled (GCP Configuration bit is programmed), applications are unable to write to the first 512 bytes of the program memory space (0000h through 0200h). In applications that may require the interrupt vectors to be changed during run time, such as bootloaders, modifications to the Interrupt Vector Tables (IVT) will not be possible.

Work around

Create two new Interrupt Vector Tables, one each for the IVT and AIVT, in an area of program space beyond the affected region. Map the addresses in the old vector tables to the new tables. These new tables can then be modified as needed to the actual addresses of the ISRs.

Affected Silicon Revisions

A3	A5	A6					
X							

27. Module: CTMU (A/D Trigger)

The CTMU may not trigger an automatic A/D conversion after the current source is turned off. This happens even when the A/D trigger control bit, CTTRIG (CTMUCON<8>), has been set.

Work around

Perform a manual A/D conversion by clearing the SAMP bit (AD1CON1<1>) immediately after the CTMU current source has been stopped.

Affected Silicon Revisions

A3	A5	A6					
X							

28. Module: Oscillator (LPRC)

The LPRC may not automatically restart following BOR events (i.e., when supply voltage sags to between the BOR and POR thresholds, then returns to above the BOR level). When this happens, systems that use the LPRC clock may not work. This includes the PLL, Two-Speed Start-up, Fail-Safe Clock Monitor and the WDT.

Work around

For PLL issues: select a non-PLL Clock mode as the initial start-up mode, using the FNOSC Configuration bits (CW2<10:8>). After the application has initialized, switch to a PLL Clock mode in software using the NOSC bits (OSCCON<10:8>). Allow 10 μs to elapse between application start-up and a software clock switch.

For WDT issues: disable the WDT by programming the FWDTEN bit (CW1<7>). After the application has initialized, enable the WDT in software by setting the SWDTEN bit (RCON<5>). Allow 10 μs to elapse between application start-up and setting SWDTEN.

Affected Silicon Revisions

A3	A5	A6					
X							

29. Module: Oscillator (Two-Speed Start-up)

Two-Speed Start-up is not functional. Leaving the IESO Configuration bit in its default state (Two-Speed Start-up enabled) may result in unpredictable operation.

Work around

None. Always program the IESO Configuration bit to disable the feature (CW2<15> = 0).

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

30. Module: Output Compare

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0000h (0% duty cycle) and the OCxRS register is updated with a value of 0001h. The compare event is only missed the first time a value of 0001h is written to OCxRS and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0000h, avoid writing a value of 0001h to OCxRS. Instead, write a value of 0002h. In this case, however, the duty cycle will be slightly different from the desired value.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

31. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT4) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses, 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC5 are not being used in the application, the code sequence would be:

```
IEC5 = 0x1E;
INTCON2 = 0x1E;
IEC5 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

32. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current, even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD register also disables the AD1PCFG registers, which in turn affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

33. Module: Oscillator

The POSCEN bit (OSCCON<2>) has no effect when a Primary Oscillator with PLL mode is selected (COSC<2:0> = 011). If XTPLL, HSPLL or ECPLL Oscillator mode are selected, and the device enters Sleep mode, the Primary Oscillator will be disabled, regardless of the state of the POSCEN bit.

XT, HS and EC Oscillator modes (without the PLL) will continue to operate as expected.

Work around

None.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

34. Module: Output Compare (Interrupt)

Under certain circumstances, an Output Compare match may cause the interrupt flag (OCxIF) to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- the module is in One-Shot mode (OCM<2:0> = 001, 010 or 100);
- one of the timer modules is being used as the time base; and
- a timer prescaler other than 1:1 is selected.

If the module is re-initialized by clearing OCM<2:0> after the One-Shot compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing OCM<2:0>. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

35. Module: CTMU

Using the CTMUMD bit (PMD4<2>) to selectively power down the module may reduce the accuracy of the internal band gap reference (V_{BG}). In those cases where V_{BG} is used as a reference for other analog modules, the accuracy of measurements or comparisons may be affected.

Work around

If the A/D Converter or Comparators are being used with V_{BG} selected as a reference, do not set the CTMUMD bit.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

36. Module: UART

When using UTXISEL<1:0> = 01 (interrupt when last character is shifted out of the Transmit Shift Register), and the final character is being shifted out through the Transmit Shift Register, the TX interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, after which, the following work around can be implemented:

Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register empty bit, as shown in Example 2.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

37. Module: USB (Device Mode)

In previous literature for this module, the EPSTALL bits (U1EPn<1>) are described as being only stall status indicator bits in Device mode. In actual implementation, the EPSTALL bits function as both status and control bits.

If the EPSTALL bit for endpoint 'n' is set (either by the SIE hardware or manually in firmware), both the IN and OUT endpoints, associated with the endpoint, will send STALL packets when the endpoint's UOWN bit (BDnSTAT<15>) is also set.

Work around

For Host Applications: No work around is needed as hosts do not send STALL packets.

For Device Mode Applications: When it is necessary to stop sending STALL packets on an endpoint, clear the endpoint's respective BSTALL (BDnSTAT<10>) and EPSTALL bits. If the application firmware was developed based on one of the examples in the Microchip USB framework, this is already the default behavior of the USB stack firmware (except Version 2.8); no further work around is normally needed.

If a Device mode application was based upon Version 2.8 of the USB framework, and the application uses STALL packets on any of the application endpoints (1-15), it is suggested to update the application to the latest version.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

EXAMPLE 2: DELAYING THE ISR BY POLLING THE TRMT BIT

```
// in UART2 initialization code
...
U2STAbits.UTXISEL0  = 1;          // Set to generate TX interrupt when all
U2STAbits.UTXISEL1  = 0;          // transmit operations are complete.
...

U2TXInterrupt(void)
{
    while(U2STAbits.TRMT==0);     // wait for the transmit buffer to be empty
    ...                           // process interrupt
```

38. Module: USB (Device and Host Modes)

In previous literature for this module, the ACTVIF interrupt flag (U1OTGIR<4>) is described as being asserted, based on state changes detected on D+, D- or VBUS, when the microcontroller is in Sleep mode. In actual implementation, state changes on the RF3/USBID pin also cause the ACTVIF flag to be asserted.

As a result, logic input level changes on RF3/USBID may cause ACTVIF to be asserted, even in non-OTG applications that do not use the USBID function. This may cause the microcontroller to wake up unexpectedly.

Work around

For On-The-Go (OTG) Based Applications: No work around is needed.

For non-OTG Device, Host or Dual-Role Applications: If ACTVIF is used as a wake-up source, it is recommended that the application be designed so that RF3/USBID does not see any changes while the microcontroller is in a power-saving mode.

If RF3/USBID is not needed in the application, it is recommended to configure it as a digital output.

If the RF3/USBID pin is configured as a digital input, ensure that the signal provider does not change the pin state while ACTVIF is enabled as a wake-up source. If the pin is used as a general purpose input, which can change while in the USB Suspend state, check the IDIF flag (U1OTGIR<7>) after waking up from an ACTVIF event to determine if the wake-up event was caused by a state change on RF3/USBID.

Affected Silicon Revisions

A3	A5	A6					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39897**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

Note:	This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to **Section 26.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

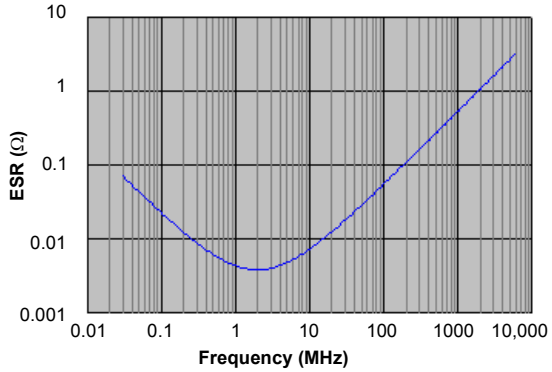
When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 29.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to +125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to +85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

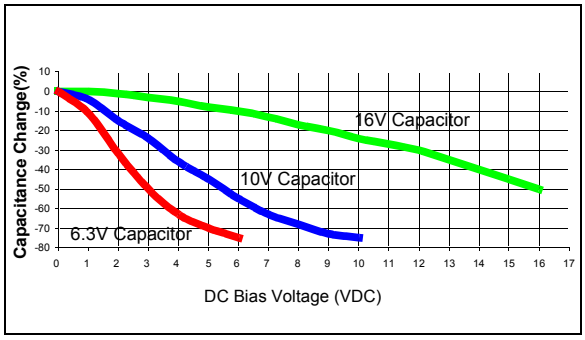
Typical low-cost 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2. Module: Electrical Specifications

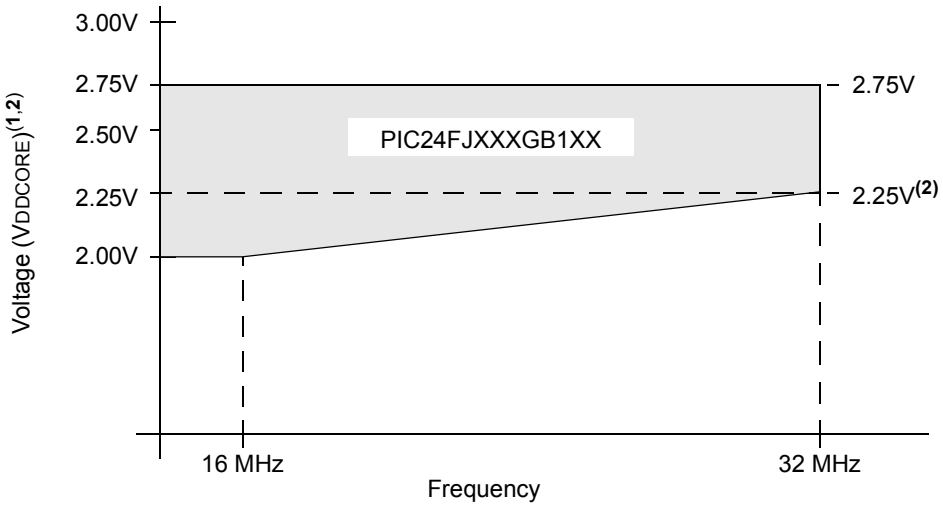
The “Absolute Maximum Ratings” listed on page 311 are amended by adding the following specification:

Voltage on V_{USB} with respect to V_{SS}..... (V_{DDCORE} – 0.3V) to 4.0V

3. Module: Electrical Specifications (DC Characteristics)

Figure 29-1 (“PIC24FJ256GB110 Family Voltage-Frequency Graph”) is amended by adding an additional footnote. The updated figure is shown below (changes in **bold**; bold in original removed for clarity).

FIGURE 29-1: PIC24FJ256GB110 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



For frequencies between 16 MHz and 32 MHz, F_{MAX} = (64 MHz/V) * (V_{DDCORE} – 2V) + 16 MHz.

Note 1: When the voltage regulator is disabled, V_{DD} and V_{DDCORE} must be maintained so that $V_{DDCORE} \leq V_{DD} \leq 3.6V$.

2: When the USB module is enabled, V_{USB} should be provided at 3.0V to 3.6V while V_{DDCORE} must be 2.35V. When the USB module is not enabled, the wider limits shaded in grey apply. The voltage on the V_{USB} pin should be maintained at (V_{DDCORE} – .3V) or greater. Optionally, the pin may be left in a high-impedance state when the USB module is not in use, but doing so may result in higher I_{PD} currents than specified.

4. Module: Electrical Specifications (DC Characteristics)

Table 29-3 ("DC Characteristics: Temperature and Voltage Specifications") is amended by adding a new specification, V_{USB}, and an explanatory footnote. The changes are shown below in **bold text** (bold text in original was removed for clarity).

5. Module: Electrical Specifications

In Table 29-3 ("DC Characteristics: Temperature and Voltage Specifications"), the Minimum and Maximum values for DC18 (BOR Voltage on V_{DD} Transition) are changed to 1.80V and 2.25V, respectively. The Typical value remains unchanged.

TABLE 29-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS (PARTIAL REPRESENTATION)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
Operating Voltage							
	V_{USB}	**USB Supply Voltage**	**3.0**	**3.3**	**3.6**	**V**	**USB module enabled(3)**

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which V_{DD} can be lowered without losing RAM data.

3: **V_{USB} should always be maintained at V_{DD} or greater when the USB module is enabled. The V_{USB} pin may be left in a high-impedance state when the USB module is disabled and pins, RG2 and RG3, will not be used as general purpose inputs, but doing so may result in higher I_{PD} currents than specified.**

6. Module: Electrical Specifications

Table 29-7 (I/O Pin Input Specifications) is amended by the addition of the following new specifications:

- DI31 (Maximum Load Current for Internal Pull-up)
- DI60 (Injection Currents)

The new specifications, and accompanying new footnotes, 5 through 9, are shown below (additions in **bold**; bold in existing text was removed for clarity).

TABLE 29-7: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (PARTIAL PRESENTATION)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ(1)	Max.	Units	Conditions
DI31	**IPU**	**Maximum Load Current for Digital High Detection with Internal Pull-up**	**—**	**—**	**30**	**µA**	**VDD = 2.0V**
			—	**—**	**100**	**µA**	**VDD = 3.3V**
DI60a	**IICL**	**Input Low Injection Current**	**0**	**—**	**-5(5,8)**	**mA**	**All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB and VBUS**
DI60b	**IICH**	**Input High Injection Current**	**0**	**—**	**+5(6,7,8)**	**mA**	**All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB and VBUS, and all 5V tolerant pins(7)**
DI60c	**∑IICT**	**Total Input Injection Current (sum of all I/O and control pins)**	**-20(9)**	**—**	**+20(9)**	**mA**	**Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT**

Note 1: (existing footnote)
2: (existing footnote)
3: (existing footnote)
4: (existing footnote)
5: Parameter characterized but not tested.
6: Non-5V tolerant pins: VIH source > (VDD + 0.3), 5V tolerant pins: VIH source > 5.5V. Characterized but not tested.
7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources greater than 5.5V.
8: Injection currents > \| 0 \| can affect the performance of all analog peripherals (e.g., A/D, comparators, internal band gap reference, etc.)
9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions is permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

7. Module: Electrical Specifications

Table 29-10 and Table 29-11 (shown below) are added to **Section 28 "Electrical Characteristics"**, following the existing Table 29-9 (Program Memory). All subsequent tables in this section are renumbered accordingly. (Bold text in these tables represents original and unmodified content.)

TABLE 29-10: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage*	—	10	30	mV	
D301	VICM	Input Common Mode Voltage*	0	—	VDD	V	
D302	CMRR	Common Mode Rejection Ratio*	55	—	—	dB	
300	TRESP	Response Time*(1)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	µs	

* Parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 29-11: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VRD310	CVRES	Resolution	VDD/24	—	VDD/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	AVDD – 1.5	LSb	
VRD312	CVRUR	Unit Resistor Value (R)	—	2k	—	Ω	
VR310	TSET	Settling Time(1)	—	—	10	µs	

Note 1: Settling time measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2008)

Original version of this document, for silicon revision A3. Includes silicon issues 1 (Core, RAM Operation), 2 (Core, BOR), 3 (JTAG, Programming), 4 (UART), 5 (I/O, PORTB), 6 (SPI, Master Mode), 7 (Input Capture) and 8 through 11 (USB).

Rev B Document (7/2008)

Revised silicon issues 4 (UART) and 6 (SPI, Master Mode) to reflect updated definition of issues. Added to revision A3: silicon issues 12 (UART, UERIF Interrupt), 13 (UART, FIFO Error Flags), 14 through 16 (UART, IrDA), 17 (I^2C, Master Mode), 18 (I^2C, Slave Mode), 19 (Memory, Program Space Visibility), 20 (ICSP), 21 (Core, Instruction Set), 22 (RTCC), 23 (SPI, Enhanced Buffer Modes) and 24 (A/D Converter).

Rev C Document (10/2008)

Added silicon issue 25 (SPI – Enhanced Buffer Mode) to revision A3.

Rev D Document (1/2009)

Added silicon issue 26 (Core – Code Protection) to revision A3.

Rev E Document (5/2009)

Added silicon issues 27 (CTMU – A/D Trigger) and 28 (Oscillator – LPRC) to revision A3. Ported document to unified silicon errata/data sheet clarification format.

Rev F Document (7/2009)

Added silicon revision A5 to document. Includes existing silicon issues 1 (Core, RAM Operation), 3 (JTAG, Programming), 8 through 11 (USB) and 21 (Core, Instruction Set). No additional new issues added.

Rev G Document (02/2010)

Added silicon issue 29 (Oscillator – Two-Speed Start-up) to silicon revisions A3 and A5.

Rev H Document (06/2010)

Added silicon issues 30 (Output Compare) and 31 (Interrupts – INTx) to silicon revisions A3 and A5.

Rev J Document (07/2010)

Added silicon issue 32 (A/D Converter) to silicon revisions A3 and A5.

Rev K Document (09/2010)

Revised silicon issue 32 (A/D Converter) to reflect updated definition of issues. Added data sheet clarification issue 1 (Guidelines For Getting Started with 16-Bit Microcontrollers).

Rev L Document (04/2011)

Added data sheet clarification issues 2, 3 and 4 (Electrical Characteristics). No new silicon issues added.

Rev M Document (6/2011)

Added silicon revision A6 to document. Includes all existing silicon issues that are applicable to silicon revision A5 (issues 1, 3, 8, 9, 10, 11, 21, 29, 31 and 32). No additional new issues added.

Rev N Document (11/2011)

Added silicon issues 33 (Oscillator), 34 (Output Compare – Interrupt), 35 (CTMU), 36 (UART), 37 (USB – Device Mode) and 38 (USB – Device and Host Modes).

Added data sheet clarification issues 5, 6 and 7 (Electrical Specifications).

Rev P Document (1/2013)

Revised data sheet clarification 5 to show BOR min value as 1.80V instead of 1.90V.

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