NXP DisplayPort-to-DVI/ HDMI level shifters PTN3300/3300A/ 3300B/3301

Signal translation from PCIe and DisplayPort to DVI and HDMI

To support the new, high-speed motherboard graphics chipsets from Intel, AMD/ATI, nVidia, and others, these devices provide electrical-level translation from DisplayPort signals to the current-mode outputs required to drive DVI and HDMI displays.

Key features

- High-speed TMDS level shifting up to 2.25 Gbps per lane (225-MHz character clock)
- DDC level shifting from 3.3 V (source) to 5 V (sink) with clock frequency from 0 to 400 kHz
- DDC active buffering and rise-time accelerator (PTN3301 only)
- DDC dongle-detect feature (PTN3301 only)
- HPD level shifting from 0 to 5 V (sink) to 0 to 3.3 V (source)
- HPD inverting level shifting to 1.1 V (source; PTN3300A only)
- Integrated 50–Ω termination resistors for AC-coupled differential inputs
- Single power supply voltage of 3.3 V ±10%
- High ESD resilience to 3.5 kV HBM, 1 kV CDM
- Pin-programmable power-saving mode disabling TMDS and DDC channels
- Automatic power-saving mode upon Hot Plug Detect (HPD) going LOW
- Back-current-safe design on all sink-side terminals

Applications

- Intel and AMD motherboards with reconfigurable I/O for display interfaces
- AMD/ATI and nVidia graphics cards with reconfigurable I/O for display interfaces
- DisplayPort-to-DVI and -HDMI dongles and cable assemblies
- Desktop and notebook motherboards with reconfigurable display interfaces

These high-speed level shifters translate from DisplayPort electrical signals to DVI and HDMI signals. The PTN3300 supports DVI and HDMI for motherboard and dongle applications up to 1.65 Gbps. The PTN3300A adds an inverting HPD channel and supports speeds up to 2.25 Gbps. The PTN3300B is a high-speed version of the PTN3300, supporting speeds up to 2.25 Gbps. The PTN3301 adds active DDC buffering and rise-time acceleration, plus the HDMI dongle-detect feature.

The level shifters let chipset vendors implement reconfigurable I/O on multimode display sources, and thereby support multiple display standards while keeping the number of chipset I/O pins low. When the chipset is configured to DVI or HDMI, it outputs TMDS-coded signals, while the chipset I/O pins employ AC-coupled PCI Express or DisplayPort electrical levels. Translation of the electrical levels is necessary because DVI and HDMI use DC-coupled, 3.3-V differential signaling.

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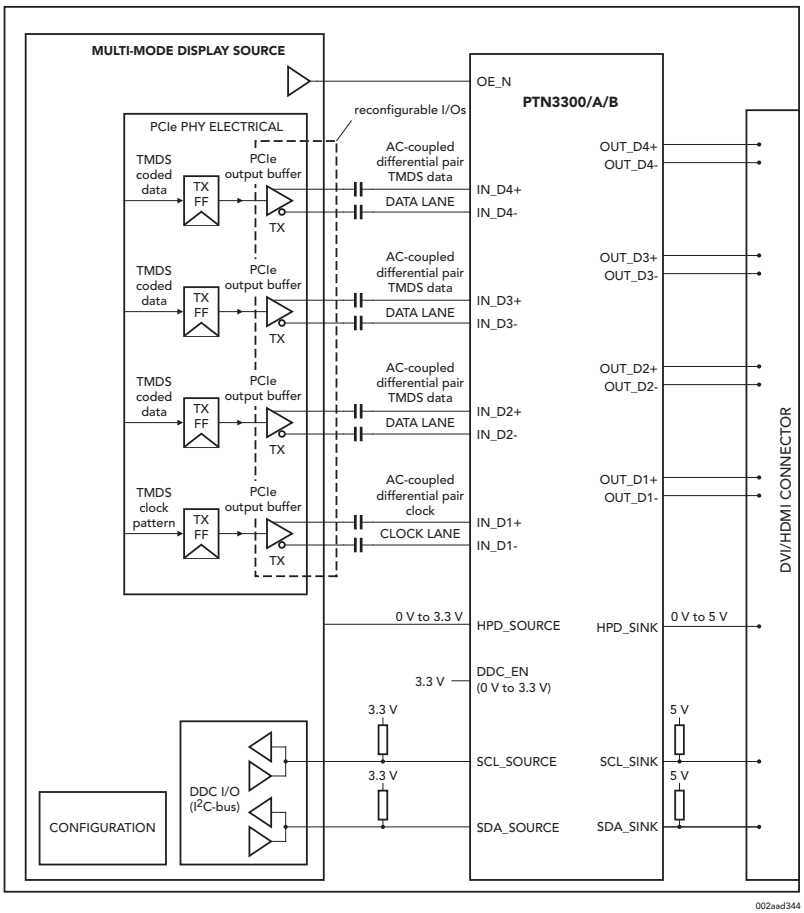
PTN3300/A/B

The PTN3300/A/B converts four lanes of low-swing, AC-coupled, differential input signals to DVI-compliant, open-drain, current-steering differential output signals. It provides level shifting for each differential lane, and equips each differential output with advanced wave-shaping for optimal performance. The PTN3300 operates at up to 1.65 Gbps, the PTN3300A and B versions operate at up to 2.25 Gbps.

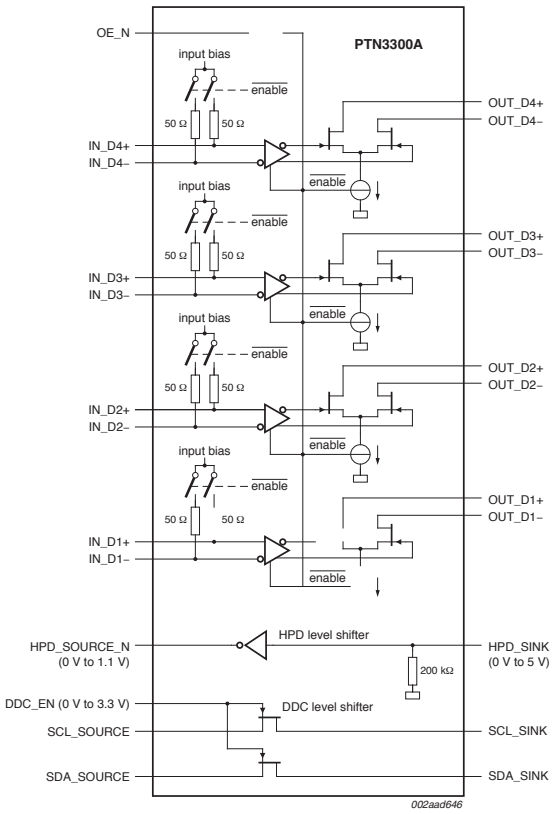
The PTN3300A is identical to PTN3300B, with the exception that its HPD channel is a logic-inverter function, and level shifts, on the source side, to a 1.1-V level instead of a 3.3-V logic level.

The PTN3300/A/B also supplies a single-ended, active buffer for voltage translation of the HPD signal, from 5 V on the sink side to 3.3 V on the source side. An integrated 200-kΩ pull-down resistor on the HPD sink input guarantees "input LOW" when no display is plugged in.

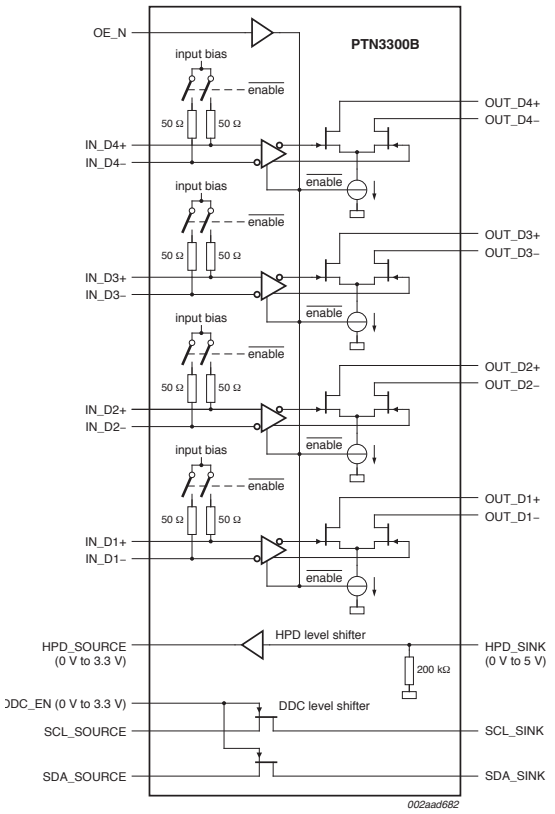
A DDC channel (clock and data lines) level shifts between 3.3 V on the source side and 5 V on the sink side. The DDC channel uses pass-gate technology, so it can level-shift and disable the clock and data lines, isolating the source from the sink. The DDC level shifting is back-power safe, to disallow back-drive current when the power is off or when DDC is not enabled.



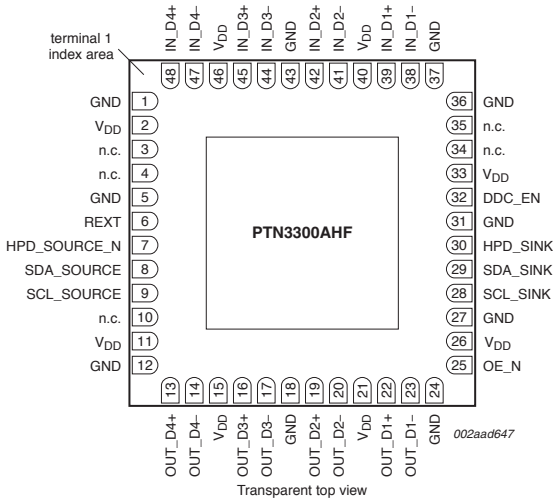
Application example, (except in case of PTN3300A, HPD_SOURCE is inverted and level shifted to 1.1 V)



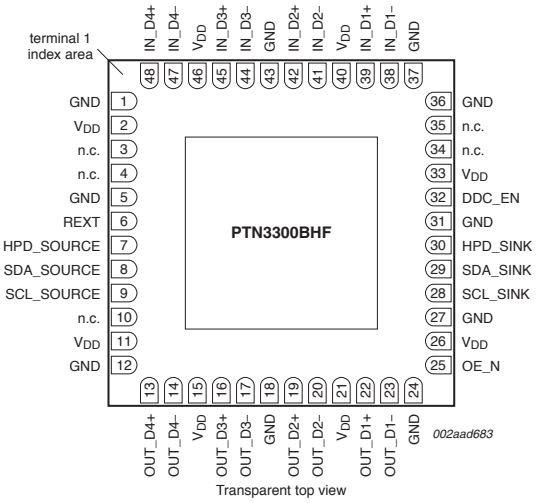
PTN3300A block diagram



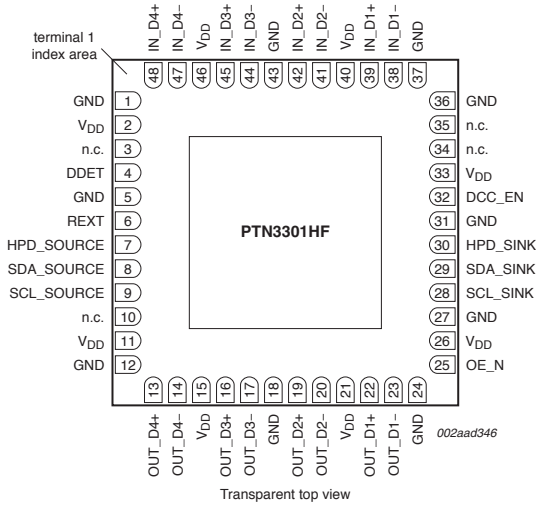
PTN3300B block diagram



PTN3300A pinout diagram (HWQFN48R and HWQFN48)



PTN3300B pinout diagram (HWQFN48R and HWQFN48)



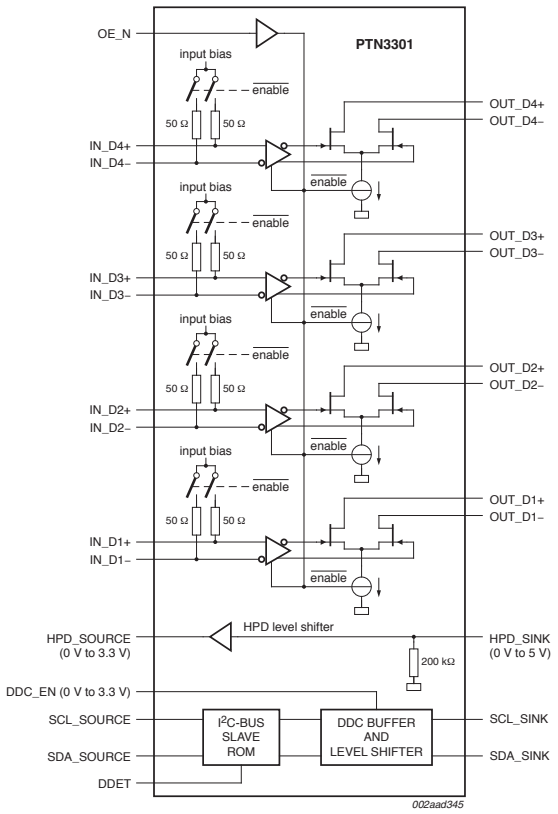
PTN3301 pinout diagram (HWQFN48R and HWQFN48)

PTN3301

The PTN3301 is the same as the PTN3300B, but with additional features for HDMI applications. It has actively buffered DDC lines that meet HDMI's more stringent specifications for capacitive loading, and, in accordance with the DisplayPort interoperability guidelines, is capable of responding to an I²C-based query to detect an HDMI dongle via the DDC channel.

All the level shifters are available in a very thin, 48-pin HWQFNR (7 x 7 x 0.7 mm) or a 48-pin HWQFN (7 x 7 x 0.65 mm) package. All operate from a 3.3-V power supply, and save power by using active pin control and automatic control via hot-plug detection. When there is no monitor actively connected to the device, the device automatically goes into idle mode and consumes only a negligible amount of supply current.

For more information visit **www.nxp.com/displayport**



PTN3301 block diagram

Selection guide

Feature	PTN3300	PTN3300A	PTN3300B	PTN3301
Data rate per lane	1.65 Gbps	2.25 Gbps	2.25 Gbps	2.25 Gbps
TMDS level shifters	•	•	•	•
DDC active buffer / level shifter				•
DDC passive level shifter	•	•	•	
HPD level shifter	3.3-V, non-inverting	1.1-V, inverting	3.3-V, non-inverting	3.3-V, non-inverting
Automatic standby mode upon HPD_SINK = LOW	•	•	•	•
Interchangeable TMDS data and clock lanes	•	•	•	•
Responds to I²C-bus HDMI dongle detection				Optional
Applications	DVI motherboard, dongle	DVI, HDMI motherboard	DVI, HDMI motherboard, dongle	DVI, HDMI motherboard, dongle

Ordering information

Type number	Package type	Dimensions	Package feature
PTN3300HF	HWQFN48R	7 x 7 x 0.7 mm	Non-wraparound terminals
PTN3300AHF	HWQFN48R	7 x 7 x 0.7 mm	Non-wraparound terminals
PTN3300BHF	HWQFN48R	7 x 7 x 0.7 mm	Non-wraparound terminals
PTN3301HF	HWQFN48R	7 x 7 x 0.7 mm	Non-wraparound terminals
PTN3300AHF2	HWQFN48	7 x 7 x 0.65 mm	Wrap-around terminals
PTN3300BHF2	HWQFN48	7 x 7 x 0.65 mm	Wrap-around terminals
PTN3301HF2	HWQFN48	7 x 7 x 0.65 mm	Wrap-around terminals

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