Analog Power AM1541CE

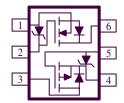
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$r_{DS(on)}(\Omega)$	$I_{D}(A)$			
40	$140 @ V_{GS} = 10V$	1.2			
	190 @ $V_{GS} = 4.5V$	1.1			
-20	$300 @ V_{GS} = -10V$	-0.9			
	$390 @ V_{GS} = -4.5V$	-0.8			

- Low r<sub>DS(on)</sub> provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-6 saves board space
- Fast switching speed
- High performance trench technology







$\mathbf{r}$						
ப	m	$\sim$ 1	ÞΔ	0	te	_
						ı

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter			N-Channel	P-Channel	Units		
Drain-Source Voltage		$V_{DS}$	40	-40	V		
Gate-Source Voltage			20	-20	v		
	T <sub>A</sub> =25°C	T	1.2	-0.9			
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	$\mathbf{I}_{\mathrm{D}}$	1	-0.7	A		
Pulsed Drain Current <sup>b</sup>			1.2	-1.2			
Continuous Source Current (Diode Conduction) <sup>a</sup>			0.25	-0.25	A		
D a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$		0.3	0.3	w		
Power Dissipation <sup>a</sup>			0.21	0.21	VV		
Operating Junction and Storage Temperature Range			-55 to	°C			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
M . I	t <= 5 sec	$R_{THJA}$	415	0000		
Maximum Junction-to-Ambient <sup>a</sup>	Steady-State		460	C/W		

1

## Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit		
Static								
Cata Sauraa Threahald Valtaga	V	$V_{DS} = V_{GS}$ , $I_{D} = 250 \text{ uA}$ (N-ch)	1			V		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$ (P-ch)	-1			V		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V$ , $V_{GS} = \pm 20 V$			±10	uA		
Zero Gate Voltage Drain Current	1	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$ (N-ch)			1	uА		
Zero date voltage Brain Gurrent	I <sub>DSS</sub>	$V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}$ (P-ch)			-1	uA		
On-State Drain Current	la,	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$ (N-ch)	1.5			Α		
On State Blain Suitent	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$ (P-ch)	-1.5			Α		
		$V_{GS} = 10 \text{ V}, I_D = 1.2 \text{ A}$ (N-ch)			140	mΩ		
Drain-Source On-Resistance	rno()	$V_{GS} = 4.5 \text{ V}, I_D = 0.96 \text{ A}$ (N-ch)			190	11152		
Diam-Source On-Hesistance	r <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -0.8 \text{ A}$ (P-ch)			300	mΩ		
		$V_{GS} = -4.5 \text{ V}, I_D = -0.64 \text{ A}$ (P-ch)			390	11177		
Forward Transconductance	g <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 1.2 \text{ A}$ (N-ch)		3		S		
1 orward Transconductance	91s	$V_{DS} = -10 \text{ V}, I_{D} = -0.8 \text{ A}$ (P-ch)		5		S		
Diode Forward Voltage	$V_{SD}$	$I_S = 0.2 \text{ A}, V_{GS} = 0 \text{ V}$ (N-ch)		0.65		V		
Diode i orward voltage	<b>V</b> SD	$I_S = -1.2 \text{ A}, V_{GS} = 0 \text{ V}$ (P-ch)		-0.66		V		
		Dynamic						
Total Gate Charge	$Q_g$	N - Channel		5				
Gate-Source Charge	$Q_gs$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.2 \text{ A}$		0.3		nC		
Gate-Drain Charge	$Q_{gd}$	VDS = 10 V, VGS = 4.3 V, ID = 1.2 /\ =		0.7				
Turn-On Delay Time	$t_{d(on)}$	N - Channel		8		ns		
Rise Time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 8.3 \Omega,$		13				
Turn-Off Delay Time	$t_{d(off)}$	$I_D = 1.2 A,$		25				
Fall Time	t <sub>f</sub>	$V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		8				
Input Capacitance	$C_{iss}$	N - Channel		73				
Output Capacitance	Coss	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		25		рF		
Reverse Transfer Capacitance	$C_{rss}$	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, 1 = 1 101112		20				
Total Gate Charge	$Q_g$	P - Channel		4				
Gate-Source Charge	$Q_gs$	$V_{DS} = -10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = -0.8 \text{ A}$		0.5		nC		
Gate-Drain Charge	$Q_{gd}$	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 1.0 V, V <sub>D</sub> = 0.0 / V		0.9				
Turn-On Delay Time	t <sub>d(on)</sub>	P - Channel		8				
Rise Time	t <sub>r</sub>	$V_{DD}=\text{-}10~V,~R_L=12.5~\Omega,$		10		ns		
Turn-Off Delay Time	$t_{d(off)}$	$I_D = -0.8 A$ ,		28				
Fall Time	t <sub>f</sub>	$V_{GEN}$ = -4.5 $V$ , $R_{GEN}$ = 6 $\Omega$		13				
Input Capacitance	C <sub>iss</sub>	P - Channel		120				
Output Capacitance	Coss	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		28		pF		
Reverse Transfer Capacitance	$C_{rss}$	- LO - 10 v, vG5 - 0 v, 1 - 1 WII IZ		25				

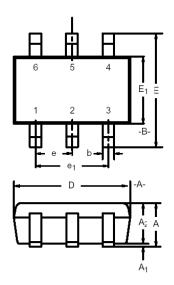
## Notes

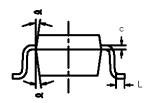
- a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

## Package Information

**SC-70: 6LEAD** 





	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.90	_	1.10	0.035	_	0.043
A <sub>1</sub>	_	_	0.10	_	_	0.004
A <sub>2</sub>	0.80	_	1.00	0.031	_	0.039
b	0.15	_	0.30	0.006	_	0.012
С	0.10	-	0.25	0.004	_	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC				0.026BSC	;
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
~	7°Nom 7°Nom					