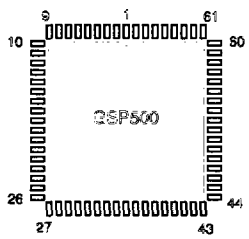
VGA/NTSC Video Genlock Processor with Overlay

Overview

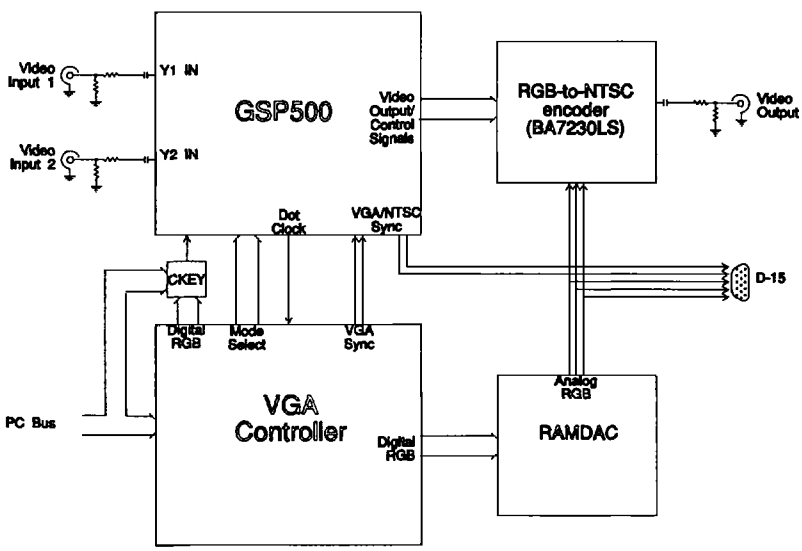
The **GSP500** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard NTSC televisions or recorded on a VCR. Additionally, the **GSP500** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP500** also allows VGA and video images to be overlaid on the same television screen. The **GSP500** meets or exceeds all RS-170A broadcast standards for timing accuracy and allows the VGA controller to maintain true NTSC compatibility at all times. The **GSP500** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR already have full BIOS support available for the **GSP500**.

Features

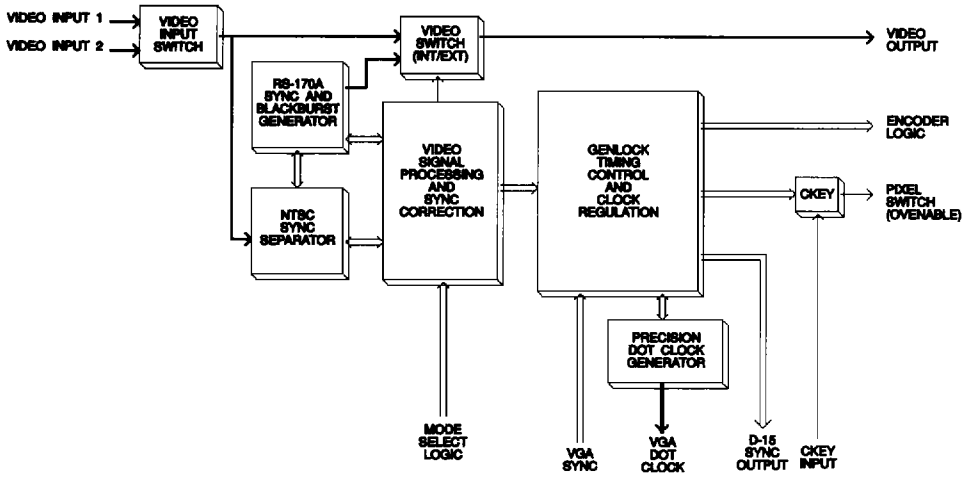
- Direct input of NTSC or S-Video (S-VHS and Hi-8 video).
- On board NTSC/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 3.579545 MHz and 14.31818 MHz phase locked outputs.
- Meets or exceeds alltiming specifications for studio and broadcast television.
- High efficiency NTSC/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of NTSC/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and NTSC/S-Video modes.
- NTSC/S-Video conversion support for all VGA and Extended VGA modes with 480 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA, plus extended VGA operation up to 135 MHz.
- Low power consumption, ideal for laptop computers.



68-Pin PLCC
K-10



Internal Block Diagram



Theory of Operation

The **GSP500** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP500** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP500** from VGA mode to NTSC mode. Under NTSC mode, the **GSP500** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP500** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with an NTSC reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP500** provides an RGB-to-NTSC encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP500**.

During NTSC modes the **GSP500** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

Block definition

Video Input Switch

The Video Input Switch selects whether the **GSP500** uses VIDEO INPUT 1 or VIDEO INPUT 2 as the external video source. It is controlled by an external pin of the **GSP500**.

NTSC Sync Separator

The **GSP500** contains a high quality sync separator to allow direct input of NTSC, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP500** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.

RS-170A Sync and Black Burst Generator

RS170A Sync Generator

The studio quality built-in video sync generator allows the **GSP500** to operate without an external video input and still maintain broadcast video timing. This assures NTSC compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

Black Burst Generation

Most RGB-to-NTSC encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP500** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP500** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

INT/EXT Video Switch

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP500** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

Video Signal Processing and Correction

Video Signal Processing

The Video Signal Processing circuitry of the **GSP500** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or NTSC operation and selects whether genlock to external video is to be enabled.

Sync Correction

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

Genlock Timing Control and Clock Regulation

The **GSP500** looks at the input sync from the VGA controller and determines how to alter the dot clock to create RS-170A timing. Both the frequency and the method can change with different VGA modes. The **GSP500** enables virtually any VGA controller capable of interlacing to create RS-170A timing. The **GSP500**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 480 or fewer lines, to meet RS-170A NTSC specifications. The **GSP500** genlock timing control and clock regulation design is awaiting patent approval.

Precision Dot Clock Generator

The **GSP500** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

CKEY

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP500** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.

PIN NUMBER	NAME	DESCRIPTION
1	VLE	VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.
2	ODD/EVEN	ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
3	BP	BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-NTSC encoders.
4	DATAIN	Data input for inserting SMPTE time code in video signal.
5	CB	COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of NTSC signal.
6	CS	COMPOSITE SYNC. NTSC Composite sync output for RGB-to-NTSC encoders. Gated off during VGA modes.
7	CKEY	COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.
8	TEST	For ICS use only.
9	VSYNCOUT	VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.
10	DATAFRAME	TTL level framing signal active during lines 10-20. For use in time code applications.
11	OVENABLE	OVERLAY ENABLE. Fast pixel rate switch. HIGH displays NTSC output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.
12	I/ES	INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.
13	LOC/REM	LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.
14	BRSTACT	For ICS use only.
15	$\overline{\text{FRTSTOUT}}$	For ICS use only, wire to pin 37.
16	HS	HORIZONTAL SYNC. For some RGB-to-NTSC encoders. Gated off during VGA modes.
17	$\overline{\text{HRSTOUT}}$	For ICS use only.
18	HSYNCOUT	HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.
19	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
20	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
21	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
22	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
23	FS5	Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and NTSC frequencies. See Dot Clock Generation and NTSC Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details.

PIN NUMBER	NAME	DESCRIPTION
24	FS4	Frequency Select 4. Selects between VGA Dot Clock frequencies and NTSC modes.
25	FS3	Frequency Select 3. Selects between VGA Dot Clock frequencies and NTSC modes.
26	FS2	Frequency Select 2. Selection between VGA Dot Clock frequencies and NTSC modes.
27	FS1	Frequency Select 1. Selects between VGA Dot Clock frequencies and NTSC modes.
28	FS0	Frequency Select 0. Selects between VGA Dot Clock frequencies and NTSC modes.
29	EXTSYNC	For ICS use only.
30	VCR1	HIGH permits using VCRs as an input.
31	CLAMPLEV	Clamping level adjustment for video input. See Application Notes for more details.
32	Y2	NTSC video input number 2. Note: This is also the Y (luminance) input for S-Video systems.
33	Y1	NTSC video input number 1. Note: This is also the Y (luminance) input for S-Video systems.
34	C2	C (Chrominance) input number 2 for S-Video systems.
35	C1	C (Chrominance) input number 1 for S-Video systems.
36	3.58SC	3.579545 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.
37	$\overline{\text{FRSTIN}}$	For ICS use only, wire to pin 15.
38	AVDD	5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.
39	GFF	Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.
40	VCOLF	VCO LOOP FILTER CIRCUIT. External RC circuit used in VCO circuitry. See Application Notes for component values.
41	SYNCTHRS	Sync threshold adjustment for video input. See Application Notes schematic.
42	VGAO/E	VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
43	COUT	C (Chrominance) OUTPUT. C output for S-Video systems.
44	$\overline{\text{RST}}$	Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.
45	YOUT	Y (Luminance) OUTPUT. NTSC video output when the NTSC/SVID input is in the HIGH state. Y output for S-Video systems when the NTSC/SVID input is in the LOW state.
46	$\overline{\text{HALIGNOUT}}$	For ICS use only, wire to pin 62.
47	SYSLF	SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.
48	XTALI	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.
49	XTALO	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.

PIN NUMBER	NAME	DESCRIPTION
50	AVSS	Analog ground. We strongly recommend the use of a multilayer board and a ground plane.
51	VID1/2	Input selector. High for Y1/C1. Low for Y2/C2.
52	VCOOUT	For ICS use only, do not wire.
53	FILTSEL	For ICS use only, wire to pin 57.
54	DOTCLOCK	Clock signal input for VGA chip.
55	$\overline{\text{VFF}}$	Inverts field 1 and field 2 of NTSC sync. Normally tied HIGH.
56	$\overline{\text{VCR2}}$	LOW modifies sync characteristics to permit operation with VCR input.
57	VGA/NTSC	Mode identification output signal. HIGH indicates a VGA mode, LOW indicates an NTSC mode.
58	$\overline{\text{BG}}$	BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-NTSC encoders.
59	LOC/REM IN	For ICS use only, wire to pin 13.
60	VGAHSYNC	VGA HORIZONTAL SYNC. HSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
61	VGAVSYNC	VGA VERTICAL SYNC. VSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
62	$\overline{\text{HALIGNIN}}$	For ICS use only, wire to pin 46.
63	NTSC/SVID	NTSC/S-VIDEO. Selects between NTSC and S-Video output. HIGH=NTSC; Low=S-Video.
64	VS	VERTICAL SYNC. NTSC Vsync output for RGB-to-NTSC encoders. Gated off during VGA modes.
65	4XSC	4 TIMES SUBCARRIER OUTPUT. 14.31818 MHz signal phase-locked to the chroma burst signal.
66	PCLK	PCLK from VGA chip.
67	DATAOUT	TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.
68	SCH	SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders.

BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2 , 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

Horizontal CRTC Registers

CRTC INDEX	CRTC REGISTER	Modes: 00, 01, 04, 05, 0D	Modes: 02, 03, 06, 07, 0E, 0F, 10	Modes: 11, 12, 13
00	HT	35	6B	66
01	HDE	27	4F	4F
02	SHB	2A	53	52
03	EHB	96	8B	87
04	SHR	30	5B	58
05	EHR	92	83	80

Vertical CRTC Registers

CRTC INDEX	CRTC REGISTER	200 Line Modes: (Non-Interlaced) 00, 01, 02, 03, 07, 04, 05, 06, 0D, 0E, 13	350 Line Modes: (Interlaced) 0F, 10	480 Line Modes: (Interlaced) 12, 13
06	VT	05	05	05
07	OVERFLOW	11	11	11
10	VRS	E0	D3	F4
11	VRE	84	87	88
12	VDE	C7	AE	EF
15	SVB	DC	CF	F0
16	EVB	F2	E5	06

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

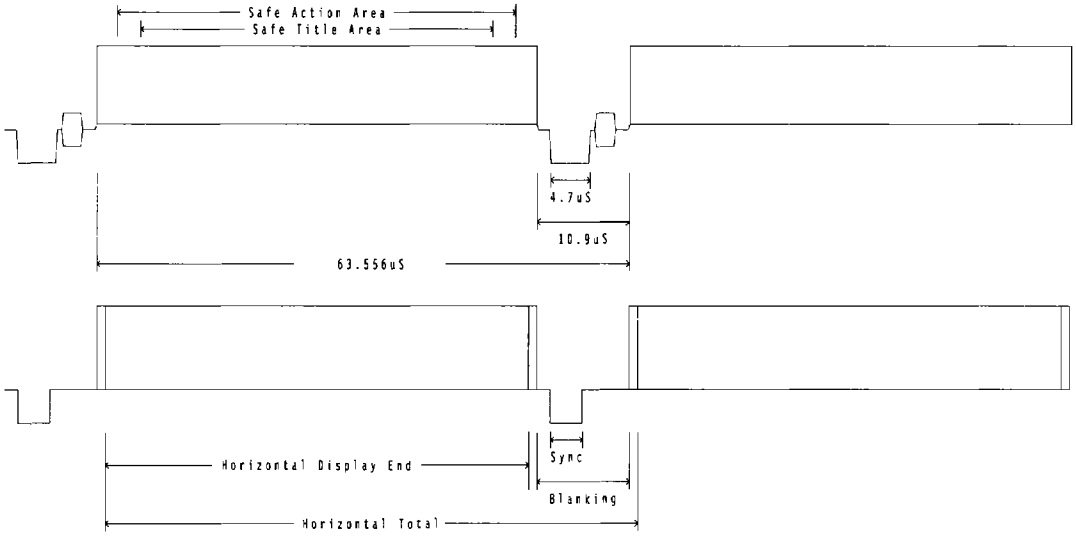
Miscellaneous Output Register

NTSC mode	Color Modes: 00, 01, 02, 03, 04, 05, 06, 0D, 0E, 10, 11, 12, 13	Monochrome Modes: 07, 0F
Genlock (GL)	23	22
Overlay (OV)	27	26
Video Only (VO)	2B	2A
Graphics Only (GO)	2F	2E

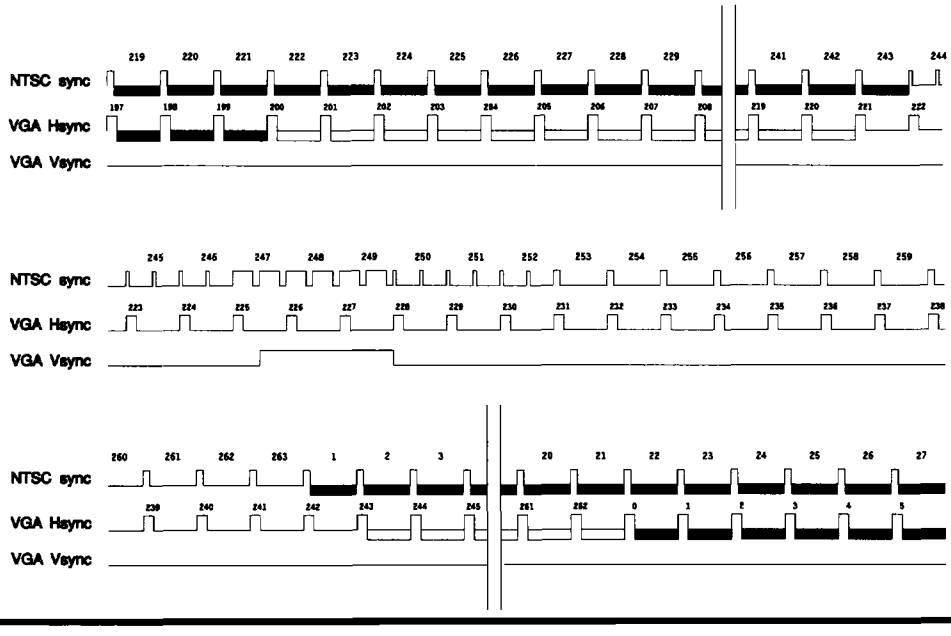
Extended Registers

Turn OFF all DOTCLOCK/2 bits.

NTSC vs VGA Horizontal Timing



NTSC vs VGA Vertical Timing (200 line mode)



Electrical Specifications

Operating temperature range 0°C to 70°C

Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply	A_{VDD}	4.5	5.0	5.5	Volts
Digital Supply	D_{VDD}	4.5	5.0	5.5	Volts
Operating Current - VGA Mode	I_{DD} (VGA)		35		mA
Operating Current - NTSC Mode	I_{DD} (NTSC)		50		mA

Input Signals

SIGNAL TITLE	PIN #	TYPICAL VALUE	OPERATING CONDITIONS
Y1	33	1 V_{P-P}	75 Ohm load
C1	35	1V_{P-P}	75 Ohm load
Y2	32	1V_{P-P}	75 Ohm load
C2	34	1V_{P-P}	75 Ohm load
VID1/2	51	TTL/CMOS	High = Y1,C1; Low = Y2,C2
NTSC/SVID	63	TTL/CMOS	High = NTSC; Low = S-Video
VGAVSYNC	61	TTL/CMOS	Positive polarity
VGAHSYNC	60	TTL/CMOS	Positive polarity
FS0-5	28-23	TTL/CMOS	Address/mode select
CKEY	7	TTL/CMOS	High = RGB; Low = NTSC
PCLK	66	TTL/CMOS	Pixel (DAC) Clock from VGA
I/ES	12	TTL/CMOS	High = Internal sync Low = External sync
DATAIN	4	TTL/CMOS	Active during DATAFRAME
CLAMPLEV	31	1-1.5 V	
SYNCTHRS	41	CLAMPLEV +0.1 V	
VLE	1	TTL/CMOS	Tie to V_{DD} through resistor
RST/	44	TTL/CMOS	Tie to V_{DD} through resistor

G

Output Signals

SIGNAL TITLE	PIN#	TYPICAL VALUE	OPERATING CONDITIONS
VSYNCOUT	9	TTL	Positive polarity during NTSC modes
HSYNCOUT	18	TTL	Composite sync during NTSC modes
VS	64	$1V_{P-P}$	Positive polarity
HS	16	$1V_{P-P}$	Positive polarity
CS	6	$1V_{P-P}$	Positive polarity
DOTCLOCK	54	TTL	
YOUT	45	$1V_{P-P}$	75 Ohm load
COUT	43	$1V_{P-P}$	75 Ohm load
3.58SC	36	TTL	3.579545 MHz
4XSC	65	TTL	14.31818 MHz
LOC/REM	13	TTL	High = local; Low = remote
OVENABLE	11	TTL	High = NTSC; Low = RGB
VGA/NTSC	57	TTL	High = VGA; Low = NTSC
CB	25	TTL	Positive polarity
ODD/EVEN	2	TTL	High = odd field; Low = even field
VGAO/E	42	TTL	High = VGA odd field Low = VGA even field
BG/	58	TTL	Negative polarity
FP/	3	TTL	Negative polarity
SCH	68	TTL	Positive polarity
DATAFRAME	10	TTL	Lines 10-20
DATAOUT	67	TTL	Active during DATAFRAME

Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP500**. See the BIOS manual or contact ICS applications engineering for additional information.

FREQUENCY (MHz)	FS5	FS4,FS3,FS2	FS1	FS0
50.350	0	1	0	0
56.644	0	1	0	1
65.028	0	1	1	0
72.000	0	1	1	1
75.000	1	0	0	0
80.000	1	0	0	1
89.800	1	0	1	0
110.000	1	0	1	1
GenLock	1	1	0	0
OVerlay	1	1	0	1
Video Only	1	1	1	0
Graphics Only	1	1	1	1

FREQUENCY (MHz)	FS5,FS3	FS4, FS2	FS1	FS0
25.175	0	1	0	0
28.322	0	1	0	1
40.000	0	1	1	0
44.900	0	1	1	1
GenLock	1	1	0	0
OVerlay	1	1	0	1
Video Only	1	1	1	0
Graphics Only	1	1	1	1

G

Ordering Information

GSP500V

Example:

ICS XXXX V

Package Type
V=PLCC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device