

# 512Kx8 MONOLITHIC SRAM

## FEATURES

- Access Times 15, 17, 20ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 36 lead Ceramic SOJ (Package 100)
  - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Thinpack™ Flat Pack (Package 321)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Low Power CMOS
- Low Voltage Operation
  - 3.3V ± 10% Power Supply
- Commercial, Industrial and Military Temperature Range
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required
- Three State Output

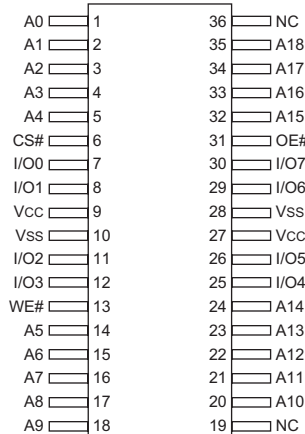
\* This product is subject to change without notice.

### REVOLUTIONARY PINOUT

### EVOLUTIONARY PINOUT

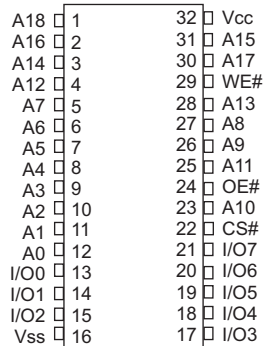
36 FLAT PACK  
36 CSOJ

TOP VIEW



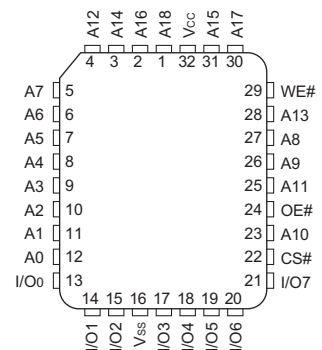
32 DIP  
32 CSOJ (DE)  
32 FLAT PACK (FF)

TOP VIEW



32 CLCC

TOP VIEW



### PIN DESCRIPTION

|         |                   |
|---------|-------------------|
| A0-18   | Address Inputs    |
| I/O 0-7 | Data Input/Output |
| CS#     | Chip Select       |
| OE#     | Output Enable     |
| WE#     | Write Enable      |
| Vcc     | Power Supply      |
| Vss     | Ground            |



**ABSOLUTE MAXIMUM RATINGS**

| Parameter                   | Symbol           | Min  | Max  | Unit |
|-----------------------------|------------------|------|------|------|
| Operating Temperature       | T <sub>A</sub>   | -55  | +125 | °C   |
| Storage Temperature         | T <sub>STG</sub> | -65  | +150 | °C   |
| Signal Voltage Range to GND | V <sub>G</sub>   | -0.5 | 4.6  | V    |
| Junction Temperature        | T <sub>J</sub>   |      | 150  | °C   |
| Supply Voltage              | V <sub>CC</sub>  | -0.5 | 4.6  | V    |

**TRUTH TABLE**

| CS# | OE# | WE# | MODE        | DATA I/O | POWER   |
|-----|-----|-----|-------------|----------|---------|
| H   | X   | X   | Standby     | High Z   | Standby |
| L   | L   | H   | Read        | Data Out | Active  |
| L   | X   | L   | Write       | Data In  | Active  |
| L   | H   | H   | Out Disable | High Z   | Active  |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter             | Symbol          | Min  | Max                   | Unit |
|-----------------------|-----------------|------|-----------------------|------|
| Supply Voltage        | V <sub>CC</sub> | 3.0  | 3.6                   | V    |
| Input High Voltage    | V <sub>IH</sub> | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage     | V <sub>IL</sub> | -0.3 | +0.8                  | V    |
| Operating Temp. (Mil) | T <sub>A</sub>  | -55  | +125                  | °C   |

**CAPACITANCE**

T<sub>A</sub> = +25°C

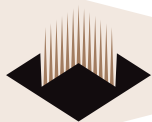
| Parameter          | Symbol           | Conditions                          | Max | Unit |
|--------------------|------------------|-------------------------------------|-----|------|
| Input capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 12  | pF   |
| Output capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0 V, f = 1.0 MHz | 12  | pF   |

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS - CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ 125°C

| Parameter                | Symbol          | Conditions  | Min | Max | Unit |
|--------------------------|-----------------|---|-----|-----|------|
| Input Leakage Current    | I <sub>LI</sub> | V <sub>CC</sub> = 3.6, V <sub>IN</sub> = GND to V <sub>CC</sub>                           |     | 10  | μA   |
| Output Leakage Current   | I <sub>LO</sub> | CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub> |     | 10  | μA   |
| Operating Supply Current | I <sub>CC</sub> | CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6           |     | 100 | mA   |
| Standby Current          | I <sub>SS</sub> | CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6           |     | 50  | mA   |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 4.0mA   |     | 0.4 | V    |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -4.0mA  | 2.4 |     | V    |



**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ 125°C

| Parameter Read Cycle               | Symbol            | -15 |     | -17 |     | -20 |     | Unit |
|------------------------------------|-------------------|-----|-----|-----|-----|-----|-----|------|
|                                    |                   | Min | Max | Min | Max | Min | Max |      |
| Read Cycle Time                    | t <sub>RC</sub>   | 15  |     | 17  |     | 20  |     | ns   |
| Address Access Time                | t <sub>AA</sub>   |     | 15  |     | 17  |     | 20  | ns   |
| Output Hold from Address Change    | t <sub>OH</sub>   | 0   |     | 0   |     | 0   |     | ns   |
| Chip Select Access Time            | t <sub>ACS</sub>  |     | 15  |     | 17  |     | 20  | ns   |
| Output Enable to Output Valid      | t <sub>OE</sub>   |     | 8   |     | 8   |     | 10  | ns   |
| Chip Select to Output in Low Z     | t <sub>CLZ1</sub> | 1   |     | 1   |     | 1   |     | ns   |
| Output Enable to Output in Low Z   | t <sub>OLZ1</sub> | 0   |     | 0   |     | 0   |     | ns   |
| Chip Disable to Output in High Z   | t <sub>CHZ1</sub> |     | 8   |     | 8   |     | 10  | ns   |
| Output Disable to Output in High Z | t <sub>OHZ1</sub> |     | 8   |     | 8   |     | 10  | ns   |

1. This parameter is guaranteed by design but not tested.

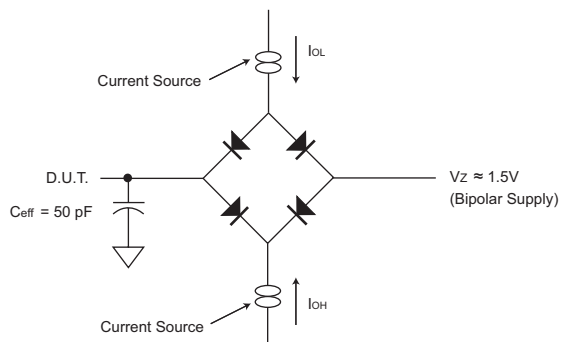
**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ 125°C

| Parameter Write Cycle            | Symbol            | -15 |     | -17 |     | -20 |     | Unit |
|----------------------------------|-------------------|-----|-----|-----|-----|-----|-----|------|
|                                  |                   | Min | Max | Min | Max | Min | Max |      |
| Write Cycle Time                 | t <sub>WC</sub>   | 15  |     | 17  |     | 20  |     | ns   |
| Chip Select to End of Write      | t <sub>CW</sub>   | 12  |     | 12  |     | 14  |     | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>   | 12  |     | 12  |     | 14  |     | ns   |
| Data Valid to End of Write       | t <sub>DW</sub>   | 9   |     | 9   |     | 10  |     | ns   |
| Write Pulse Width                | t <sub>WP</sub>   | 12  |     | 14  |     | 14  |     | ns   |
| Address Setup Time               | t <sub>AS</sub>   | 0   |     | 0   |     | 0   |     | ns   |
| Address Hold Time                | t <sub>AH</sub>   | 0   |     | 0   |     | 0   |     | ns   |
| Output Active from End of Write  | t <sub>OW1</sub>  | 2   |     | 3   |     | 3   |     | ns   |
| Write Enable to Output in High Z | t <sub>WHZ1</sub> |     | 8   |     | 8   |     | 9   | ns   |
| Data Hold Time                   | t <sub>DH</sub>   | 0   |     | 0   |     | 0   |     | ns   |

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT**



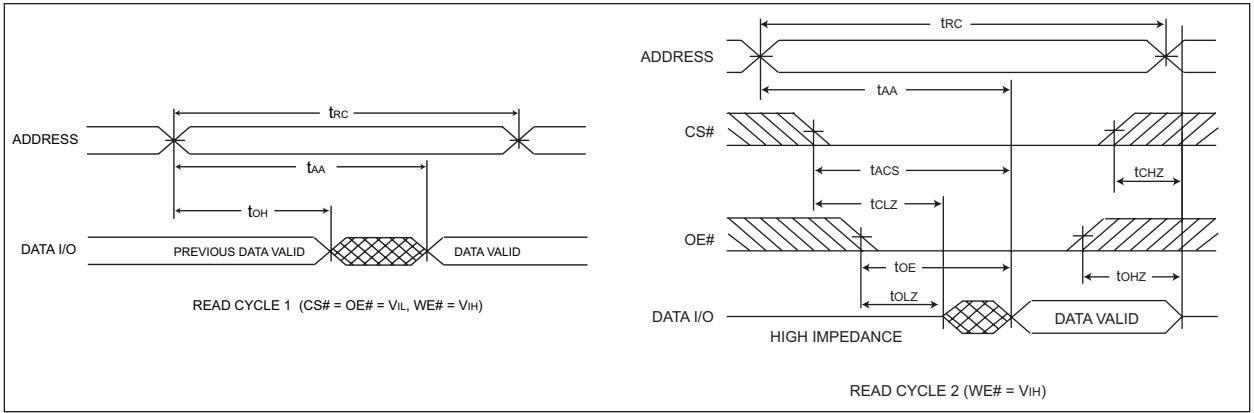
**AC TEST CONDITIONS**

| Parameter                        | Typ  | Unit |
|----------------------------------|--|------|
| Input Pulse Levels               | V <sub>IL</sub> = 0, V <sub>IH</sub> = 2.5 | V    |
| Input Rise and Fall              | 5  | ns   |
| Input and Output Reference Level | 1.5  | V    |
| Output Timing Reference Level    | 1.5  | V    |

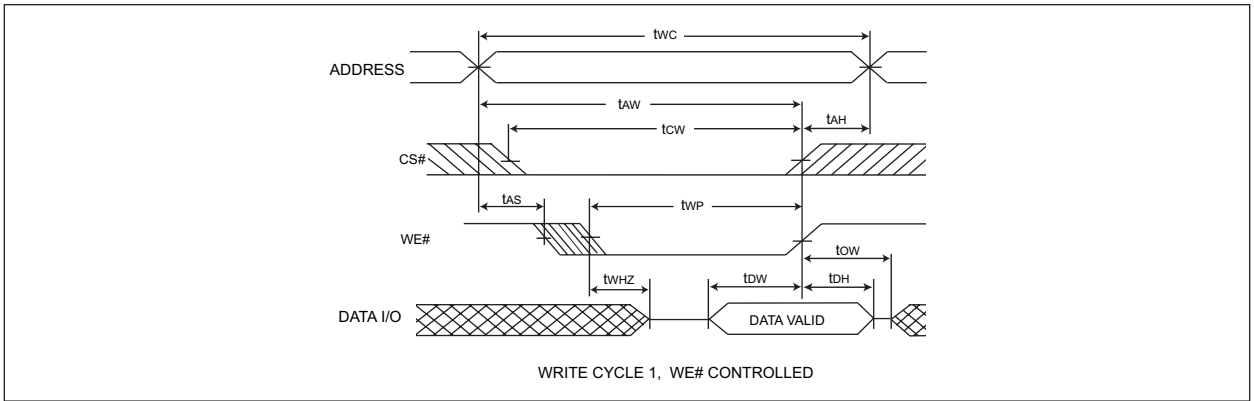
Notes:  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



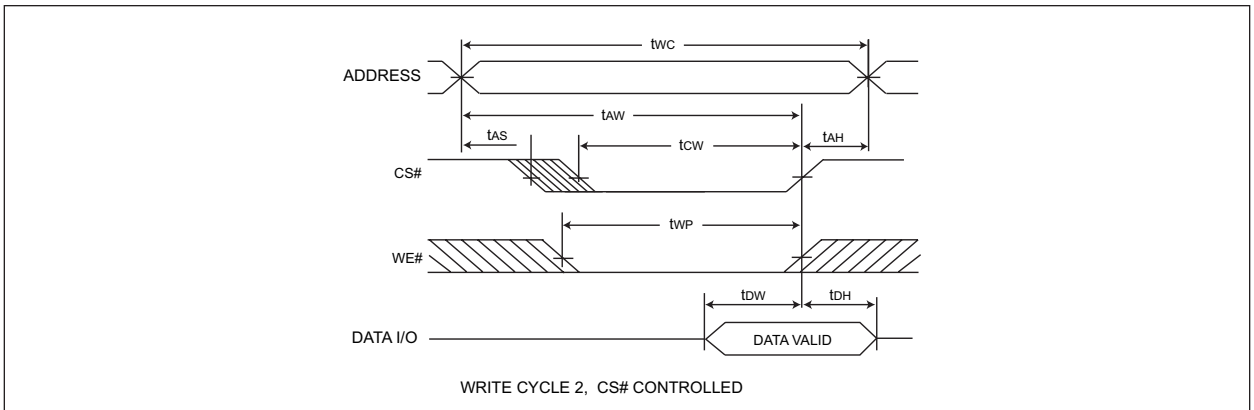
### TIMING WAVEFORM - READ CYCLE



### WRITE CYCLE - WE# CONTROLLED

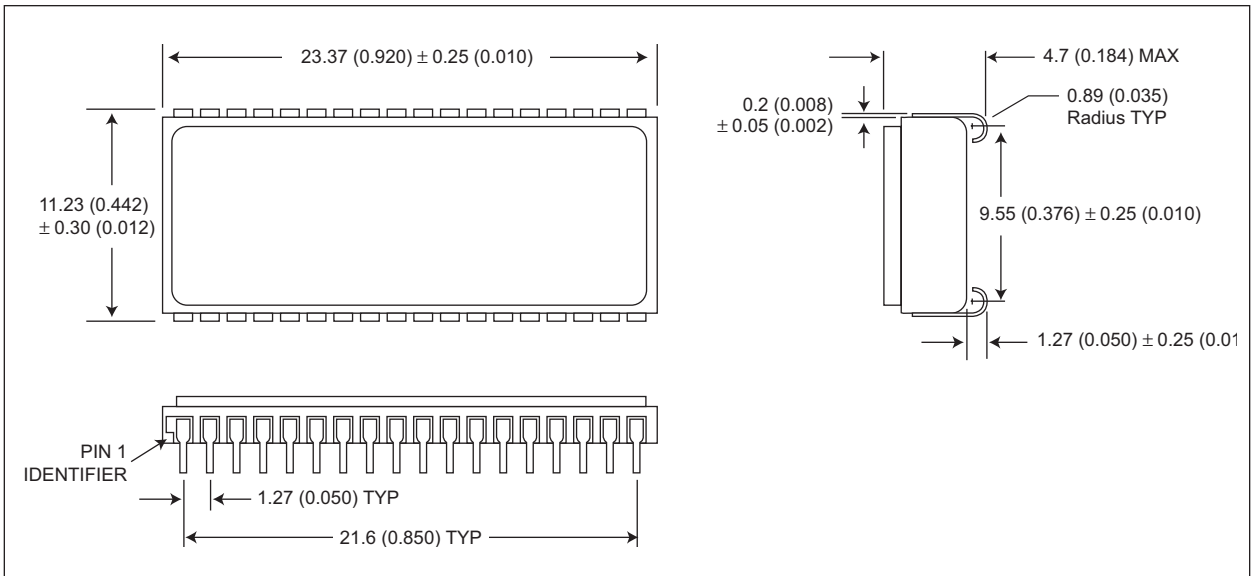


### WRITE CYCLE - CS# CONTROLLED



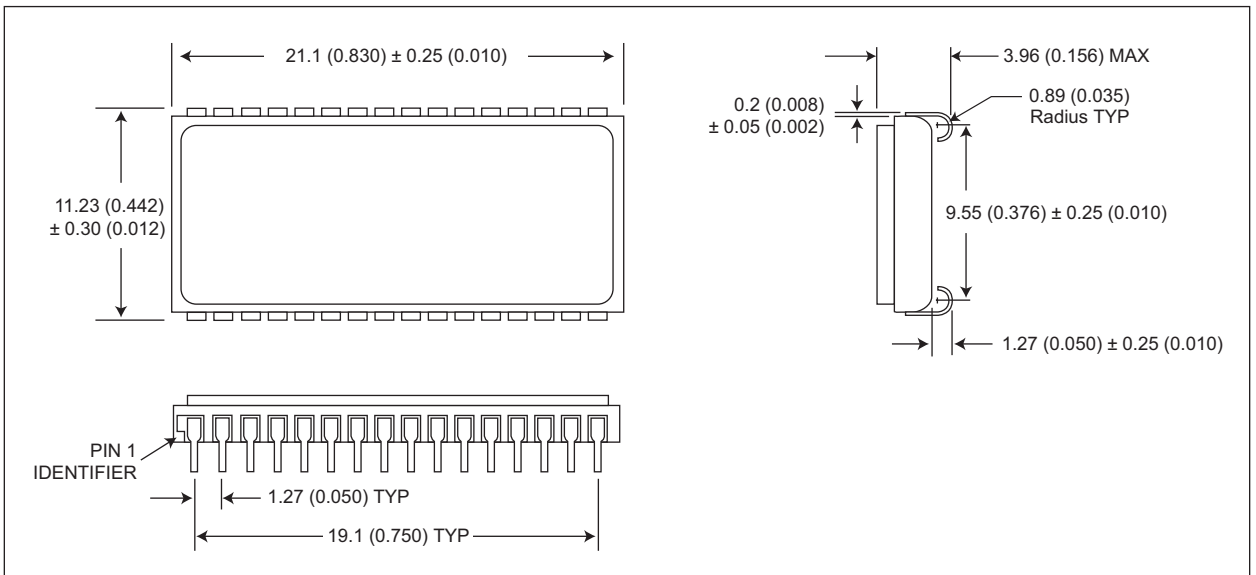


**PACKAGE 100: 36 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

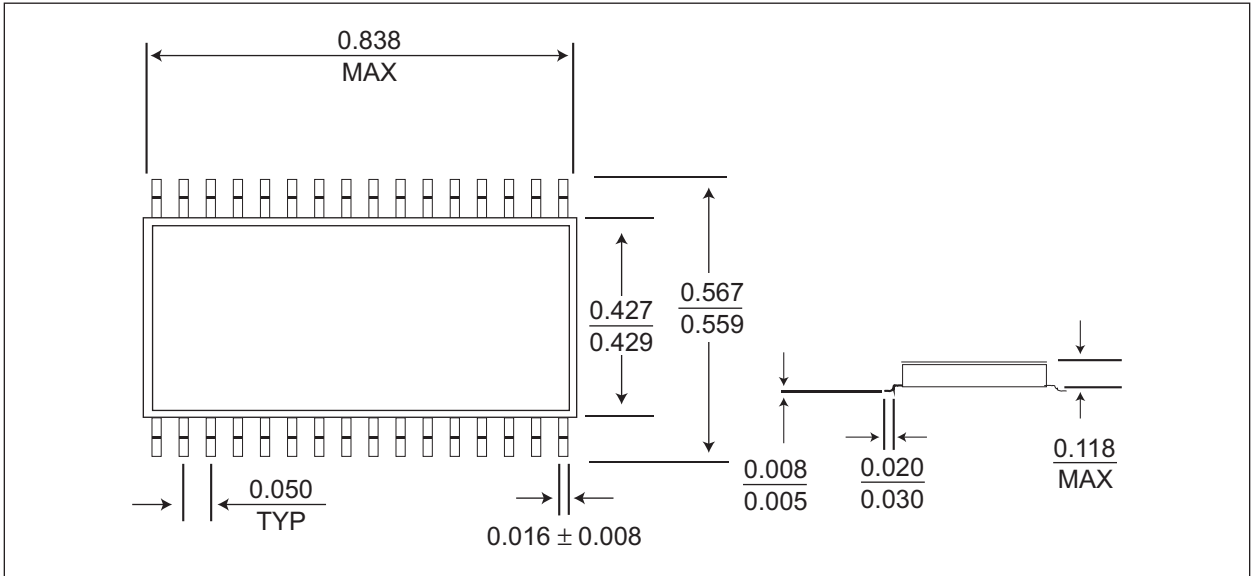
**PACKAGE 101: 32 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

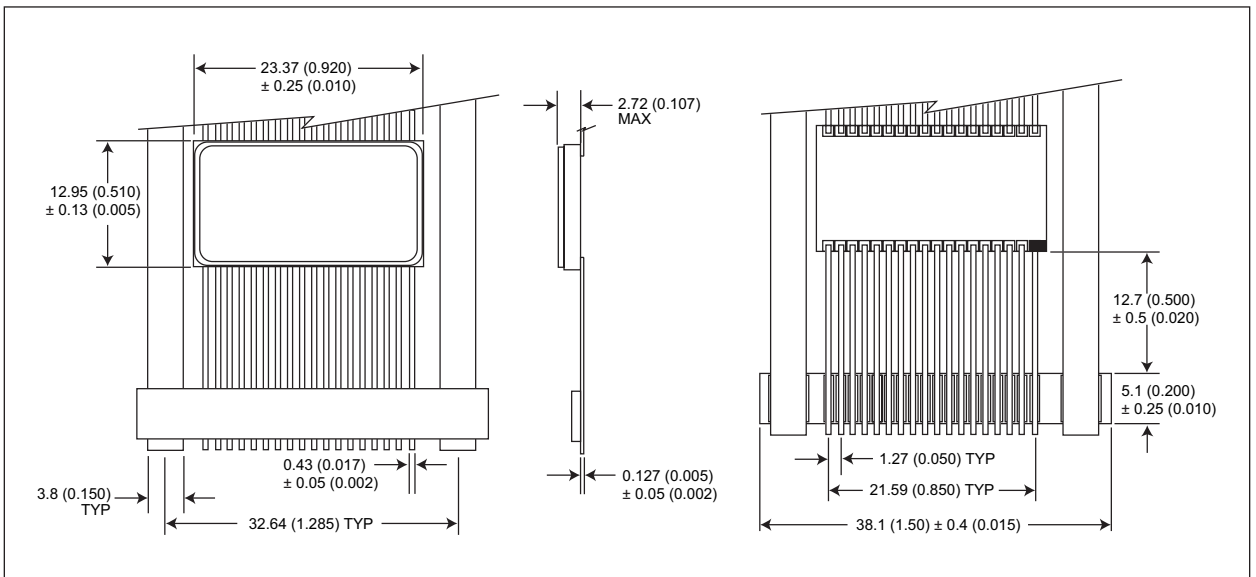


**PACKAGE 321: 32 PIN CERAMIC THINPACK™ FLATPACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

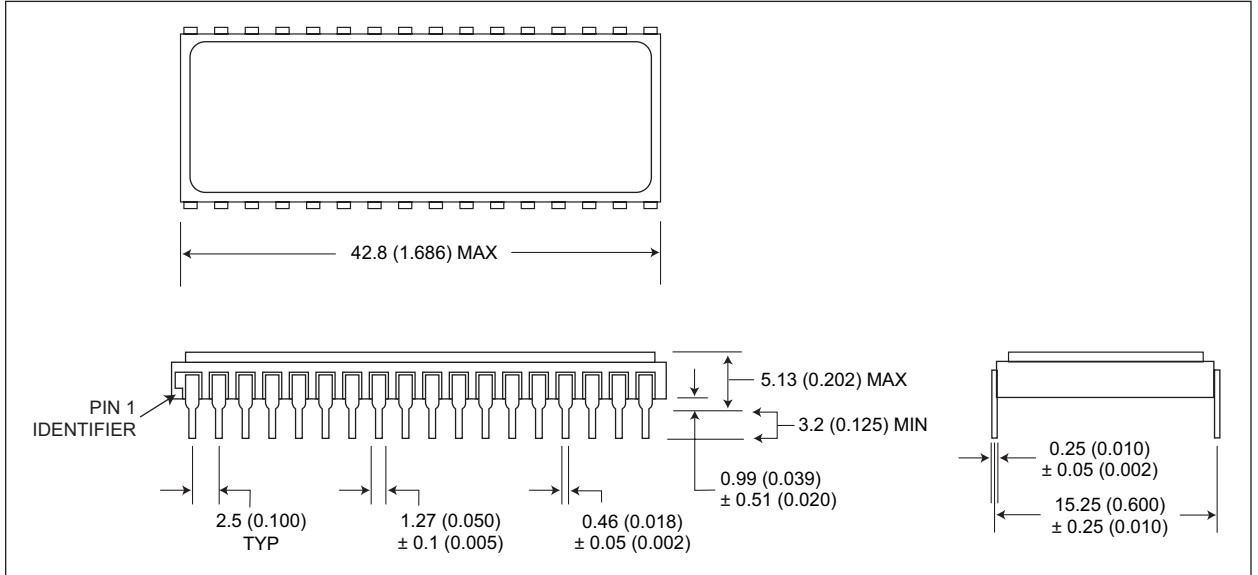
**PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK**



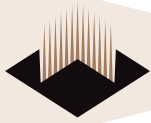
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



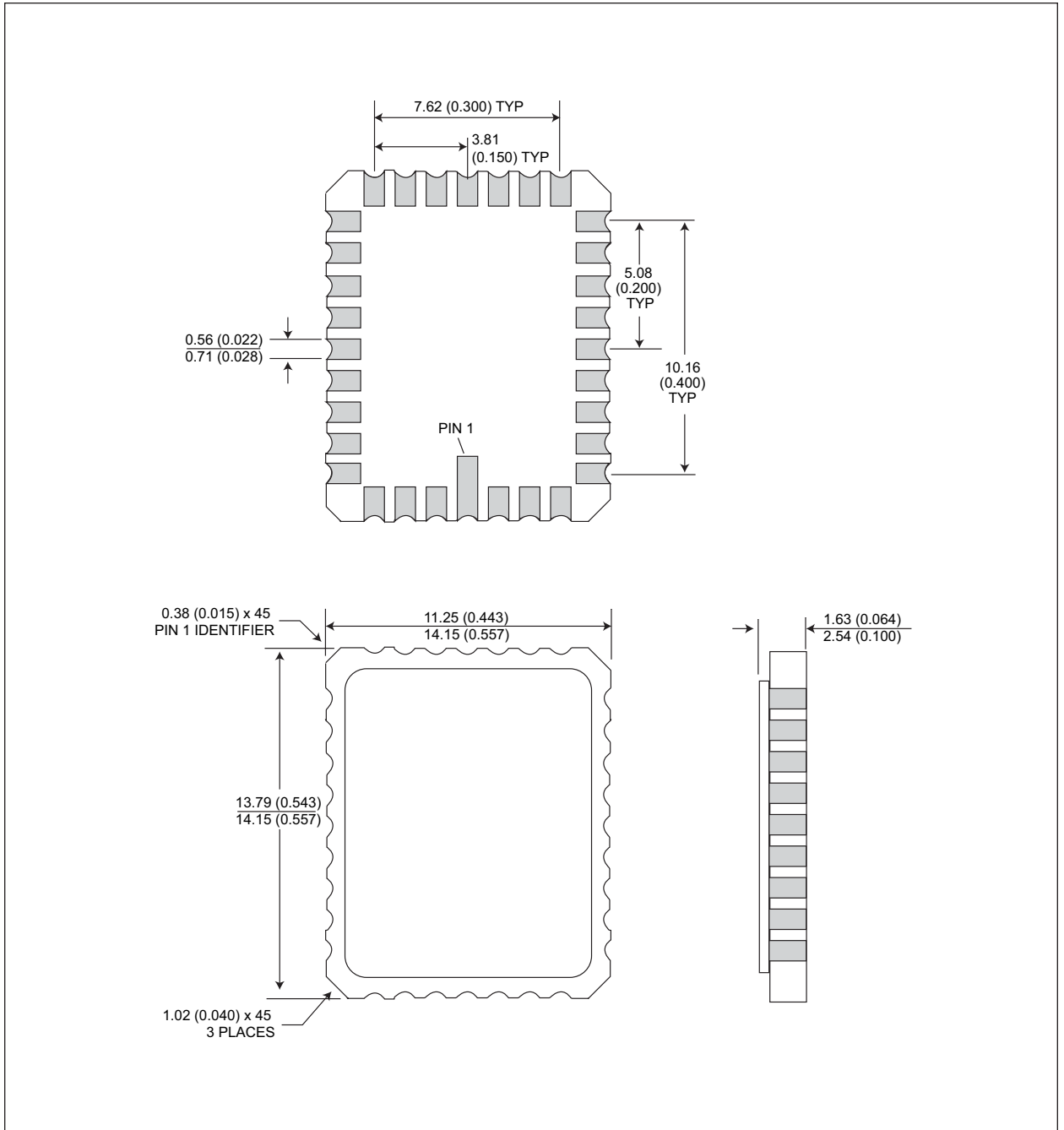
**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





ORDERING INFORMATION

W M S 512K 8 V - XXX X X X

WHITE ELECTRONIC DESIGNS CORP.

MONOLITHIC

SRAM

ORGANIZATION, 512K x 8

LOW VOLTAGE SUPPLY 3.3V ± 10%

ACCESS TIME (ns)

PACKAGE:

- C = 32 pin Ceramic 0.600" DIP (Package 300)
- CL = 32 pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
- DJ = 36 Lead Ceramic SOJ (Package 100)
- F = 36 Lead Ceramic Flat Pack (Package 226)
- FF = 32 Lead Ceramic Thinpack™ Flat Pack (Package 321)

DEVICE GRADE:

- M = Military Screened    -55°C ≤ T<sub>A</sub> ≤ 125°C
- I = Industrial            -40°C ≤ T<sub>A</sub> ≤ 85°C
- C = Commercial         0°C ≤ T<sub>A</sub> ≤ 70°C

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads