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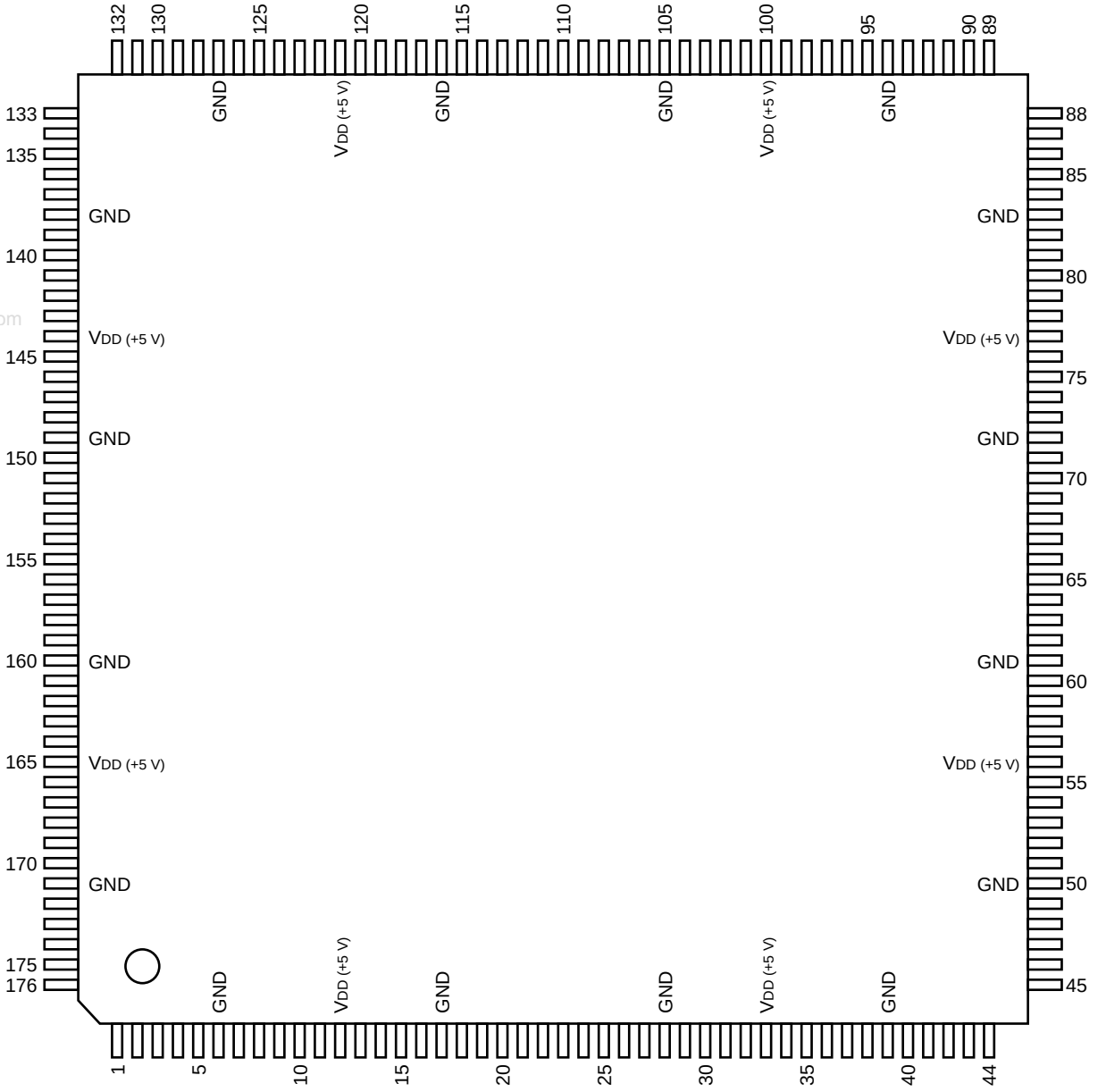
IL11

C-MOS A/V DATA REC PROCESS (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	DIAG	45	O	GWDATA5	89	I	CADRS5	133	I	R_DAT5
2	I	$\overline{\text{AINT0}}$	46	O	GWDATA6	90	I	CADRS6	134	I	R_DAT6
3	I	$\overline{\text{AINT1}}$	47	O	GWDATA7	91	I	CADRS7	135	I	R_DAT7
4	I	$\overline{\text{PAY\_EN}}$	48	O	GWSYNC	92	I	CRD	136	I	$\overline{\text{I\_PORT0}}$
5	I	$\overline{\text{AINT2}}$	49	O	GWSTART	93	I	CWR	137	I	$\overline{\text{I\_PORT1}}$
6	—	GND	50	—	GND	94	—	GND	138	—	GND
7	I	$\overline{\text{ADEN2}}$	51	O	$\overline{\text{GWEND}}$	95	I	CCS	139	O	TEST_R
8	I	$\overline{\text{SW\_DET}}$	52	O	$\overline{\text{WE\_V}}$	96	I/O	CDATA0	140	O	PINT_RE0
9	I	$\overline{\text{PCERD}}$	53	O	$\overline{\text{WE\_A}}$	97	I/O	CDATA1	141	O	PINT_RE1
10	I	$\overline{\text{IN\_FP}}$	54	O	$\overline{\text{WE\_T}}$	98	I/O	CDATA2	142	O	PINT_RE2
11	O	RX_INIT	55	O	$\overline{\text{RSTW\_V}}$	99	I/O	CDATA3	143	O	PINT_RE3
12	—	V_{DD}	56	—	V_{DD}	100	—	V_{DD}	144	—	V_{DD}
13	O	$\overline{\text{DIAGRE}}$	57	O	$\overline{\text{RSTW\_A}}$	101	I/O	CDATA4	145	O	PINT_RE4
14	O	$\overline{\text{DIAGRST}}$	58	O	$\overline{\text{RSTW\_T}}$	102	I/O	CDATA5	146	O	PINT_RE5
15	O	$\overline{\text{ATRIWE}}$	59	O	W_CKO	103	I/O	CDATA6	147	O	PINT_RE6
16	O	$\overline{\text{ATRIRSTW}}$	60	I	W_CK	104	I/O	CDATA7	148	O	PINT_RE7
17	—	GND	61	—	GND	105	—	GND	149	—	GND
18	I	S_DAT0	62	I	GRDATA0	106	O	DMA_DAT0	150	O	W_DAT0
19	I	S_DAT1	63	I	GRDATA1	107	O	DMA_DAT1	151	O	W_DAT1
20	I	S_DAT2	64	I	GRDATA2	108	O	DMA_DAT2	152	O	W_DAT2
21	I	S_DAT3	65	I	GRDATA3	109	O	DMA_DAT3	153	O	W_DAT3
22	I	S_DAT4	66	I	GRDATA4	110	O	DMA_DAT4	154	O	W_DAT4
23	I	S_DAT5	67	I	GRDATA5	111	O	DMA_DAT5	155	O	W_DAT5
24	I	S_DAT6	68	I	GRDATA6	112	O	DMA_DAT6	156	O	W_DAT6
25	I	S_DAT7	69	I	GRDATA7	113	O	DMA_DAT7	157	O	W_DAT7
26	I	S_DAT8	70	I	$\overline{\text{GRSYNC}}$	114	O	$\overline{\text{DFWE1}}$	158	O	O_PORT0
27	I	S_DAT9	71	I	$\overline{\text{GRSTART}}$	115	O	$\overline{\text{DFWE2}}$	159	O	O_PORT1
28	—	GND	72	—	GND	116	—	GND	160	—	GND
29	O	WCCONT0	73	I	GREND	117	O	$\overline{\text{DFWE3}}$	161	O	$\overline{\text{MAIN\_RE}}$
30	O	WCCONT1	74	O	$\overline{\text{RE\_V}}$	118	O	$\overline{\text{DFWE4}}$	162	O	$\overline{\text{P\_INIT}}$
31	O	WCCONT2	75	O	$\overline{\text{RSTR\_V}}$	119	O	$\overline{\text{DFRSTW}}$	163	O	$\overline{\text{M\_RSTR}}$
32	O	WCCONT3	76	I	XSM	120	I	$\overline{\text{DMA\_DREQ}}$	164	I	XACK
33	—	V_{DD}	77	—	V_{DD}	121	—	V_{DD}	165	—	V_{DD}
34	O	WCCONT4	78	I	XTST	122	O	RCCONT0	166	I	BCK
35	O	$\overline{\text{MAIN\_WE}}$	79	I	SDI	123	O	RCCONT1	167	I	XTCK
36	O	$\overline{\text{W\_INIT}}$	80	O	SDO	124	O	RCCONT2	168	O	$\overline{\text{TEST\_W}}$
37	O	$\overline{\text{M\_RSTW}}$	81	O	$\overline{\text{RE\_A}}$	125	O	RCCONT3	169	O	WCCONT5
38	O	H_REC	82	O	$\overline{\text{RSTR\_A}}$	126	O	RCCONT4	170	O	RCCONT5
39	—	GND	83	—	GND	127	—	GND	171	—	GND
40	O	GWDATA0	84	I	CADRS0	128	I	R_DAT0	172	O	$\overline{\text{EXT\_CS0}}$
41	O	GWDATA1	85	I	CADRS1	129	I	R_DAT1	173	O	$\overline{\text{EXT\_CS1}}$
42	O	GWDATA2	86	I	CADRS2	130	I	R_DAT2	174	I	R_CK
43	O	GWDATA3	87	I	CADRS3	131	I	R_DAT3	175	I	$\overline{\text{SG\_FP}}$
44	O	GWDATA4	88	I	CADRS4	132	I	R_DAT4	176	I	$\overline{\text{SYS\_RST}}$

INPUT

$\overline{\text{ADEN2}}$, $\overline{\text{PAY\_EN}}$	; DATA ENABLE (SDDI RX)
$\overline{\text{AINT0}}$	; VIDEO/NON-AV INTERRUPT (SDDI RX)
$\overline{\text{AINT1}}$	; AUDIO INTERRUPT (SDDI RX)
$\overline{\text{AINT2}}$	; ATTRIBUTE INTERRUPT (SDDI RX)
BCK, XACK, XTCK	; IC TEST PIN
CADRS0 - CADRS7	; CPU ADDRESS BUS
CCS	; CPU CHIP SELECT
CRD	; CPU READ PULSE
CWR	; CPU WRITE PULSE
$\overline{\text{DMA\_DREQ}}$	; DMA FIFO WRITE REQUEST
GRDATA0 - GRDATA7	; GOP DELAY READ DATA IN
GREND	; GOP DELAY END PULSE
$\overline{\text{GRSTART}}$	; GOP DELAY START PULSE
$\overline{\text{GRSYNC}}$	; GOP DELAY SYNC
$\overline{\text{I\_PORT0}}$, $\overline{\text{I\_PORT1}}$	; IN PORT
$\overline{\text{IN\_FP}}$, $\overline{\text{SG\_FP}}$	; FRAME PULSE IN
$\overline{\text{PCERD}}$	; PAYLOAD CRCC ERROR (SDDI RX)
R_CK	; READ PROCESS CLOCK
R_DAT0 - R_DAT7	; MAIN FIFO READ DATA IN
S_DAT0 - S_DAT10	; DATA IN (SDDI RX)
SDI, XSM, XTST	; IC TEST PIN
$\overline{\text{SW\_DET}}$	; SWITCHING DETECT (SDDI RX)
$\overline{\text{SYS\_RST}}$	; POWER ON RESET
W_CK	; WRITE PROCESS CLOCK

OUTPUT

ATRIRSTW	; ATTRIBUTE FIFO RSTW
ATRIWE	; ATTRIBUTE FIFO WRITE ENABLE
DFRSTW	; DMA FIFO RSTW
DFWE1 - DFWE4	; DMA FIFO WRITE ENABLE
DIAG	; DIAG MODE SEL (H: DIAG MODE)
DIAGRE	; DIAG FIFO READ ENABLE
DIAGRST	; DIAG FIFO RSTR
DMA_DAT0 - DMA_DAT7	; DMA FIFO WRITE DATA OUT
EXT_CS0, EXT_CS1	; CHIP SELECT OUT
GWDATA0 - GWDATA7	; GOP DELAY WRITE DATA OUT
GWEND	; GOP DELAY END PULSE OUT
GWSTART	; GOP DELAY START PULSE OUT
GWSYNC	; GOP DELAY SYNC OUT
H_REC	; REC LED DRIVE (H: REC)
M_RSTR	; MAIN FIFO RSTR
M_RSTW	; MAIN FIFO RSTW
MAIN_RE	; MAIN FIFO READ ENABLE
MAIN_WE	; MAIN FIFO WRITE ENABLE
O_PORT0, O_PORT1	; OUT PORT
P_INIT	; MAIN FIFO POWER ON INITIAL PULSE
PINT_RE0 - PINT_RE7	; MAIN FIFO POWER ON INITIAL CHIP SELECT
RCCOUNT0 - RCCOUNT5	; MAIN FIFO READ CHIP COUNTER OUT
RE_A	; AUDIO FIFO READ ENABLE
RE_V	; VIDEO FIFO READ ENABLE
RSTR_A	; AUDIO FIFO RSTR
RSTR_V	; VIDEO FIFO RSTR
RSTW_A	; AUDIO FIFO RSTW
RSTW_T	; TIME CODE FIFO RSTW
RSTW_V	; VIDEO FIFO RSTW
RX_INIT	; CPU INTERRUPT
SDO	; IC TEST PIN
TEST_R	; IC TEST
TEST_W	; IC TEST
W_CKO	; WRITE PROCESS CLOCK OUT
W_DAT0 - W_DAT7	; MAIN FIFO WRITE DATA OUT
W_INIT	; MAIN FIFO POWER ON INITIAL PULSE
WCCOUNT0 - WCCOUNT5	; MAIN FIFO WRITE CHIP COUNTER OUT
WE_A	; AUDIO FIFO WRITE ENABLE
WE_T	; TIME CODE FIFO WRITE ENABLE
WE_V	; VIDEO FIFO WRITE ENABLE

INPUT/OUTPUT

CDATA0 - CDATA7	; CPU DATA BUS 0 - 7