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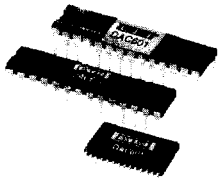


DAC601

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

12-Bit 250MHz Latched ECL DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW HARMONICS: 72dB AT 10MHz
- LOW SETUP AND HOLD TIMES
- LOW POWER: 480mW
- LOW REFERENCE DRIFT: ±20ppm/°C
- LOW GLITCH
- STREAMLINED PINOUT: 28-Pin 0.3" DIP or SOIC Package

APPLICATIONS

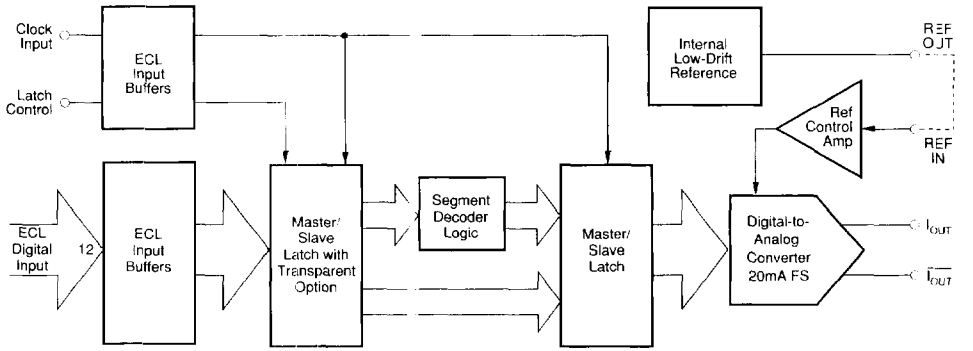
- TELECOMMUNICATIONS: Local Oscillator Generation Modulated Baseband Generation
- FUNCTION GENERATORS
- ARBITRARY WAVEFORM GENERATORS
- TEST EQUIPMENT

DESCRIPTION

The DAC601 is a high speed, high performance digital-to-analog converter capable of 256MHz data rates. It is complete with a low-drift reference and internal latches.

The user-friendly dual master/slave latches require minimal setup and hold times, thus reducing the speed and cost requirements of the driving memory. These optimized latches are also designed to suppress digital feedthrough. Segmented DAC current sources further minimize the output glitch.

The DAC601 has been optimized for excellent spurious-free dynamic performance while dissipating only 480mW. This high performance device is available in streamlined (0.3" wide) 28-pin DIP and SOIC packages. A mil temp range DIP is also available.



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SPECIFICATIONS

T_A = +25°C, $-V_S$ = 5.2V, using internal reference unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC601P, U, HSQ MIN	DAC601P, U, HSQ TYP	DAC601P, U, HSQ MAX	DAC601PB, UB MIN	DAC601PB, UB TYP	DAC601PB, UB MAX	UNITS
TEMPERATURE RANGE									
Specification: P, PB, U, UB Grades	Tambient		–40		+85	*		*	°C
HSQ Grade			–55		+125	*		*	°C
Thermal Resistance: H Package	Junction-to-Ambient			75			*		C/W
P Package				75			*		C/W
U Package				75			*		C/W
DIGITAL INPUTS									
Logic Inputs				ECL Compatible			*		
Resolution					12			*	Bits
ECL Logic Input Levels: V_{IL}	Logic "0"	Full	–1.48	–1.95	–2	*	*	*	V
I_{IL}		Full			10			*	µA
V_{IH}	Logic "1"	Full	–1.1	–0.75	0	*	*	*	V
I_{IH}		Full			10			*	µA
DIGITAL TIMING									
Input Data Rate		Full	DC		256	*		*	MHz
Clock Pulse Width High or Low		Full		1.25			*		ns
Set-up Time		Full		500			*		ps
Hold Time (Referred to Clock)		Full		500			*		ps
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Analog Output Format				Complementary, Unipolar			*		
Full Scale Output Current, Both Outputs	All Bits High, R_L = 0Ω	Full		–19.995			*		mA
Low Output Current, Both Outputs	All Bits Low, R_L = 0Ω			0			*		mA
Output Resistance[1]	No External Termination	Full	632	744	856	*	*	*	Ω
Output Capacitance		Full		3			*		pF
REFERENCE CHARACTERISTICS									
REFIN	Reference Input			–2.5			*		V
Input Range			0		–2.7	*		*	V
Input Resistance				2			*		kΩ
Full Power Bandwidth				500			*		kHz
REFOUT	Internal Reference								
Accuracy		+25°C	–2.49	–2.5	–2.51	*	*	*	V
Drift		Full		20			*		ppm/°C
TRANSFER CHARACTERISTICS									
Monotonicity		Full		Guaranteed			Guaranteed		
Differential Linearity Error	Worst Case Code	+25°C		0.5	1.0		0.3	0.5	LSB
		Full			2.0		0.35	0.5	LSB
Integral Linearity Error		+25°C		0.5	1.0		0.5	0.75	LSB
		Full			2.0		0.6	1.0	LSB
Gain Error		Full		0.3	0.7		0.2	0.5	%FSR
Output Offset		Full		0.4	0.7		0.2	0.5	%FSR
Power Supply Rejection	$\Delta -V_S$ = ±10%	Full		±0.03	±0.07		*	*	%FSR/%
TIME DOMAIN PERFORMANCE									
Rise Time		+25°C		770			*		ps
Fall Time		+25°C		510			*		ps
Settling Time									
±0.1%	Major Carry, 1LSB Change	Full		4			*		ns
±.024%		Full		15			*		ns
Glitch Energy		Full		1.5			*		pV_S
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range (SFDR)									
f_O = 1MHz	f_{CLOCK} = 50MHz	+25°C		76			*		dBFS
f_O = 5MHz	f_{CLOCK} = 50MHz	+25°C		74			*		dBFS
f_O = 10MHz	f_{CLOCK} = 50MHz	+25°C		72			*		dBFS
f_O = 5MHz	f_{CLOCK} = 100MHz	+25°C		73			*		dBFS
f_O = 10MHz	f_{CLOCK} = 100MHz	+25°C		72			*		dBFS
f_O = 20MHz	f_{CLOCK} = 100MHz	+25°C		62			*		dBFS
f_O = 50MHz	f_{CLOCK} = 256MHz	+25°C		78			*		dBFS
f_O = 80MHz	f_{CLOCK} = 256MHz	+25°C		72			*		dBFS
Differential Gain Error	NTSC	+25°C		TBD			*		%
Differential Phase Error	NTSC	+25°C		TBD			*		
Output Noise	Bits 1-12 High	+25°C		10.6			*		nV/√Hz
POWER SUPPLY REQUIREMENTS									
Supply Voltage: $-V_S$	Operating	Full	–5.46	–5.2	–4.94	*	*	*	V
Supply Current: $-I_S$	Operating	Full		92	105		*	*	mA
Power Consumption		Full		478	546		*	*	W

NOTE: (1) The DAC601 output may be externally terminated with a 53.6Ω resistor to ground for an equivalent 50Ω nominal output impedance and 0V to –1V output swing.

ORDERING INFORMATION

DAC601 ( ) ( ) ( )

- Basic Model Number
- Package Code
  - P
  - U
  - H
- Performance Grade Code
  - No letter or "B" = –40°C to +85°C
  - S = –55°C TO +125°C
- Reliability Screening
  - Q-Screened (HS Model Only)

ABSOLUTE MAXIMUM RATINGS

$-V_S$	0.3V to –7V
Logic Inputs	0V to –5.5V
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC, 3s)	+260°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC601H, HSQ	28-Pin, 0.3" Wide Hermetic Sidebraze	247
DAC601P, PB	28-Pin, 0.3" Wide Plastic DIP	246
DAC601U, UB	28-Pin, 0.3" Wide SOIC	217

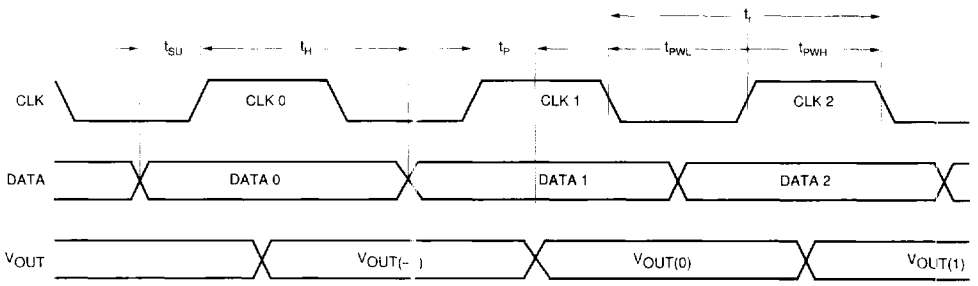
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION
1	B_1	Bit 1, Most Significant Bit
2	B_2	
3	B_3	
4	B_4	
5	B_5	
6	B_6	
7	B_7	
8	B_8	
9	B_9	
10	B_{10}	
11	B_{11}	
12	B_{12}	Bit 12, Least Significant Bit
13	Clock	Data Clocking Input
14	NCLOCK	Complement of Clock Input
15	GND	Ground
16	$-V_S$	Voltage Supply Input (–5.2V)
17	DIVGND	Divider Ground
18	BYP	Bypass DAC
19	LM	Latch Mode[1]
20	NIC	No Internal Connection
21	$-V_S$	Voltage Supply Input (–5.2V)
22	NOUT	Complementary Output
23	OUT	Output
24	REFIN	Reference Input
25	REFOUT	Reference Output
26	GND	Ground
27	$-V_S$	Negative Supply Input (–5.2V)
28	GND	Ground

NOTE: (1) If LM is left floating, the input latches will be in the latch mode. If LM is grounded, the input latches will be in the transparent mode.

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagaton delay. 50% of CLK to 50%V_{OUT} Time not including one pipeline delay		2		ns
t_{SU}	Setup time DATA must be stable before CLK		500		ps
t_H	Hold time DATA must remain stable after CLK		500		ps
t_{PWL}	CLK pulse width low (50% to 50%)		1.25		ns
t_{PWH}	CLK pulse width high (50% to 50%)		1.25		ns
t_r	Data update period	4			ns

NOTE: Timing is specified in the mode with the LATCH mode floating.