

RJK03N2DPA

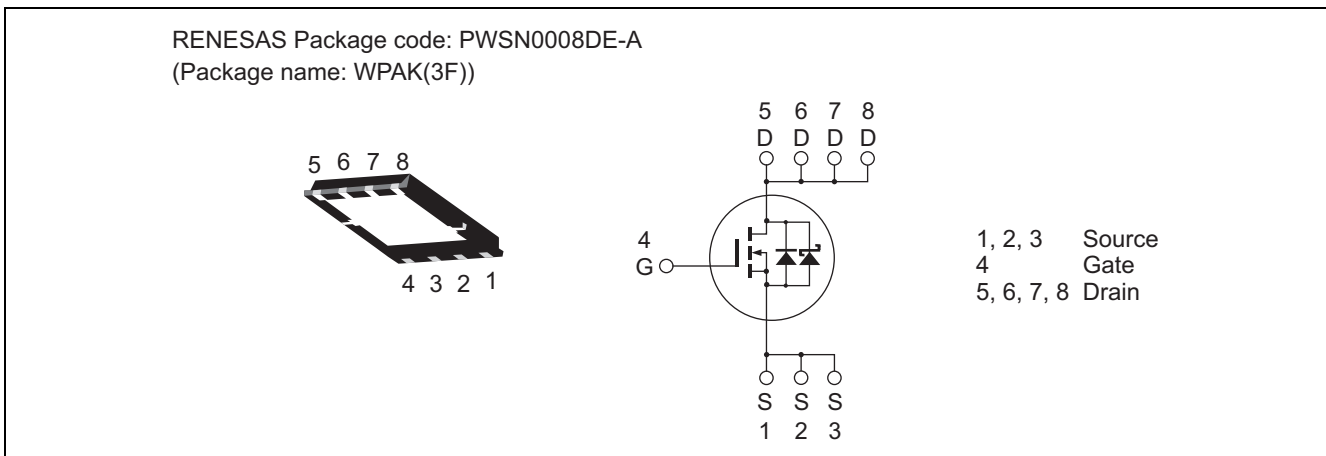
30V, 40A, 4.0mΩmax.
 Built in SBD N Channel Power MOS FET
 High Speed Power Switching

R07DS0783EJ0200
 Rev.2.00
 Feb 12, 2013

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	±12	V
Drain current	I _D	40	A
Drain peak current	I _{D(pulse)} ^{Note1}	160	A
Body-drain diode reverse drain current	I _{DR}	40	A
Avalanche current	I _{AP} ^{Note 2}	14	A
Avalanche energy	E _{AS} ^{Note 2}	19.6	mJ
Channel dissipation	P _{ch} ^{Note3}	35	W
Channel to case thermal impedance	θ _{ch-c} ^{Note3}	3.57	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
 3. T_c = 25°C

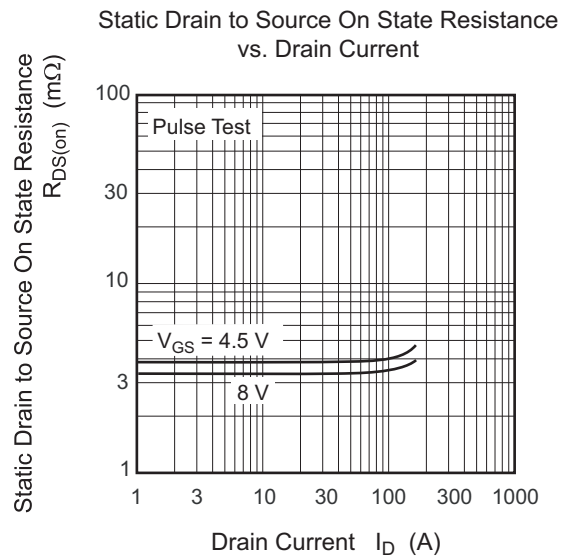
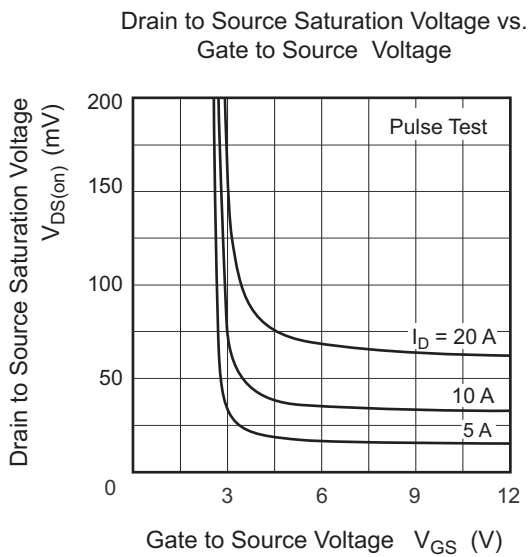
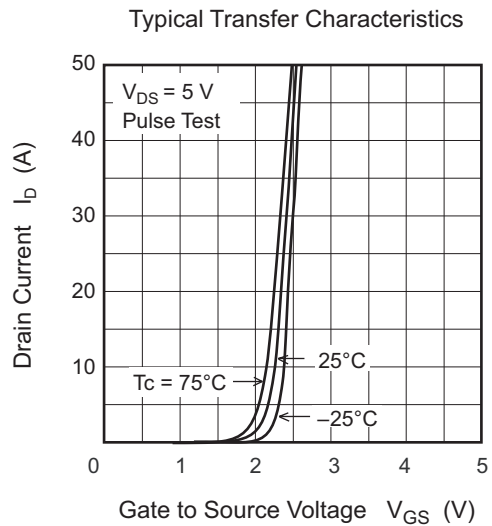
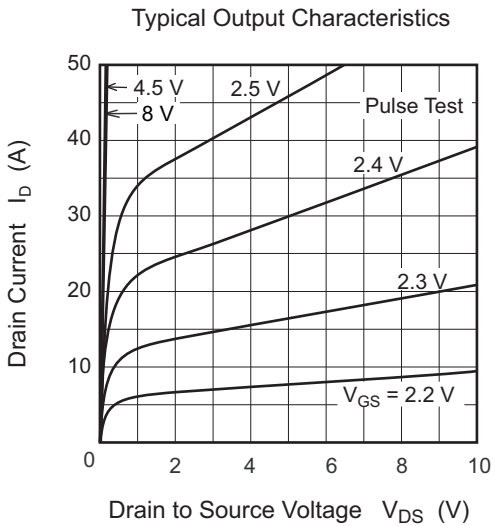
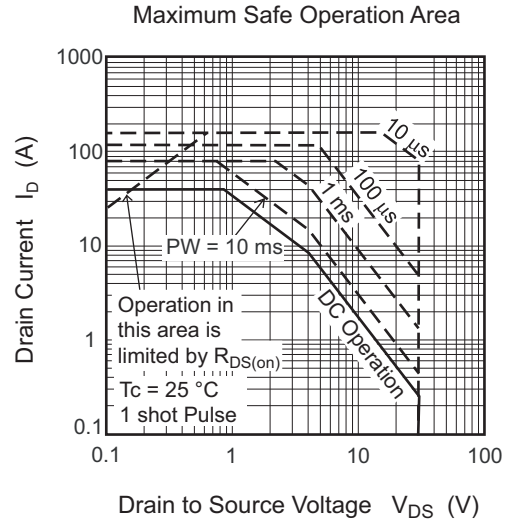
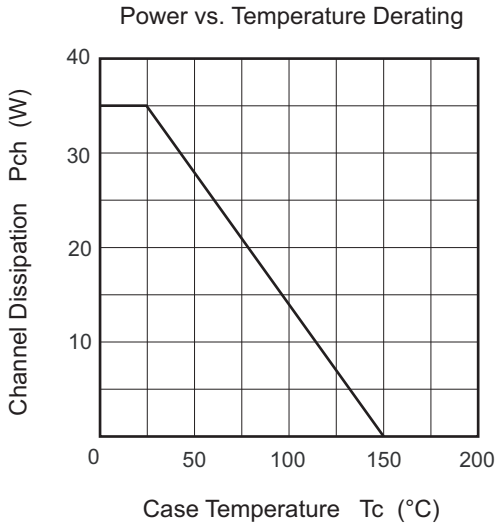
Electrical Characteristics

(Ta = 25°C)

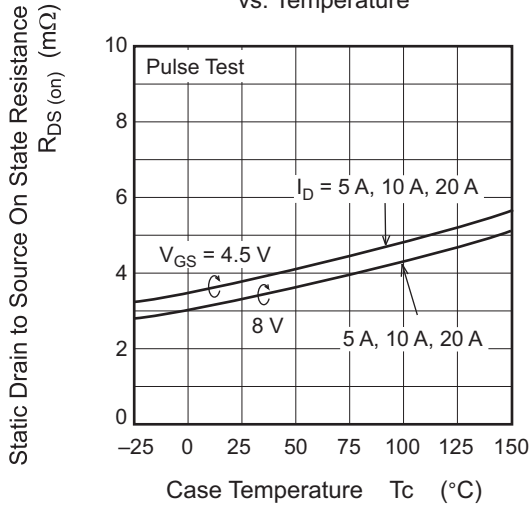
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 12 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.3	4.0	m Ω	$I_D = 20 \text{ A}$, $V_{GS} = 8.0 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	3.8	4.8	m Ω	$I_D = 20 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	105	—	S	$I_D = 20 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	3350	4690	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	405	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	250	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	2.1	4.2	Ω	
Total gate charge	Q_g	—	27.2	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	7.6	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	7.8	—	nC	$I_D = 40 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	6.0	—	ns	$V_{GS} = 8 \text{ V}$, $I_D = 20 \text{ A}$
Rise time	t_r	—	4.4	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	63.3	—	ns	$R_L = 0.5 \Omega$
Fall time	t_f	—	18.7	—	ns	$R_g = 4.7 \Omega$
Body–drain diode forward voltage	V_{DF}	—	0.41	—	V	$I_F = 2 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body–drain diode reverse recovery time	t_{rr}	—	7.4	—	ns	$I_F = 40 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

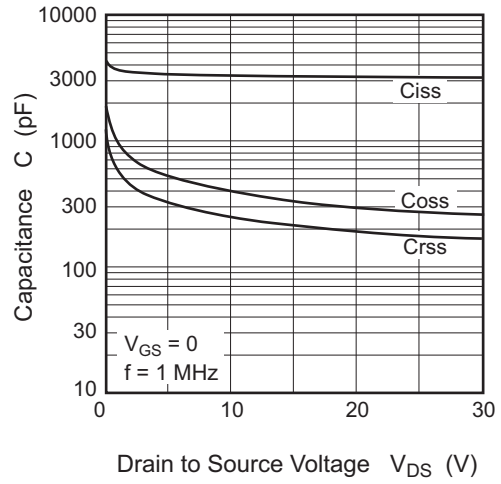
Main Characteristics



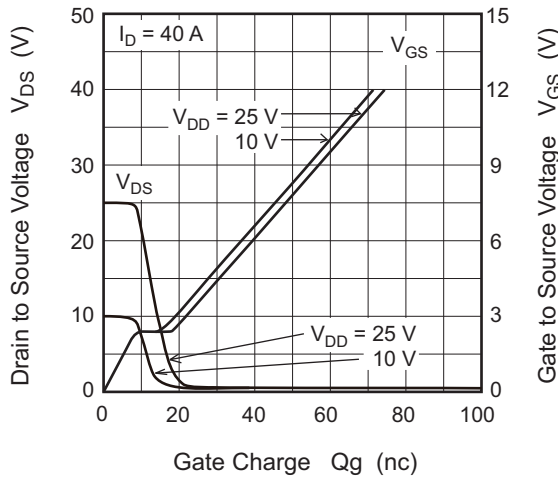
Static Drain to Source On State Resistance vs. Temperature



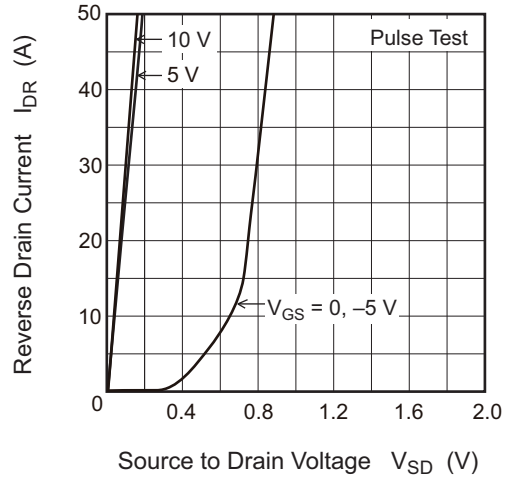
Typical Capacitance vs. Drain to Source Voltage



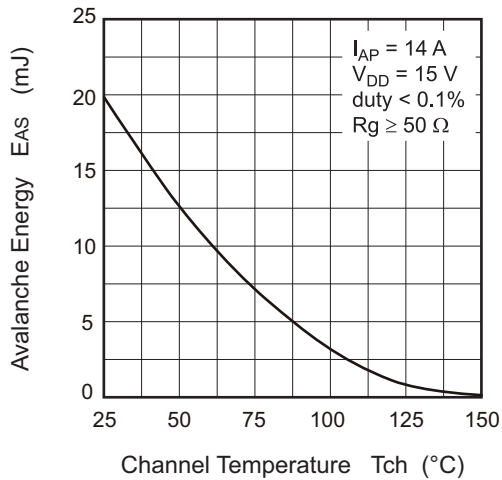
Dynamic Input Characteristics



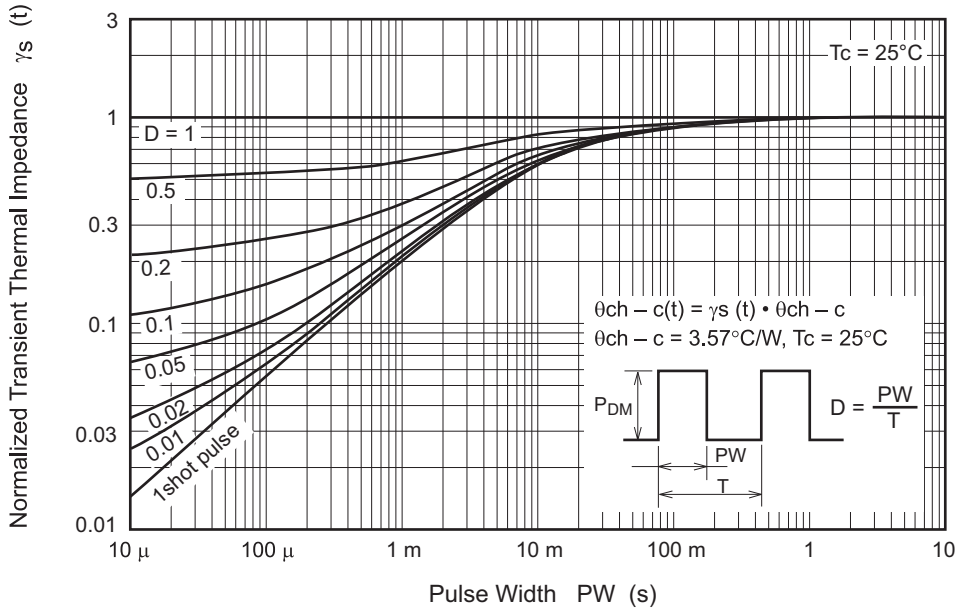
Reverse Drain Current vs. Source to Drain Voltage



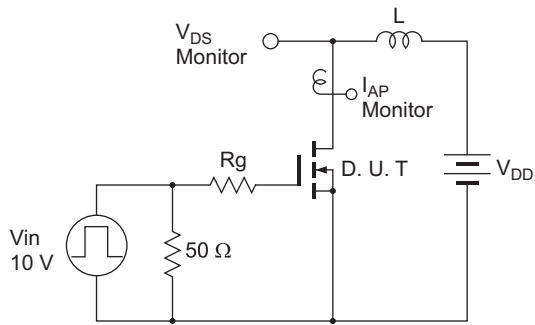
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

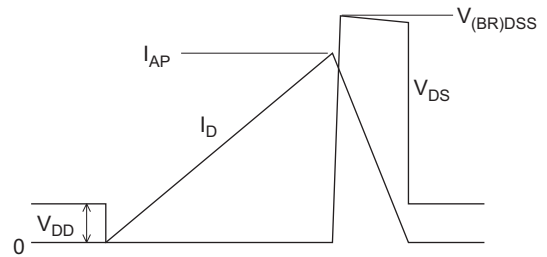


Avalanche Test Circuit

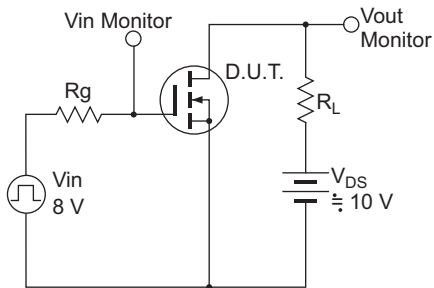


Avalanche Waveform

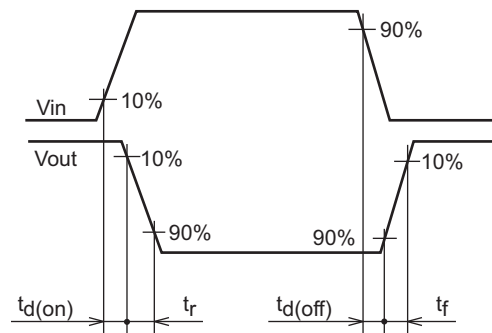
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



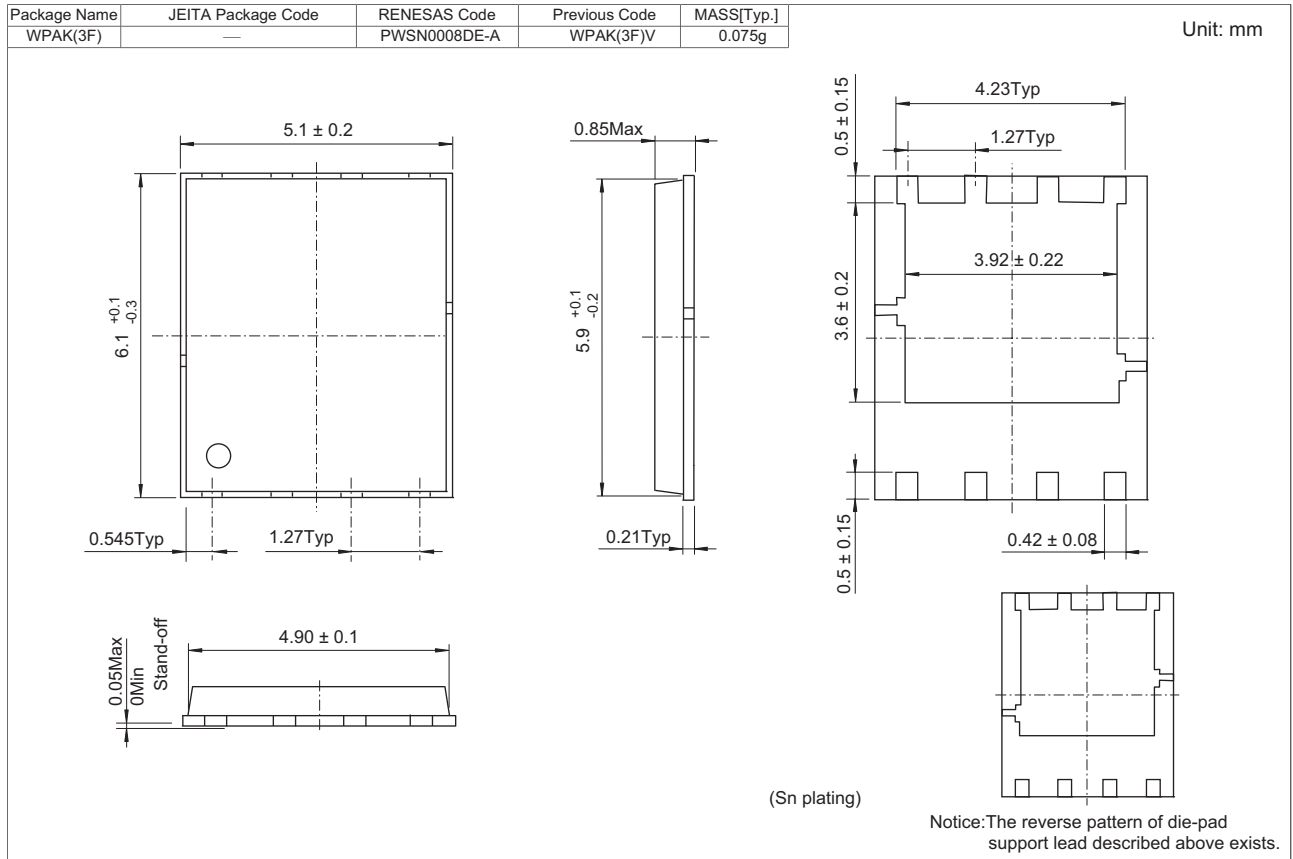
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03N2DPA-00-J5A	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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