

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

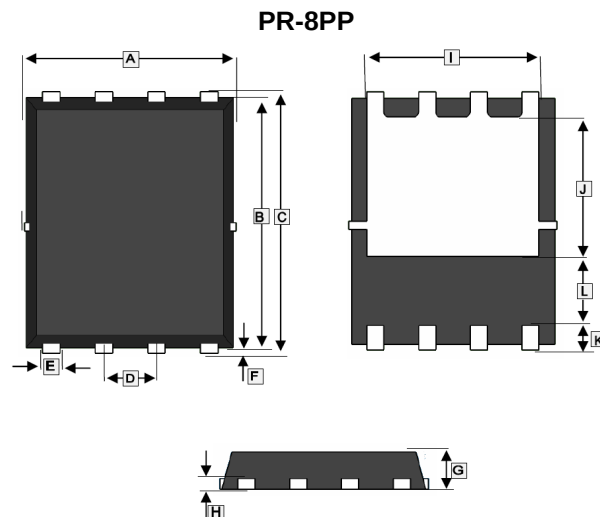
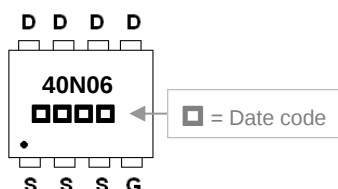
DESCRIPTION

The SPR40N06 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

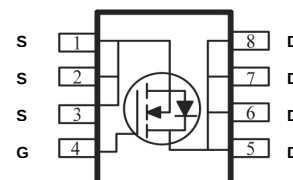
MARKING



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	

PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ @ $V_{GS}=10\text{V}$	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ²	I_{DM}	110	A
Single Pulse Avalanche Energy ³	EAS	50	mJ
Avalanche Current	I_{AS}	30	A
Total Power Dissipation ⁴	P_D	69	W
Operating Junction & Storage Temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Thermal Resistance Junction-Ambient ¹ (Max).	$R_{\theta JA}$	36	$^\circ\text{C} / \text{W}$
Thermal Resistance Junction-Case ¹ (Max).	$R_{\theta JC}$	1.8	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	60	-	-	V	V _{GS} =0, I _D = 250uA
Gate-Threshold Voltage	V _{GS(th)}	2	-	4	V	V _{DS} =V _{GS} , I _D =250uA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current	I _{DSS}	-	-	1	uA	V _{DS} =60V, V _{GS} =0, T _J =25℃
		-	-	5		V _{DS} =60V, V _{GS} =0, T _J =55℃
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	12	mΩ	V _{GS} =10V, I _D =20A
Gate Resistance	R _g	-	-	3.5	Ω	f =1.0MHz
Total Gate Charge	Q _g	-	20	-	nC	I _D =20A V _{DS} =30V V _{GS} =10V
Gate-Source Charge	Q _{gs}	-	5	-		
Gate-Drain Change	Q _{gd}	-	1.8	-		
Turn-on Delay Time ²	T _{d(on)}	-	6	-	nS	V _{DD} =30V V _{GS} =10V R _L =1.5Ω R _G =3Ω
Rise Time	T _r	-	2.5	-		
Turn-off Delay Time	T _{d(off)}	-	25	-		
Fall Time	T _f	-	2.5	-		
Input Capacitance	C _{iss}	-	1543	-	pF	V _{GS} =0 V _{DS} =30V f =1.0MHz
Output Capacitance	C _{oss}	-	165	-		
Reverse Transfer Capacitance	C _{rss}	-	9	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ⁵	EAS	22	-	-	mJ	V _D =25V, L=0.1mH, I _{AS} =20A
Source-Drain Diode						
Diode Forward Voltage ²	V _{SD}	-	-	1.3	V	I _S =20A, V _{GS} =0
Continuous Source Current ^{1,6}	I _S	-	-	40	A	V _D =V _G =0, Force Current
Pulsed Source Current ^{2,6}	I _{SM}	-	-	110	A	
Reverse Recovery Time	T _{rr}	-	18	-	nS	I _F =20A, dI/dt=100A/μS, T _J =25℃
Reverse Recovery Charge	Q _{rr}	-	65	-	nC	

Note:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper , $\leq 10\text{sec}$, $125^\circ\text{C}/\text{W}$ at steady state
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=30\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

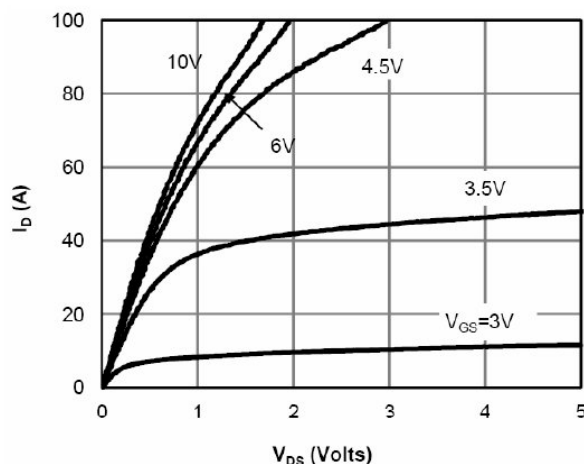


Fig 1. Typical Output Characteristics

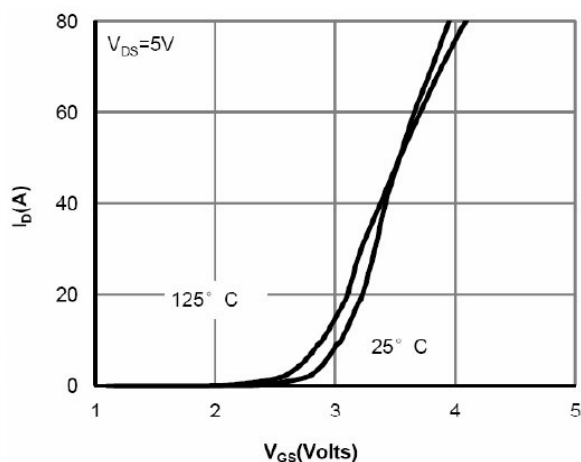


Fig 2. Transfer Characteristics

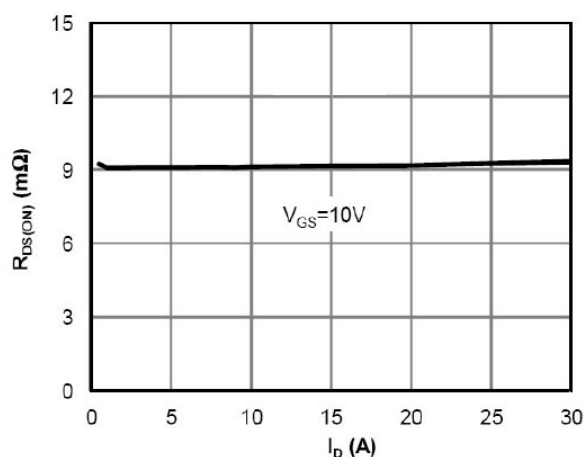
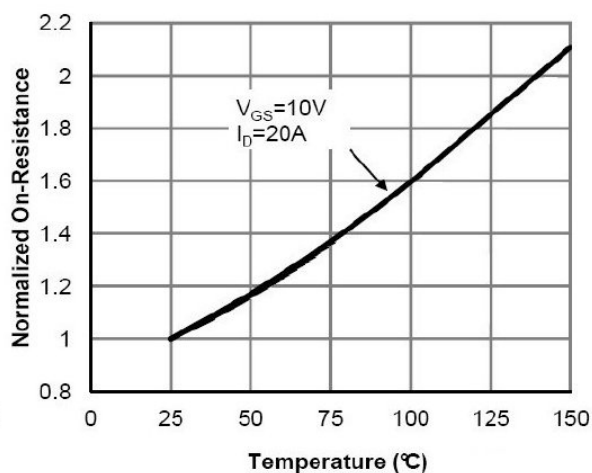
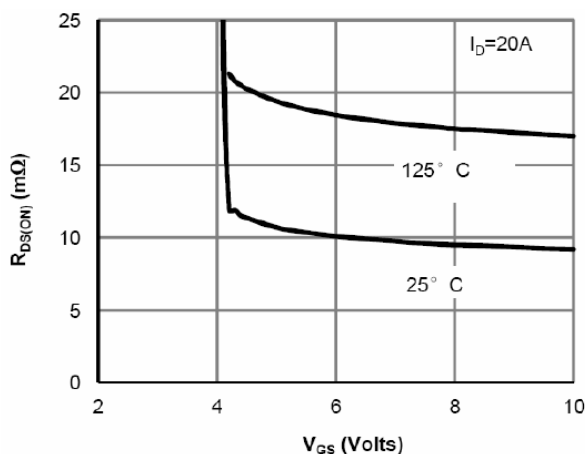


Fig 3. On-Resistance vs. Drain Current



**Fig 4. On-Resistance
vs. Junction Temperature**



**Fig 5. On-Resistance
vs. Gate-Source Voltage**

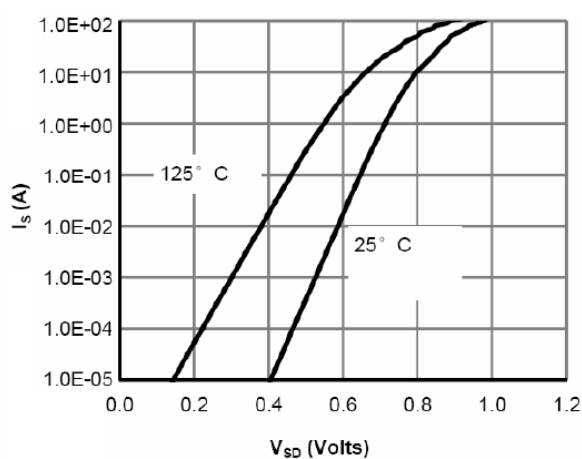


Fig 6. Body Diode Characteristics

CHARACTERISTIC CURVES

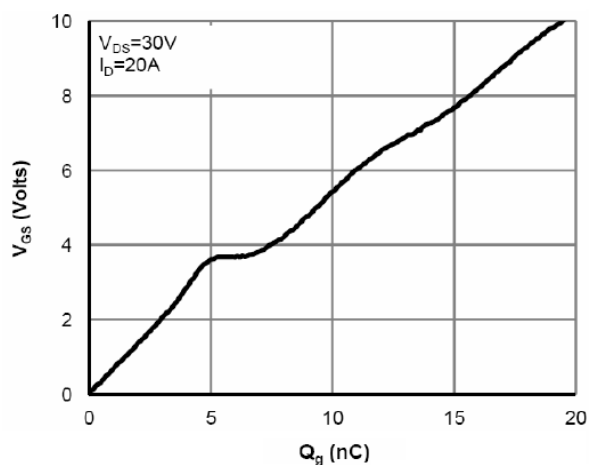


Fig 7. Gate Charge Characteristics

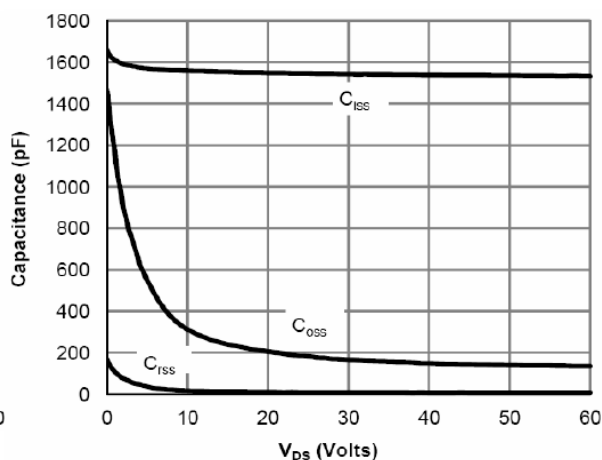


Fig 8. Typical Capacitance Characteristics

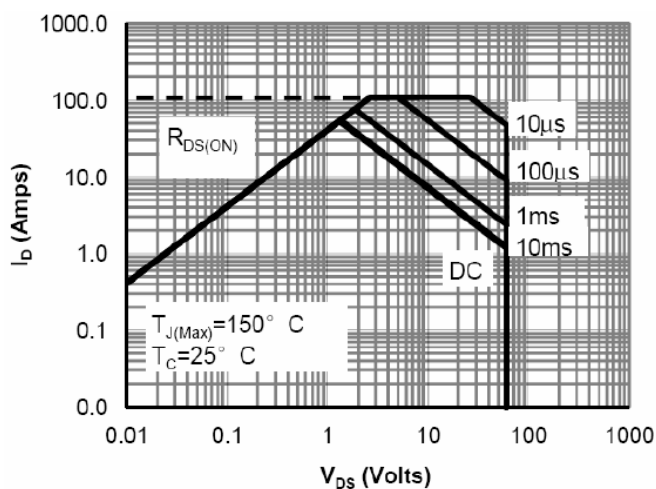


Fig 9. Safe Operating Area

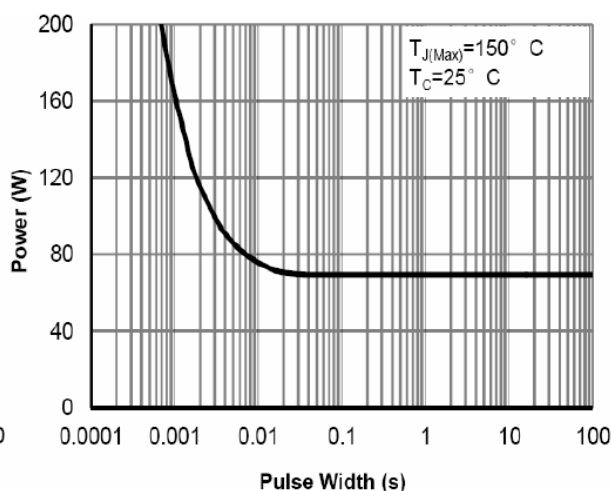


Fig 10. Single Pulse Power

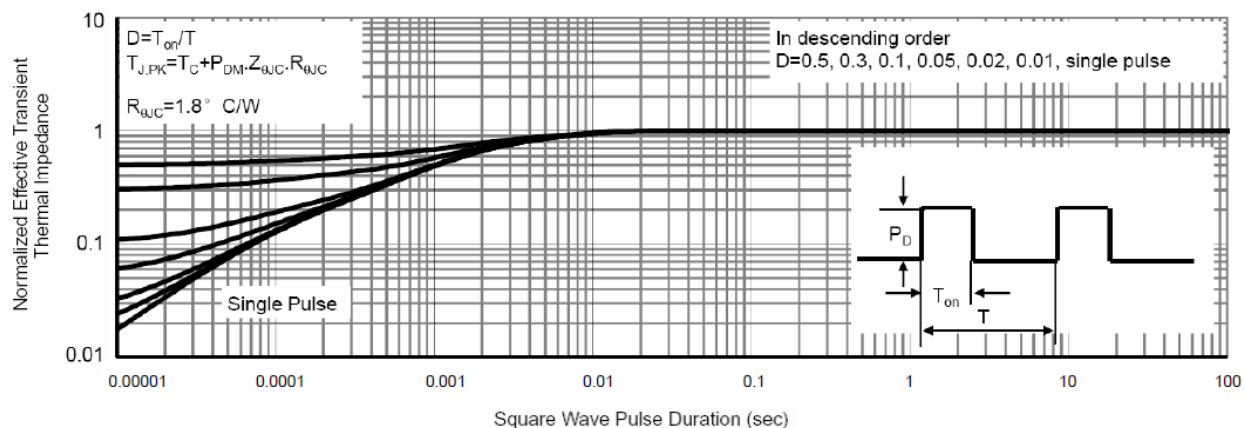


Fig 11. Normalized Maximum Transient Thermal Impedance