XP1050-QJ

2.5 W Power Amplifier
7.1 - 8.5 GHz

Rev. V1

Features

- 15.5 dB Small Signal Gain
- 47 dBm Third Order Intercept Point (OIP3)
- 2 W P1dB
- Integrated Power Detector
- Lead-Free 6 mm 24-lead QFN Package
- RoHS* Compliant and 260°C Reflow Compatible

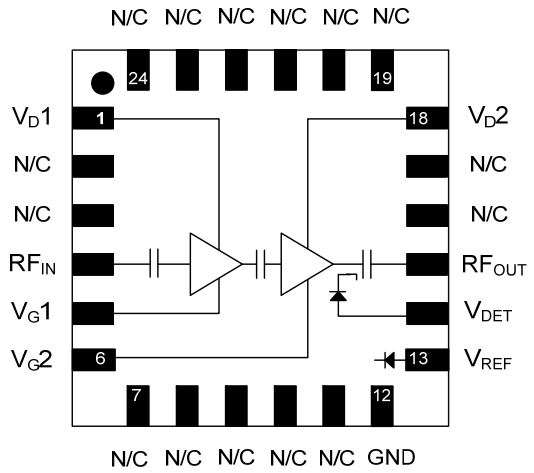
Description

The XP1050-QJ is a packaged linear power amplifier that operates from 7.1-8.5 GHz. The device provides 15.5 dB gain and 47 dBm Output Third Order Intercept Point (OIP3). The packaged amplifier comes in an industry standard, fully molded 6 mm QFN package and is comprised of a two stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part.

The device is specifically designed for use in 7 and 8 GHz Point-to-Point radio applications.

External DC blocks are required. See the reliability note on page 3 for more information.

Functional Schematic



Pin Configuration[3]

Pin No.	Pin Name	Function
1	V_D1	Drain 1 Bias
2-3	N/C	No Connection
4	RF_{IN}	RF Input
5	V_G1	Gate 1 Bias
6	V_G2	Gate 2 Bias
7-11	N/C	No Connection
12	GND	Ground
13	V_{REF}	Power Det. Ref.
14	V_{DET}	Power Detector
15	RF_{OUT}	RF Output
16-17	N/C	No Connection
18	V_D2	Drain 2 Bias
19-24	N/C	No Connection
25[4]	Pad	Ground

3. It is recommended to connect unused pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.

Ordering Information[1,2]

Part Number	Package
XP1050-QJ-0G00	bulk quantity
XP1050-QJ-0G0T	tape and reel
XP1050-QJ-EV1	evaluation module

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: Freq: 7.1 - 8.5 GHz, V_{DD} = 7 V, I_{DQ}[5] = 1350 mA, T_A = +25°C

Parameter	Units	Min.	Typ.	Max.
Gain @ 6 dBm P_{IN}	dB	13.5	15.5	18.5
Input Return Loss	dB	—	10	—
Output Return Loss	dB	—	8	—
P1dB	dBm	—	33	—
Psat[6]	dBm	—	34	—
Output IP3 @ 6 dBm P_{IN}	dBm	43.5	47	
Delta V_{DET} (V_{DET} - V_{REF}) @ 6 dBm P_{IN}, 8.5 GHz	V	—	-0.88	—
Detector Bias Voltage	VDC		5	
Gate Bias Voltage (V_{GG}1,2)	VDC		-0.7	

5. Adjust V_{GG}1 and V_{GG}2 between –1.4 and –0.4 V to achieve specified I_{DQ}. V_{GG}1 and V_{GG}2 should be the same voltage.
6. For reference only. Large signal operation is only recommended under pulsed conditions. Keep output power below P1dB for C.W. operation.

Maximum Operating Ratings[7,8,9]

Parameter	Absolute Maximum
Input Power	+24 dBm
Drain Supply Voltage	+8 Volts
Junction Temperature[10]	+160 °C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.
9. Operating at nominal conditions with $T_J \leq 160°C$ will ensure MTTF > 1 x 10^6 hours.
10. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
    Typical thermal resistance (Θ_{JC}) = 6.8°C/W
    a) For T_C = 25°C,
    T_J = 88°C @ 7 V, 1350 mA, P_{OUT} = 21.5 dBm, P_{IN} = 6 dBm
    b) For T_C = 85°C,
    T_J =149°C @ 7 V, 1350 mA, P_{OUT} = 20 dBm, P_{IN} = 6 dBm

Absolute Maximum Ratings[11,12]

Parameter	Absolute Max.
Supply Gate Voltage	-2.5 V
Supply Current (I_D1)	600 mA
Supply Current (I_D2)	1200 mA
Detector Pin	6 V
Detector Ref Pin	6 V
Continuous Power Dissipation @ 85ºC	11.2 W
Junction Temperature	175ºC

11. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
12. For saturated performance it recommended that the sum of (2*V_{DD} + abs(V_{GG})) <17

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 1A devices.

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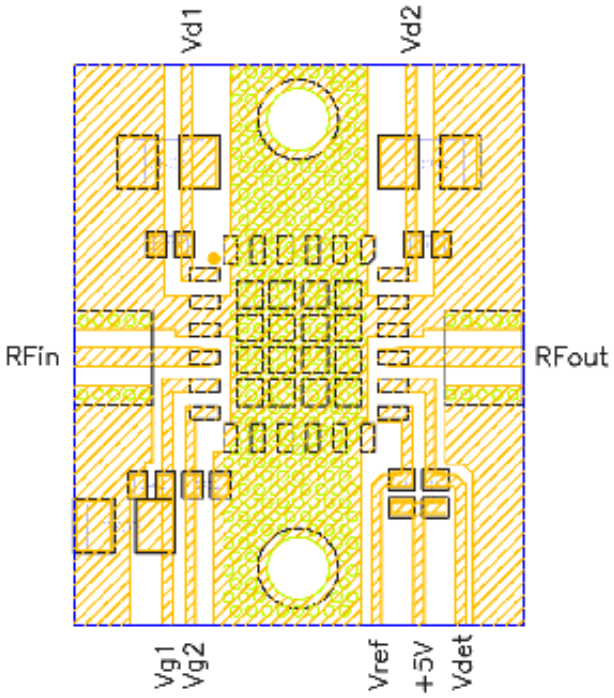
Important Reliability Information:

The input and output capacitors on the die may be damaged through handling and assembly processes. External DC blocks are recommended on the RF input and output lines on the PC board. If the output capacitor shorts due to ESD damage, the part will continue to function with slightly degraded performance. IP3 may decrease by approximately 1.5 dB. If the input capacitor shorts due to ESD damage, the part will continue to function with a slight shift in input return loss. Once shorted, the capacitor should remain shorted for the standard product lifetime. The external DC blocks are needed to maintain the bias point on the part.

Even though the ESD rating using the Human Body Model is Class 1A, it is recommended to treat this part as a Class 0 part. The rate of shorted capacitors due to ESD damage can be in the range of 10%. Shorted capacitors on this part are not subject to the warranty because the part continues to operate reliably with only slightly reduced performance.

Recommended Layout



METAL 1
METAL 2
SOLDERMASK TOP – POSITIVE VIEW
VIAS

MATERIAL: RO4350B, 10 mil.
CAPACITORS: 1µF (0805), 1000 pF (0402)

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App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing Vd1,2 at 7.0V. The nominal drain currents are Id1=450 mA and Id2=900 mA. This ratio of 1:2 between the first and second stage drain currents should be maintained for best linearity. The typical gate voltages needed are -0.9V. The negative gate voltage must be applied prior to applying the positive drain voltage.

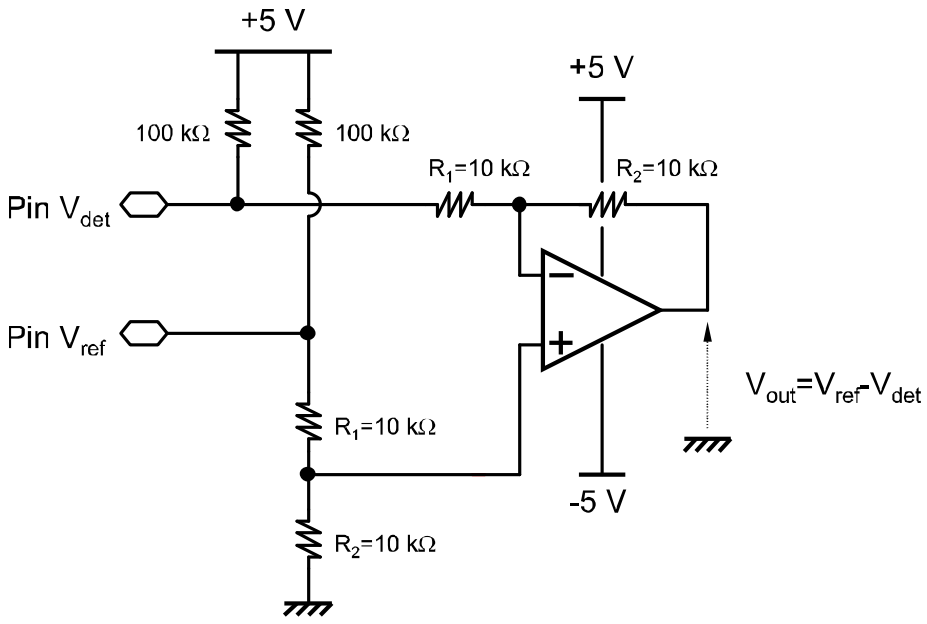
The XP1050-QJ is recommended for linear applications only. Active bias is recommended to keep the currents known and constant, and to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low-power operational amplifier, with a low value resistor in series with the drain supply used to sense the current.

App Note [2] PWB Layout Considerations - It is recommended to provide 1000 pF decoupling capacitors as close as possible to the pins of the device, with additional larger decoupling capacitors further away. For example, in the Recommended Layout, there are 1000 pF 0402 capacitors placed very near the device pins, and 1uF 0805 capacitors placed further away (the gate line shown without a 1uF capacitor (pin 6) would have this capacitor further away on the other side of the screw).

Thermal management of the device is essential. It is recommended that measures such as copper-filled vias under the package, and post/screws for top to bottom heat transfer are used (see Recommended Layout shown below). Adequate heat-sinking under the PWB is necessary in maintaining the package base at a safe operating temperature.

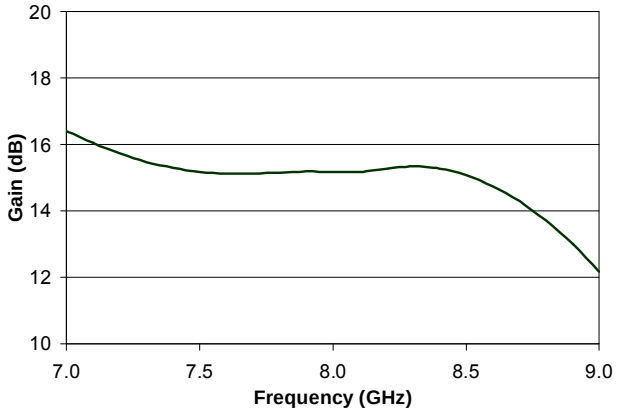
App Note [3] Power Detector - As shown in the schematic at right, the power detector is implemented by providing +5V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

Application Schematic

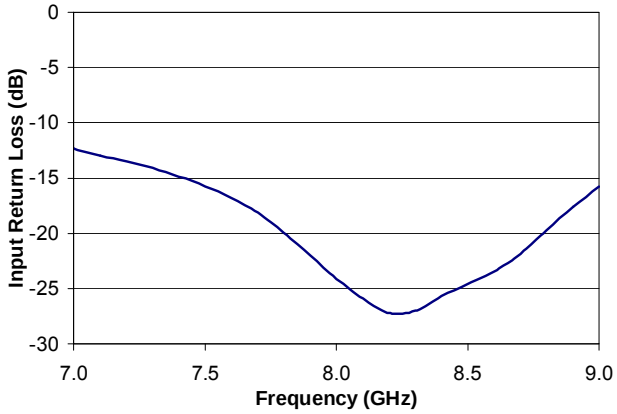


Typical Performance Curves: V_{DD} = 7 V, I_{DQ} = 1350 mA

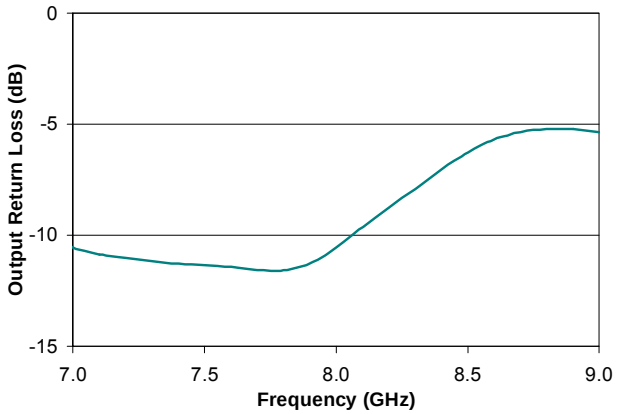
Gain vs. Frequency, +25°C



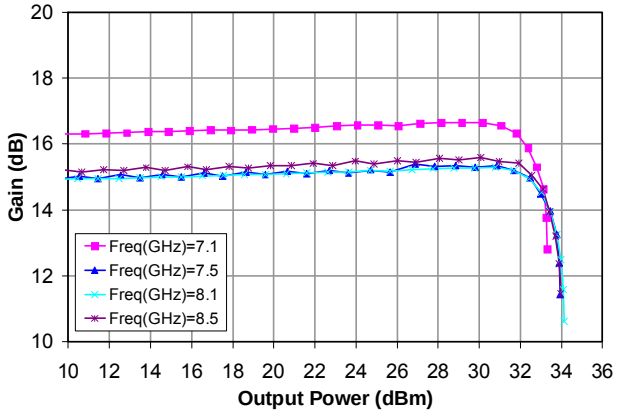
Input Return Loss vs. Frequency, +25°C



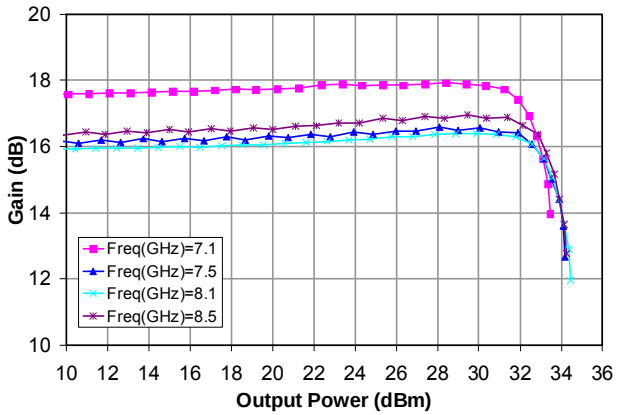
Output Return Loss vs. Frequency, +25°C



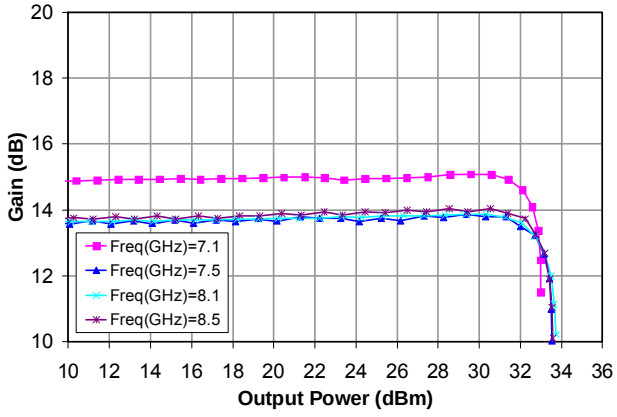
Gain vs. Output Power, +25°C



Gain vs. Output Power, -40°C



Gain vs. Output Power, +85°C



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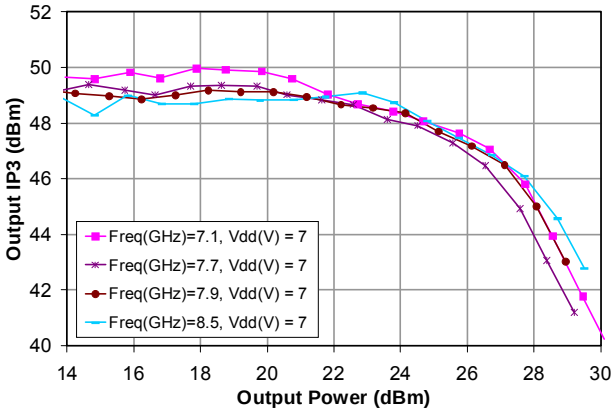
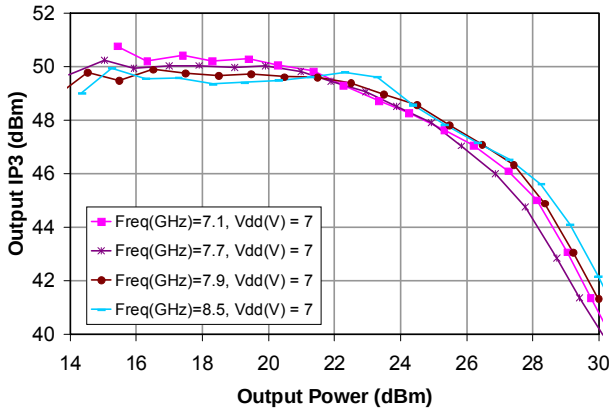
Typical Performance Curves: V_{DD} = 7 V, I_{DQ} = 1350 mA

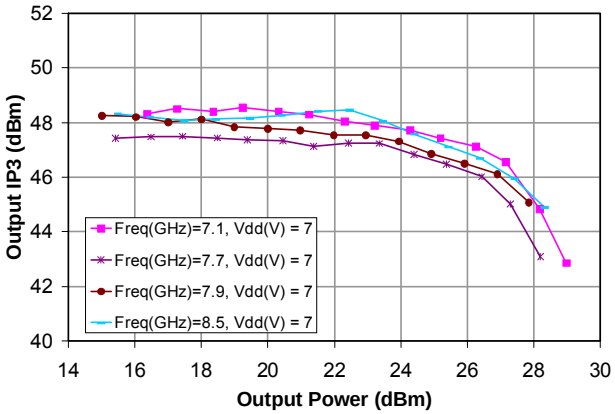
Output IP3 vs. Output Power, +25°C



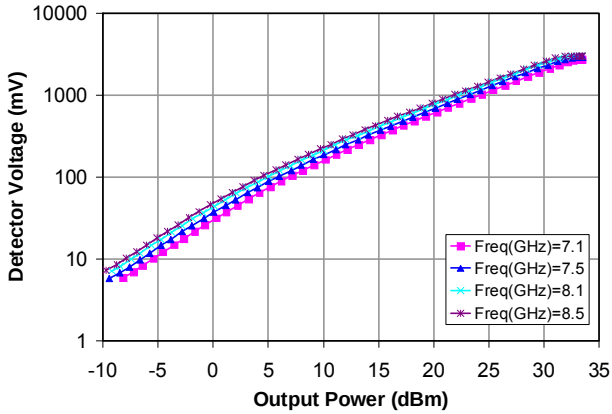
Output IP3 vs. Output Power, -40°C



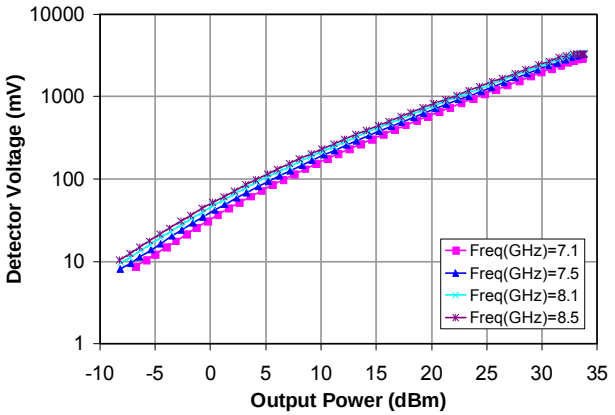
Output IP3 vs. Output Power, +85°C



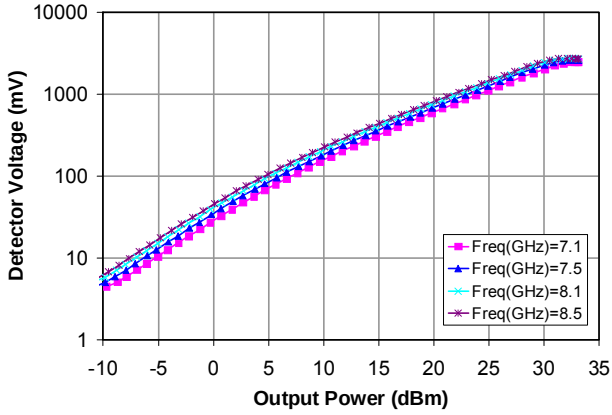
Detector Voltage (V_{REF} - V_{DET}) vs. Output Power, +25°C



Detector Voltage (V_{REF} - V_{DET}) vs. Output Power, -40°C



Detector Voltage (V_{REF} - V_{DET}) vs. Output Power, +85°C



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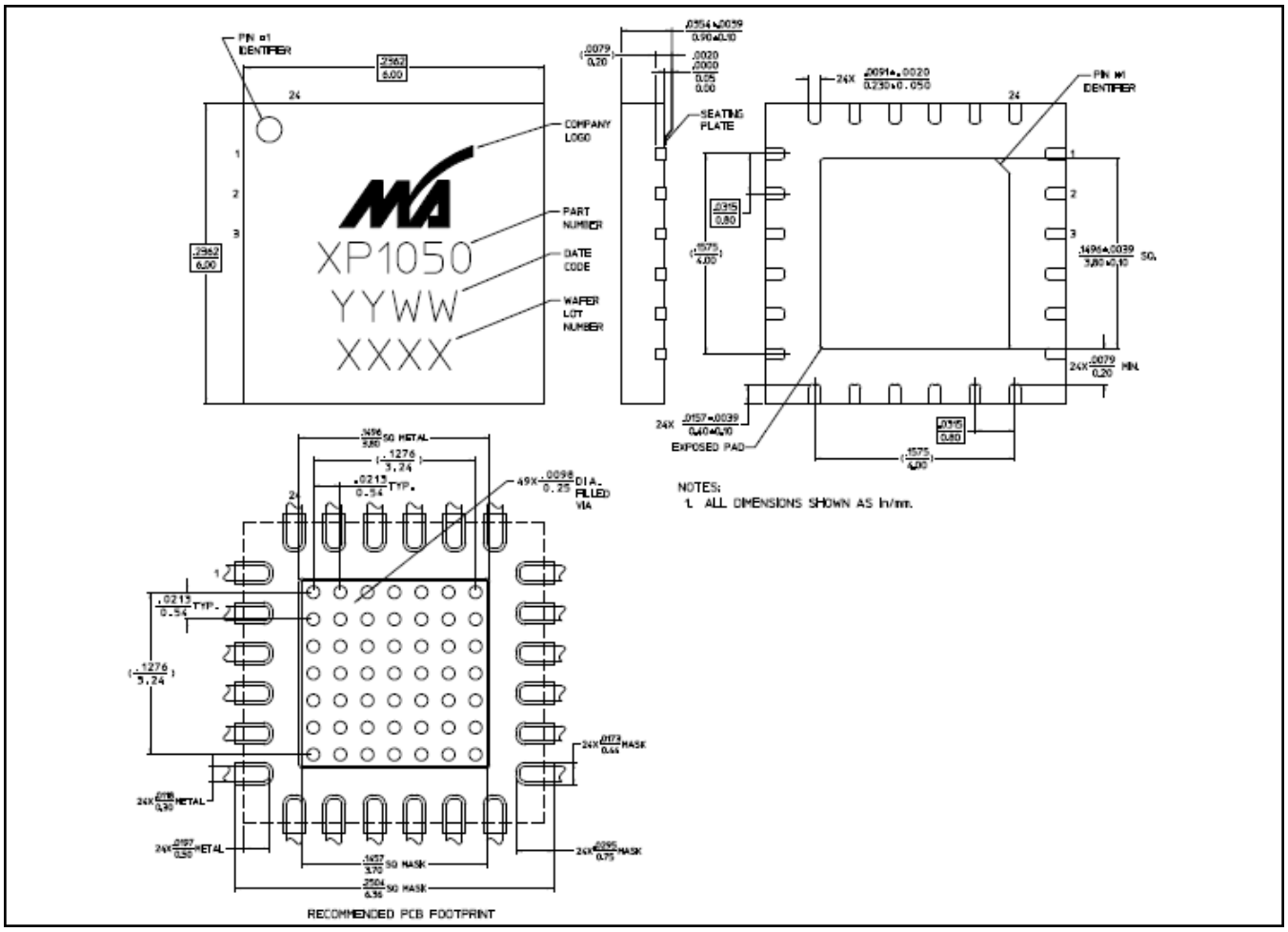
Lead-Free 6 mm 24-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is 100% matte tin over copper.

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