

AN8388S, AN8388SR

4 Ch. Linear Driver IC for CD Player

Overview

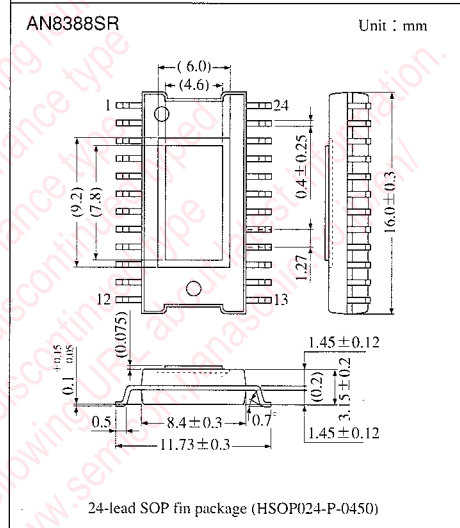
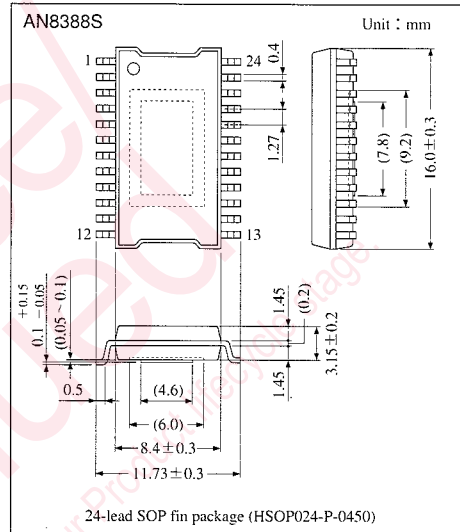
The AN8388S and AN8388SR employ 4 ch. H-bridge system that they are suitable for driving motor or actuator of CD player. Also they employ the surface mounting type package superior in radiation characteristics.

Features

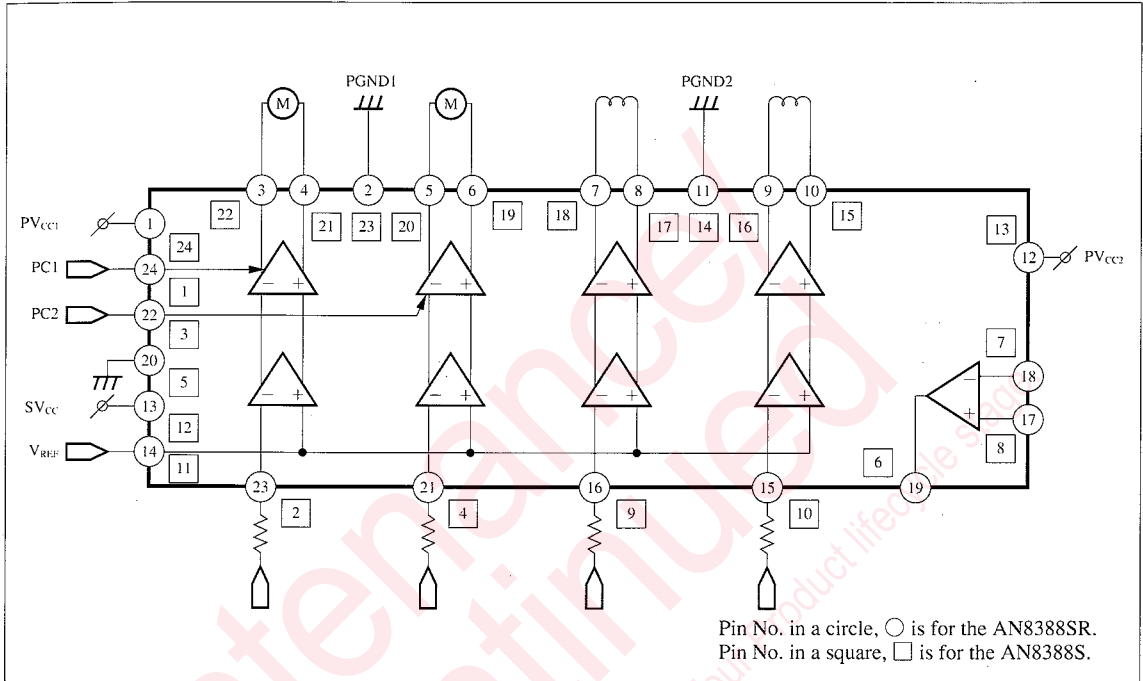
- Wide output D-range is available regardless of reference supply on the system.
- 4 ch. BTL Driver built-in. Particularly suitable for driver of actuator or motor of about $8\ \Omega$ load.
- PC (Power Control) feature built-in
- Thermal shut down circuit (with hysteresis) built-in
- Control for proper heat of IC by separating the power supplies for signal line and output line.

Application

- CD player, CD-ROM
- For drive of motor



■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	SV _{CC}	16	V
Supply Current	I _{CC}	—	mA
Power Dissipation ^{Note)}	P _D	2083	mW
Operating Ambient Temperature	T _{opr}	-30 ~ +85	°C
Storage Temperature	T _{stg}	-55 ~ +150	°C

Note) For surface mounting on 50×50×1.2mm glass epoxy board

■ Recommended Operating Range (Ta = 25°C)

Parameter	Symbol	Range
Operating Supply Voltage Range	V _{CC}	4.5V ~ 15V
	PV _{CC}	

■ Electrical Characteristics (Ta=25°C±2°C)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Total Circuit Current	I _{tot}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V	10	25	40	mA
Reset Circuit						
Reset Operation Release Supply Voltage	V _{RST}	R _L =8Ω	—	—	4.5	V
Driver 1						
Input Offset Voltage	V _{IOF1}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-10	—	10	mV
Output Offset Voltage	V _{OOF1}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-60	—	60	mV
Gain (+)	G ₁₊	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	14	17	21	dB
(+) (-) Relative Gain	ΔG ₁	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-1.7	0	1.7	dB
Limit Voltage (+)	V _{L1+}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	4.4	4.9	5.4	V
Limit Voltage (-) ^{Note 1)}	V _{L1-}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	0.93	1.0	1.07	—
Dead Zone Width	V _{DZ1}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-10	—	20	mV
PC Operation Threshold H	V _{PC1H}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	3	—	—	V
Drivers 2 to 4						
Input Offset Voltage	V _{IOF}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-10	—	10	mV
Output Offset Voltage	V _{OOF}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-60	—	60	mV
Gain (+)	G ₊	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	14	17	21	dB
(+) (-) Relative Gain	ΔG	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	0.93	1.0	1.07	—
Limit Voltage (+) ^{Note 2)}	V _{L+}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	0.93	1.0	1.07	—
Limit Voltage (-) ^{Note 1)}	V _{L-}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	0.93	1.0	1.07	—
Dead Zone Width	V _{DZ}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	-10	—	20	mV
PC Operation Threshold H	V _{PCH}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V R _L =8Ω, R _{IN} =10kΩ	3	—	—	V
Operational amplifier Offset Voltage	V _{OF-OP}	PV _{CC1} =PV _{CC2} =SV _{CC} =8V	-40	—	40	mV
Heat Protection Circuit						
Operation Temperature Equilibrium Value ^{Note 3)}	T _{THD}		(—)	(160)	(—)	°C
Operation Temperature Hysteresis Width ^{Note 3)}	ΔT _{THD}		(—)	(65)	(—)	°C

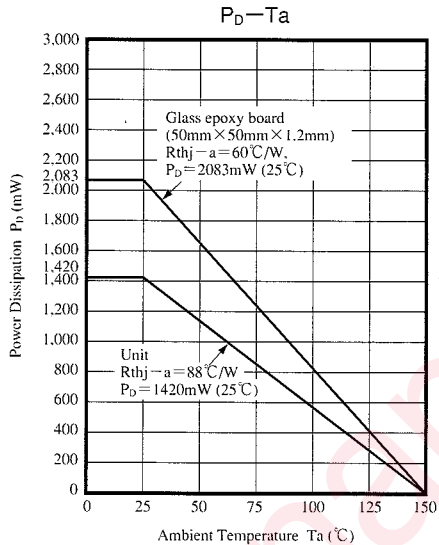
Note1) Relative voltage ratio of limit voltage (-) to limit voltage (+) for each channel.

Note2) Relative voltage ratio of limit voltage (+) of Drivers 2 to 4 to limit voltage (+) of Driver 1

Note3) Characteristic value in parentheses is a reference value for design but not a guaranteed value.

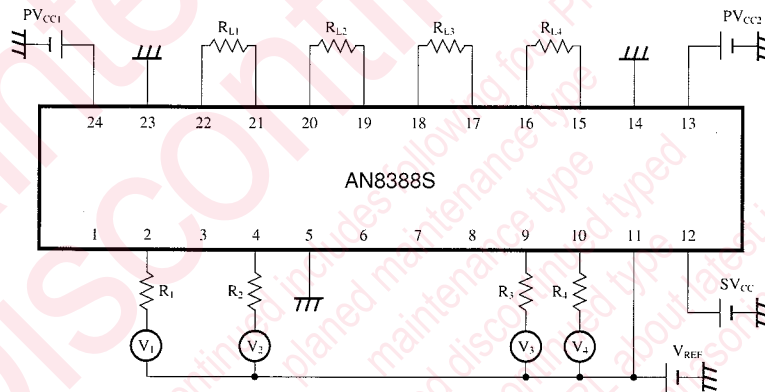


■ Characteristic Curve



■ Cautions for use

• AN8388S



When the AN8388S is used, take into account the following cautions and follow the power dissipation characteristic curve.

- (1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin⑳.

$$I_{P1} = \frac{|V_{22-21}|}{R_{L1}} + \frac{|V_{20-19}|}{R_{L2}}$$

- (2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin⑬.

$$I_{P2} = \frac{|V_{18-17}|}{R_{L3}} + \frac{|V_{16-15}|}{R_{L4}}$$

- (3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1} , R_{L2} , R_{L3} , and R_{L4} is as follows:

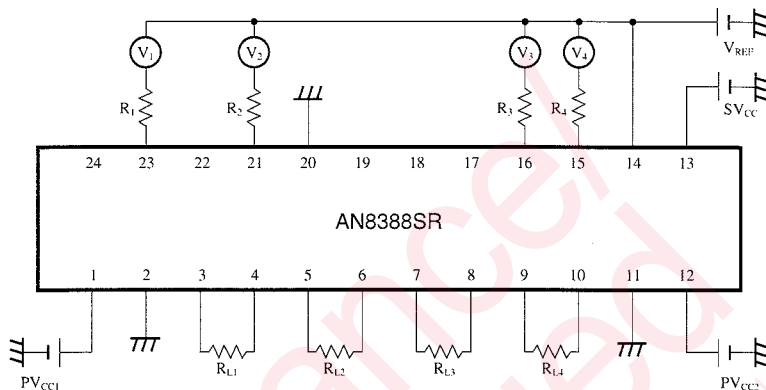
$$\Delta P_d = (PV_{CC1} - |V_{22-21}|) \times \frac{|V_{22-21}|}{R_{L1}} + (PV_{CC1} - |V_{20-19}|) \times \frac{|V_{20-19}|}{R_{L2}} \\ + (PV_{CC2} - |V_{18-17}|) \times \frac{|V_{18-17}|}{R_{L3}} + (PV_{CC2} - |V_{16-15}|) \times \frac{|V_{16-15}|}{R_{L4}}$$

- (4) Dissipation increase (ΔP_s) inside the IC (signal block supplied from Pin⑫) caused by loads R_{L1} , R_{L2} , R_{L3} , and R_{L4} is almost as follows:

$$\Delta P_s = V_{CC} \times \left(\frac{|V_1|}{R_1} + \frac{|V_2|}{R_2} + \frac{|V_3|}{R_3} + \frac{|V_4|}{R_4} \right) \times 10 + \frac{V_{CC}}{100} \times \left(\frac{|V_{22-21}|}{R_{L1}} + \frac{|V_{20-19}|}{R_{L2}} + \frac{|V_{18-17}|}{R_{L3}} + \frac{|V_{16-15}|}{R_{L4}} \right)$$

- (5) Dissipation increase inside the IC during driver running is $\Delta P_d + \Delta P_s$.

■ Cautions for use
 • AN8388SR



When the AN8388SR is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin①.

$$I_{P1} = \frac{|V_{3-4}|}{R_{L1}} + \frac{|V_{5-6}|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin②.

$$I_{P2} = \frac{|V_{7-8}|}{R_{L3}} + \frac{|V_{9-10}|}{R_{L4}}$$

(3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1} , R_{L2} , R_{L3} and R_{L4} is as follows:

$$\Delta P_d = (PV_{CC1} - |V_{3-4}|) \times \frac{|V_{3-4}|}{R_{L1}} + (PV_{CC1} - |V_{5-6}|) \times \frac{|V_{5-6}|}{R_{L2}} + (PV_{CC2} - |V_{7-8}|) \times \frac{|V_{7-8}|}{R_{L3}} + (PV_{CC2} - |V_{9-10}|) \times \frac{|V_{9-10}|}{R_{L4}}$$

(4) Dissipation increase (ΔP_s) inside the IC (signal block supplied from Pin③) caused by loads R_{L1} , R_{L2} , R_{L3} and R_{L4} is also as follows:

$$\Delta P_s = V_{CC} \times \left(\frac{|V_1|}{R_1} + \frac{|V_2|}{R_2} + \frac{|V_3|}{R_3} + \frac{|V_4|}{R_4} \right) \times 10 + \frac{V_{CC}}{100} \times \left(\frac{|V_{3-4}|}{R_{L1}} + \frac{|V_{5-6}|}{R_{L2}} + \frac{|V_{7-8}|}{R_{L3}} + \frac{|V_{9-10}|}{R_{L4}} \right)$$

(5) Dissipation increase inside the IC during driver running is, $\Delta P_d + \Delta P_s$.



Pin Description

Pin No.		Symbol	I/O	DC voltage (V _{CC} /8V)	Pin Description	Equivalent Circuit
AN8388S	AN8388SR					
1	24	PC1	I	0V	PC (power cut) input pin controlling the output of ⑳ and ㉑	
3	22	PC2	I	0V	PC (power cut) input pin controlling the output of ⑲ and ㉑	
2	23	IN1	I	2.5V	Error input pin of Driver 1	
4	21	IN2	I	2.5V	Error input pin of Driver 2	
9	16	IN3	I	2.5V	Error input pin of Driver 3	
10	15	IN4	I	2.5V	Error input pin of Driver 4	
7	18	IN-	I	- V	Reverse rotation input pin of operational amplifier	
8	17	IN+	I	- V	Normal rotation input pin of operational amplifier	
12	13	SV _{CC}	I	8V	SV _{CC} pin for control circuit of driver, not connected to power V _{CC} pin.	
5	20	SGND	I	0V	SGND pin for control circuit of driver	

Note) The pin numbers shown in the equivalent circuit diagram are only for the AN8388S. For the AN8388SR, they must be replaced.

Pin Description (Cont.)

Pin No.		Symbol	I/O	DC voltage (V _{CC} /8V)	Pin Description	Equivalent Circuit
AN8388S	AN8388SR					
6	19	OPO	O	— V	Operational amplifier output pin	
11	14	V _{REF}	I	2.5V	V _{REF} input pin	
22	3	D1-	O	0V	Reverse rotation output pin of Driver 1	
21	4	D1+	O	0V	Normal rotation output pin of Driver 1	
20	5	D2-	O	0V	Reverse rotation output pin of Driver 2	
19	6	D2+	O	0V	Normal rotation output pin of Driver 2	
18	7	D3-	O	0V	Reverse rotation output pin of Driver 3	
17	8	D3+	O	0V	Normal rotation output pin of Driver 3	
16	9	D4-	O	0V	Reverse rotation output pin of Driver 4	
15	10	D4+	O	0V	Normal rotation output pin of Driver 4	
24	1	PV _{CC1}	I	8V	Power V _{CC} pin, supplying the current flowing for output power transistors of 19, 20, 21, and 22	
13	12	PV _{CC2}	I	8V	Power V _{CC} pin, supplying the current flowing for output power transistors of 15, 16, 17, and 18	
23	2	PGND1	I	0V	PGND pin for output transistors of 19, 20, 21, and 22	
14	11	PGND2	I	0V	PGND pin for output transistors of 15, 16, 17, and 18	

Note) The pin numbers shown in the equivalent circuit diagram are only for the AN8388S. For the AN8388SR, they must be replaced.

ICs for CD/CD-ROM

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