RJK1052DPB

100V, 20A, 20mΩ max.
Silicon N Channel Power MOS FET
Power Switching

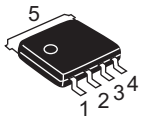
R07DS0083EJ0200
Rev.2.00
Apr 11, 2013

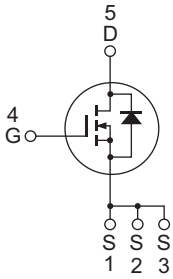
Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 15 mΩ typ. (at V_{GS} = 10 V)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)





1, 2, 3	Source
4	Gate
5	Drain

Application

- Switching Mode Power Supply

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ Note1	80	A
Body-drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP} Note 2	10	A
Avalanche energy	E_{AS} Note 2	10	mJ
Channel dissipation	Pch Note3	55	W
Channel to Case Thermal Resistance	θch-C	2.27	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

This product is for the low voltage drive (≤ 10V).
If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ($V_{GS(off)}$) which characteristics has been improved.

Electrical Characteristics

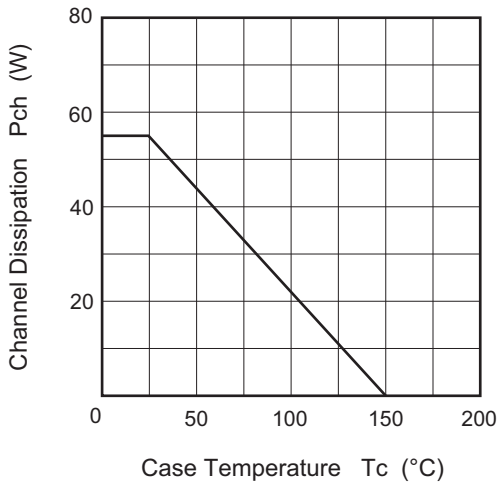
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	mΩ	I_D = 10 A, V_{GS} = 10 V [Note4]
	$R_{DS(on)}$	—	16	22	mΩ	I_D = 10 A, V_{GS} = 4.5 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	—	42	—	S	I_D = 10 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	4160	—	pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance	Coss	—	354	—	pF	
Reverse transfer capacitance	Crss	—	136	—	pF	
Gate Resistance	Rg	—	0.4	—	Ω	
Total gate charge	Qg	—	29	—	nC	V_{DD} = 50 V, V_{GS} = 4.5 V, I_D = 20 A
Gate to source charge	Qgs	—	12	—	nC	
Gate to drain charge	Qgd	—	9.2	—	nC	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	V_{GS} = 10 V, I_D = 10 A, V_{DD} ≅ 30 V, R_L = 3 Ω, Rg = 4.7 Ω
Rise time	t_r	—	5.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	54	—	ns	
Fall time	t_f	—	6.8	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.83	1.1	V	I_F = 20 A, V_{GS} = 0 V [Note4]
Body–drain diode reverse recovery time	t_{rr}	—	46	—	ns	I_F = 20 A, V_{GS} = 0 V di_F/ dt = 100 A/ μs

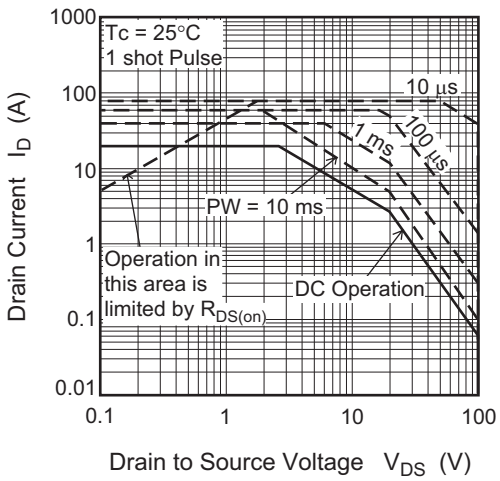
Notes: 4. Pulse test

Main Characteristics

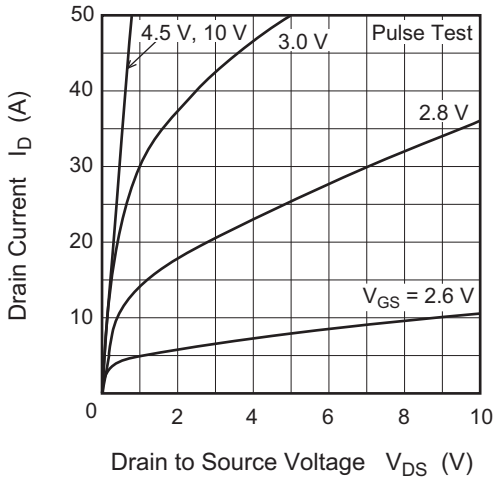
Power vs. Temperature Derating



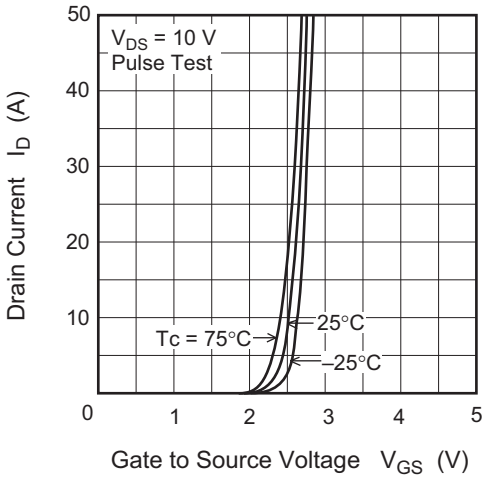
Maximum Safe Operation Area



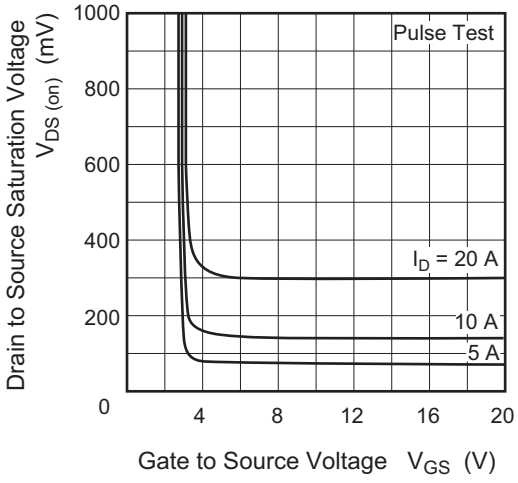
Typical Output Characteristics



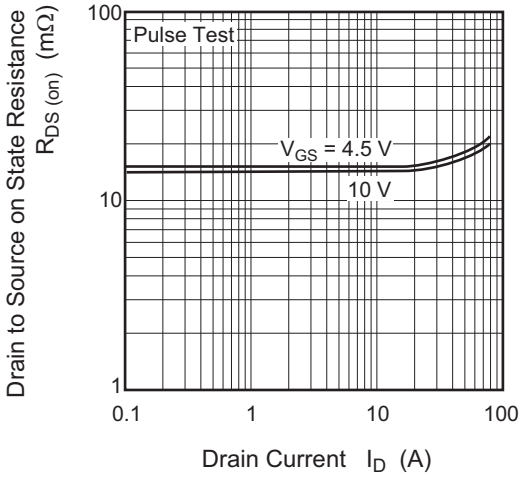
Typical Transfer Characteristics



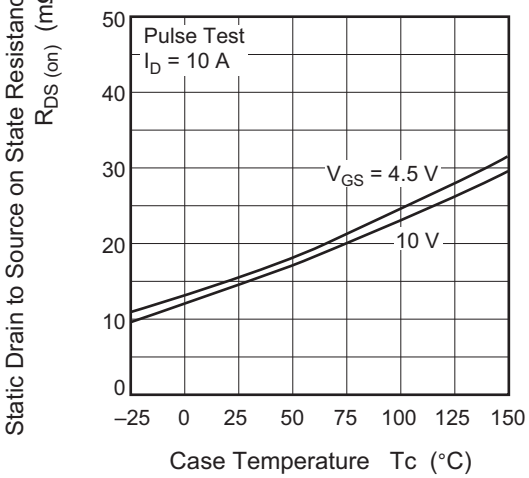
Drain to Source Saturation Voltage vs. Gate to Source Voltage



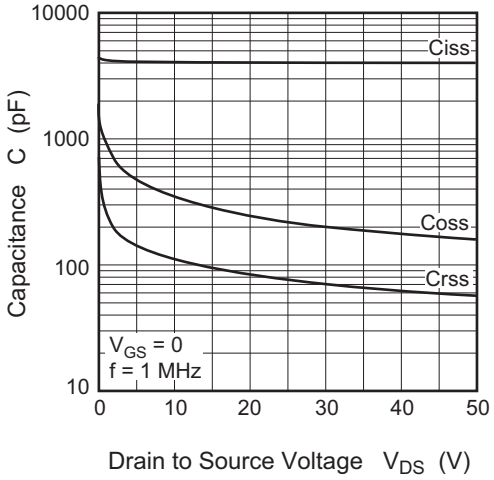
Static Drain to Source on State Resistance vs. Drain Current



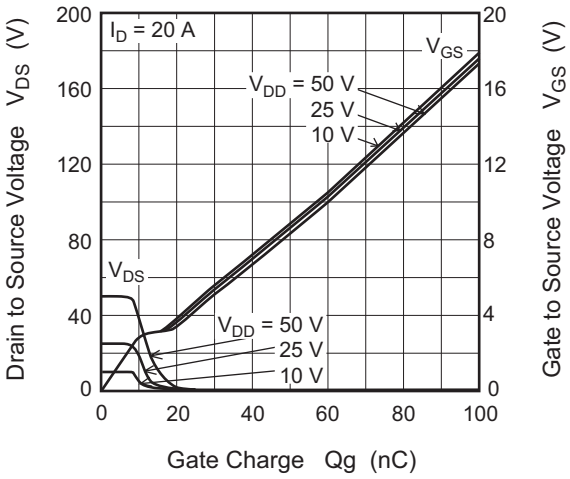
Static Drain to Source on State Resistance vs. Temperature



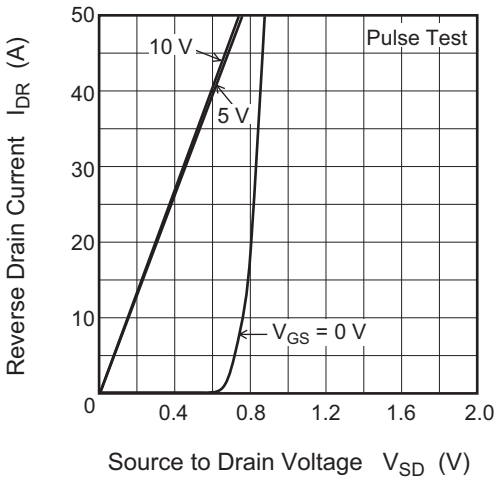
Typical Capacitance vs. Drain to Source Voltage



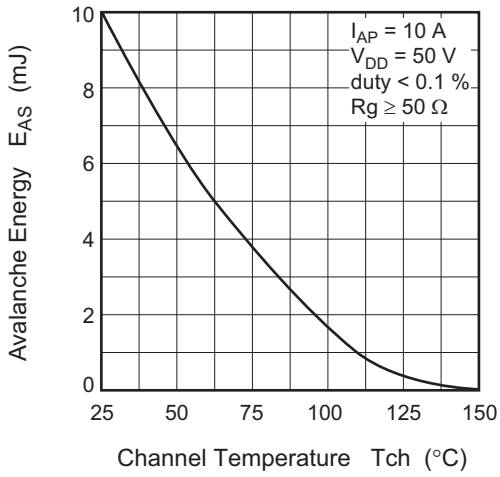
Dynamic Input Characteristics



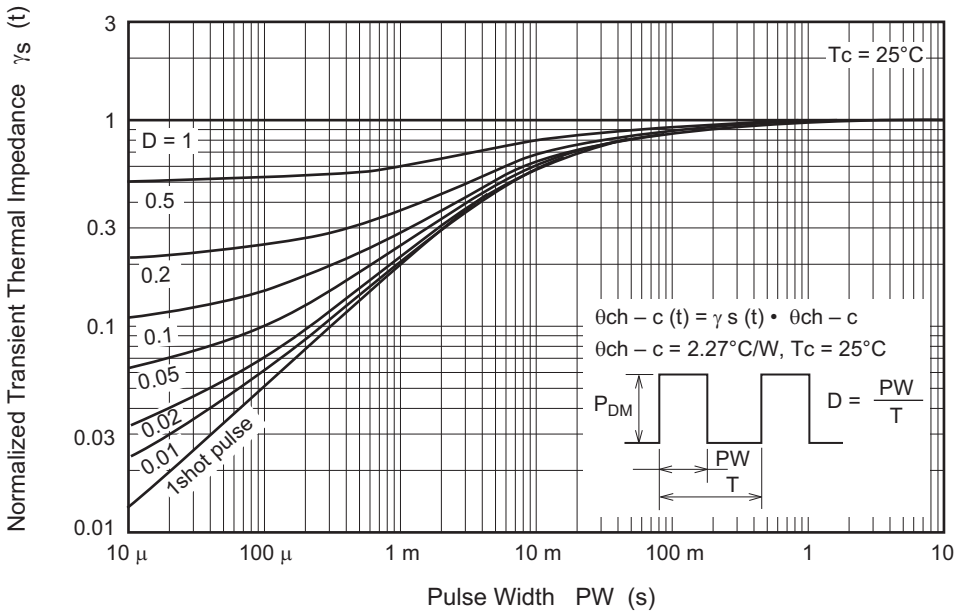
Reverse Drain Current vs. Source to Drain Voltage



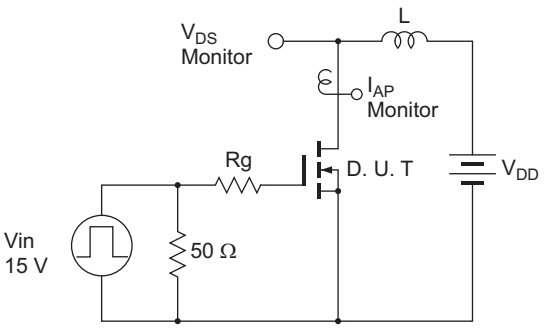
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

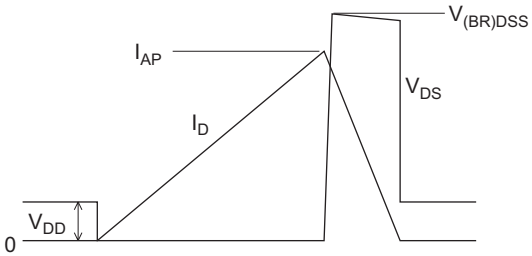


Avalanche Test Circuit

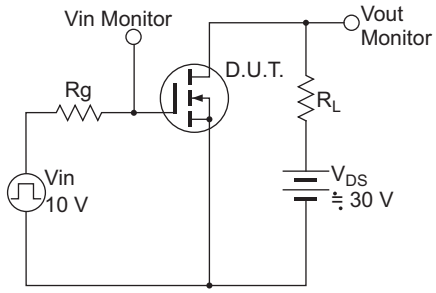


Avalanche Waveform

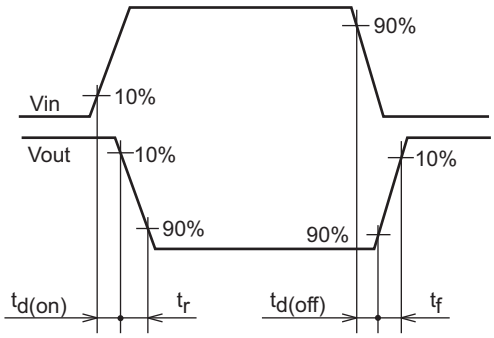
$$E_{AS} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



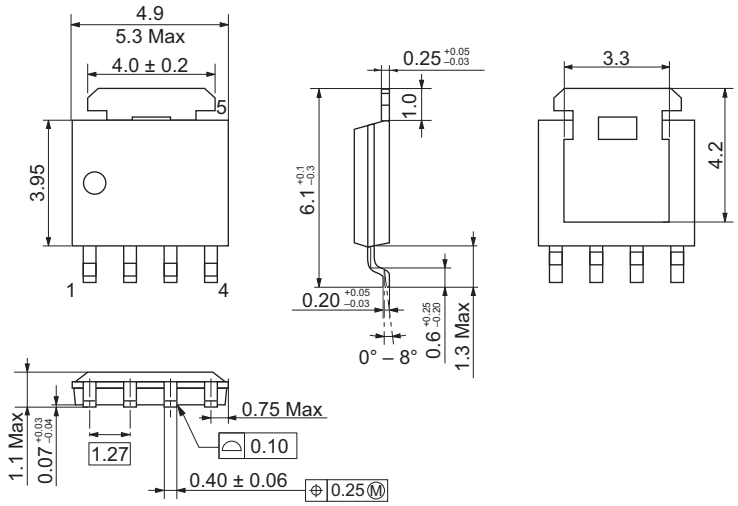
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part No.	Quantity	Shipping Container
RJK1052DPB-00-J5	2500 pcs	Taping

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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