AN3317
Application note

PCB guidelines for SPEAr1340

This document applies to the SPEAr1340 embedded microprocessor, and is intended to assist experienced printed circuit board designers.

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1 Power integrity

One of the most important requirements of a reliable high-speed memory interface, and most commonly underestimated, is a low impedance, wide bandwidth power supply at the power and ground balls of the devices.

Achieving the necessary performance requires minimizing all parasitic inductances found in power delivery and grounding connections, exploiting various techniques to provide low impedance paths, and attention to controlling plane resonances.

A solid, unbroken ground plane located close to the high-speed devices in the PCB layer stack is critical. The ground plane must not have large gaps anywhere in the area of the interface. Be especially aware of overlapping antipads that can create an extended gap in the internal plane layers.

A power plane closely spaced to the ground plane greatly aids in high-frequency decoupling by providing a low inductance path between a capacitor and the device's power balls.

Use a low-inductance layout for all high-frequency decoupling capacitors.

2 PCB layer stacking

Include a closely spaced power and ground plane pair; a minimum of 6 layers is recommended, as follows:

- Layer 1: signal
- Layer 2: ground plane, unbroken
- Layer 3: power plane and islands, signals
- Layer 4: signal and power routing
- Layer 5: ground plane, unbroken
- Layer 6: signal

Select dielectric thickness to support required signal trace characteristic impedances and power plane capacitance and inductance.

Perform resonance analysis on all plane cavities.

3 Via padstack

Ensure that via padstack dimensions support density requirements.

While meeting PCB fabrication tolerances, make antipad diameters small enough to allow an adequate copper web between the clearance holes of adjacent vias.

3.1 Part orientation and placement

To optimize routing and signal integrity, give the DRAM placement and orientation priority over other unassociated components.

Orient DRAM components such that the DQ balls face the controller.

Define a dedicated area for the memory system that encloses all components associated with the memory system and excludes all other components and signal routing.

4 Ground and power supply connections

For proper device operation, it is critical to provide a very low impedance, wide bandwidth connection to ground and to the voltage supplies. To achieve this, minimize inductance between the device power and ground balls, and the PCB ground plane and decoupling network. This guideline also applies to other critical components:

- termination resistors
- decoupling capacitors
- ICs
- multiple ground or power pins from the same IC

Directly connect each ground ball to the PCB ground plane with its own via. Do not share vias among multiple ground balls.

Exception: the center 10 x 10 ground ball grid should have a fully populated ground via grid between the balls, and the surface layers may be filled.

Directly connect each power ball to the PCB decoupling network with its own via. Do not share vias among multiple power balls.

Exception: when multiple power balls are adjacent to each other and are connected to the same voltage plane, but use the maximum number of vias that space allows.

To avoid cross-contamination of ground or power supplies between different devices (for example, an IC and a termination resistor), do not share ground connections among multiple ground or power balls. Give each ball and pin its own via to the ground or power plane. Do not simply connect power and ground connections to surface layer copper fill areas, which are not good low impedance paths at high frequencies.

Ball-to-via trace: Connect each ground and power ball to its via with a short, wide trace. Do not simply connect ground or power balls to surface fill areas; a close, direct via to the ground or power plane is necessary.

Caution: It is critical to *minimize* trace length and *maximize* trace width.

- In the ball field, make trace length less than 1 mm.
- Outside the ball field, make trace length less than 0.25 mm.
- Make trace width wide.

Note: When it is not possible to achieve a close direct trace, a relatively high impedance will result. Make every effort to minimize trace length, and consider high impedance power connections only for power connections that require lower bandwidth.

5 DDR memory interface

5.1 DRAM power decoupling

A low impedance, wide bandwidth power delivery network (PDN) is critical for the proper operation of high-speed ICs such as SPEAr and DDR memory. If the PDN impedance is too high or does not have sufficient bandwidth, logic performance is affected. This results in ground and rail bounce, and slower rise and fall times of both IO and internal logic, which in turn results in delayed timing of events. These timing delays from inadequate ground and power subtract directly from the specified timing budget, which can result in interface failure.

To achieve a low impedance wide bandwidth power delivery network, use the appropriate decoupling capacitors and capacitor layout. A large portion of the power delivery network's frequency spectrum is above the decoupling capacitor's series resonant frequency, where they are inductive. The PCB layout for decoupling capacitors is also inductive, and is a larger inductance than that of the capacitors themselves.

For IC core voltage and high-speed IO supplies (such as DDR) select:

- capacitors with low inherent inductance (small package size)
- a lossy dielectric
- a PCB layout that provides the lowest possible inductance

Use as many capacitors as can fit in the space available. This creates many parallel paths, reducing the overall inductance seen by the IC. A small capacitor package size and a small layout enable this.

5.1.1 Capacitors

See also, *Appendix A: Low-inductance capacitor layout in high-frequency applications*

Package: Use 0402 package size to minimize mounting inductance. The small 0402 package also frees board space, which is essential in high density areas for more decoupling capacitors and signal routing.

Capacitance: 100 nF or larger

A few capacitors of smaller value will probably be necessary for plane resonance suppression. The correct values for these depend on the board layout and stack up, and must be determined individually for each unique PC board.

Dielectric: X7R or X5R dielectric. Do *not* use Y5V dielectric for decoupling mid-frequency applications.

Decoupling capacitor layout

Decoupling capacitors layout is extremely important to minimize the induction loop formed between the capacitor and the IC power and ground balls. Using the layout guidelines that follow can reduce the capacitor mounting induction loop by 50% or more over a layout with vias at the end of the capacitor lands. If space allows, a second pair of vias on the opposite side of the capacitor will reduce the inductance further. Closely follow the decoupling layout example on *page 10*.

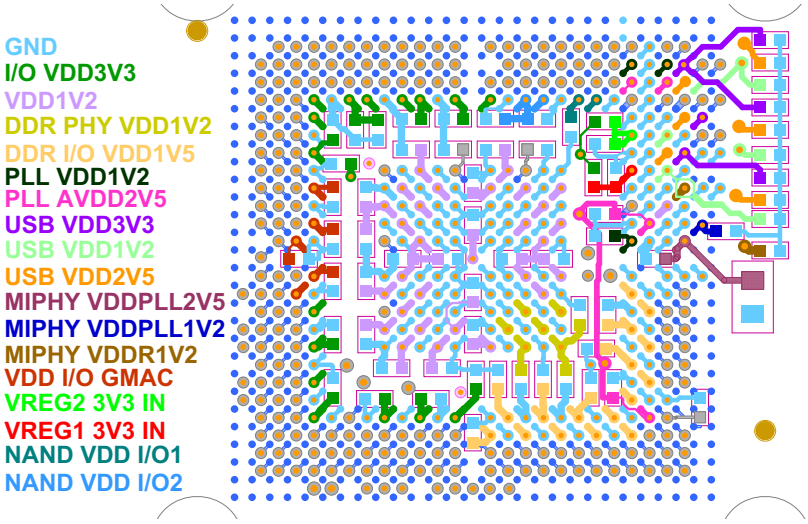
- Place vias on the side of the capacitor lands, not on the ends.
- Locate vias at minimum keepout distance, and connect them to the capacitor lands with a wide trace – at least as wide as the via pad.

- Place vias of opposite polarity as close together as possible (minimum keepout distance), and separate vias of the same polarity as much as possible.

Decoupling layout example

Figure 1 is an example of an effective low-inductance decoupling capacitor placement and mounting layout.

Figure 1. PCB bottom layer



5.2 Signal routing

The guidelines in this section are sufficient for initial routing. Simulate all layouts with IBIS models to verify adequate timing margins. Modify layouts as necessary to improve the interface and to comply with all timing parameters. Modifications can include trace length, width, and spacing, and stack up.

5.2.1 Data signal routing

Where routing density allows, increase trace spacing to reduce crosstalk (see also *Section 5.4: Return path integrity*).

Do not route any other signals inside or on top of the area reserved for the DDR.

Maintain adequate separation between DDR signals and any other signals.

For traces routed near the edge of a reference plane, keep the trace at least 30 mil from the edge of the reference plane.

To minimize reflection, ensure that all traces have an impedance of 45 to 55Ω.

5.2.2 CLK/CLK# and DQS/DQS# signals

Route CLK/CLK# and DQS/DQS# signals as length-matched differential pairs.

5.3 Trace length matching

Always use trace length equalization to maximize the valid timing window of all signals, and include the trace lengths inside the SPEAr device package.

A spreadsheet that compensates for the trace lengths inside the substrate is available to compute the necessary PCB trace length offsets (contact ST).

Fly-by and balanced-T topologies each have advantages and disadvantages. Which topology is best suited for a particular application must be evaluated on a case-by-case basis, and take into consideration any other system constraints.

5.3.1 Address, control, and command (A/C/C) signal group, fly-by configuration

Match trace lengths on the address, control, and command trace segments between the SPEAr device and the first memory device in the chain.

The spreadsheet mentioned above is the easiest way to compute lengths for the A/C/C signal group between the SPEAr device and the first memory device.

Match trace lengths for each segment group between memory devices.

Locate terminations beyond the final memory device in the chain.

Length matching is not critical between the final memory device and the termination, but keep the termination components reasonably near the final memory device.

Ensure that the termination resistors have excellent decoupling.

5.3.2 A/C/C signal group, dual DRAM balanced-T configuration

Balanced-T topology does not require termination resistors (except for clk and nclk).

Balanced-T topology does require equal length branches on all signals within the A/C/C signal group. Signal integrity degrades rapidly with unequal branch lengths, with serious negative effects on signal timing.

The spreadsheet mentioned above is the easiest way to compute lengths for the A/C/C signal group.

Place the differential clock termination resistors near the T junction.

For a *single rank* dual DRAM configuration, either fly-by or balanced-T topology can be used.

5.3.3 Data signal groups

Provide matched trace lengths for each 8-bit data slice, DM signals, and DQS/DQSn signals. It is not necessary to match the trace lengths of one data slice with the trace lengths of any other data slice, because they are independent from a timing perspective. The spreadsheet mentioned above is the easiest way to compute lengths for each data slice signal group.

Figure 2 and *Table 1* describe the length matching guidelines for a dual DRAM topology.

Note: This is a guideline only; perform simulations using IBIS models on the actual PCB layout to assess signal integrity and timing margin.

Fly-by topology routes A/C/C signal groups in a daisy chain fashion, with terminations on all signals after the last DRAM device. Data lane slices are routed to individual DRAM devices.

Balanced T topology can be used for A/C/C signal groups if only two memory devices are used.

Figure 2. Routing topologies

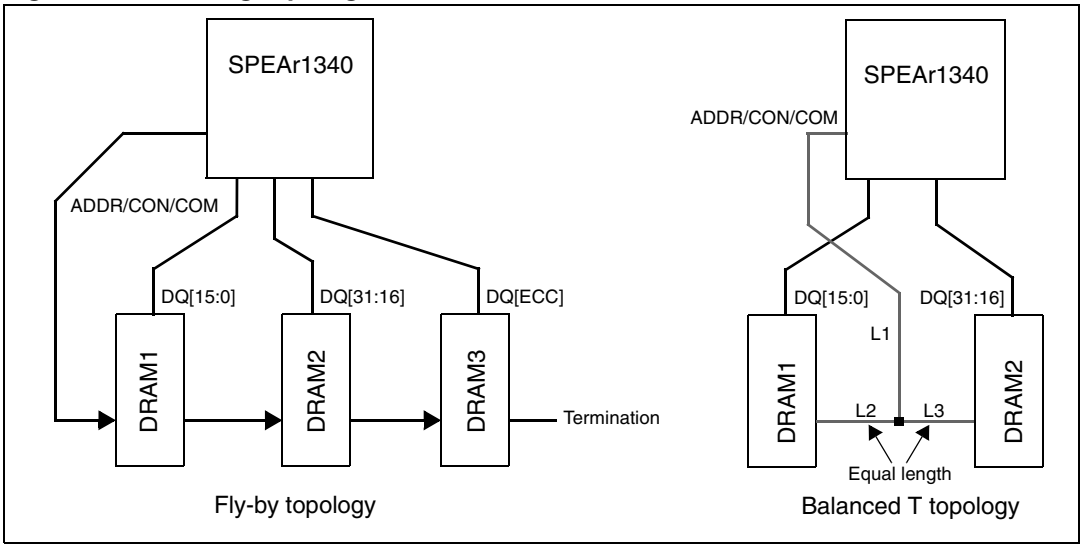


Table 1. Trace length matching guidelines, balanced-T configuration

Parameter	Description	Maximum	Unit
t_{mm}	L1+L2, L1+L3 length matching for all signals	15	ps
$T_{mm2,3}$	|L2-L3| length matching tolerance of branches	30	ps

5.3.4 Data signal routing

To simplify the routing of the data signals, it is possible to swap data between data slices. But it is mandatory to route and connect the SPEAr DDR_DQ0 (ball AF2), DDR_DQ8 (ball AH3) DDR_DQ16 (ball AE8) and DATA24 (ball AH9) on each LSB DDR data pin.

Figure 3. Data signal routing

5.4 Return path integrity

To minimize signal delays, significant crosstalk, and timing violations, a continuous path for return current must exist for all DRAM signals.

To simplify return paths, route all signals referenced to a ground plane.

Do not route any DDR3 signals on top of split planes or copper voids.

For traces routed near the edge of a reference plane, keep a minimum of 30 mil between the trace and the edge of the reference plane.

Signal layer changes

The preferred location for layer change vias is near the signal ball under a device, either DRAM or SPEAr, enabling a signal return path through the device ground vias and decoupling capacitors.

If layer changes through a via to a different reference plane are necessary away from the devices:

- Provide the layer transitions a nearby path for return current.
- If both layers are ground, place a return path ground via less than 1 mm from the signal via.
- Avoid sharing return current vias; each signal via should have its own nearby return via (ground via). If multiple signals change layers in close proximity:
  - Provide each signal via its own return current via.
  - Use a stagger pattern to separate signal vias (and their return current vias) from other signal vias.
  - If routing density prevents a stagger pattern, add as many ground vias as possible among the signal vias.

5.5 Vref routing

Provide an accurate and quiet Vref to both the dram and the controller. Because of the slope of the signal, a noisy Vref effectively introduces jitter, which can be a significant source of jitter-caused timing errors.

Vref is generated by a precision voltage divider.

Recommended: Use 0.1% tolerance resistors.

Place a decoupling capacitor very close (within 1 mm) to the Vref balls.

Use good capacitor layout techniques. Place the voltage divider resistors close to the DRAM device to minimize trace length, but not so close that they interfere with other critical signal or power routing.

Do not route the Vref trace near noisy traces or planes.

Do not place a decoupling capacitor at the junction of the resistors – only at the Vref balls.

If the Vref trace length must be long, make the divider resistor value close to 2x the characteristic impedance of the Vref trace; 150 Ω should work well without consuming too much power. If a long trace, noise coupling, or both is unavoidable between the DRAM and the controller, it is preferable to generate a separate Vref for the DRAM and the controller.

5.6 Observability

For system validation, timing, signal quality, and debugging, it is important to be able to observe certain signals. Place test points on any signals or set of signals required for these purposes.

Always provide a ground via near test points for the probe ground, preferably within 1 mm. Very small test point pads can be used, preferably just a signal via. If there is insufficient space, a simple window in the solder mask over a trace provides exposed metal for probing.

Do not create test point structures that significantly degrade signal quality, such as large test points or stubs.

Locate test points at *both ends* of a trace (two test points per signal), as close to the device balls as practical (a via next to the ball is preferable, untented on the bottom layer).

In high-speed interfaces, it is especially important to be able to observe signals at both the driving and the receiving end of a trace to validate timing parameters and to quantify driver behavior and reflection. Observing a signal at only one end can hide important features that are evident at the other end, even with very short traces as is the case in a point-to-point DDR interface.

In a DDR memory interface, the routing and component density is too high to add test points on all signals. A subset of DDR signals with test points is a good compromise. Include test points for the following DDR signals in all designs:

- **CLK/nCLK**
- **DQS/nDQS**: All data lanes
- **DQ**: Select a small number of signals that represent the best and worst signal paths, at least two DQ signals.
- **Address and Control**: Select signals of interest that represent the best and worst signal paths.

6 USB routing

Ensure that USB signal trace routing follows good high speed PCB rules, and meets the specifications for differential impedance and maximum trace delay between the connector and the SPEAr device.

Route USB data traces with the shortest, most direct path possible to their connectors.

USB data traces should have no resistors.

Route USB data traces only over ground planes.

Never route USB data traces across gaps or breaks in the return plane.

Never route USB data traces under other devices or between the pins of other devices.

Widely separate USB data vias from other signal vias.

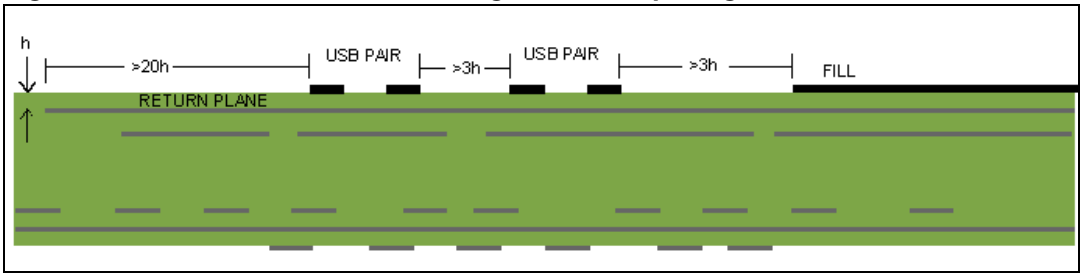
If USB data traces must transition layers to a different return plane, place ground vias for the return current very close to the signal vias.

Table 2. USB signal routing constraints

Parameter	Description	Minimum	Typical	Maximum	Units
Zo_{diff}	Differential Impedance(1)	81	90	99	Ω
Td Dev	Trace delay of device port(1)			1.0	ns
Td Host	Trace delay of host port(1)			3.0	ns
Td-match	Trace length mismatch			0.15 3.8	inch mm
—	Number or length of stubs			0	
—	Number of via transitions			1	
—	Space to adjacent signal traces(2)	3			h(3)
—	Space to adjacent area fill(4)	3			h(3)
—	Space to edge of return plane	20			h(3)

1. Trace delay between SPEAr device and USB connector (*Universal Serial Bus Specification*, Revision 2.0)
2. Includes other USB data trace pairs.
3. The same as the units used for h, the thickness of the dielectric separating the trace from the nearest plane (see *Figure 4*), which can vary from board-to-board.
4. Do *not* use guard traces or ground flood or fill adjacent to high speed signal traces.

Figure 4. PCB cross section showing minimum spacing dimensions



6.1 USB decoupling and reference resistor

Place decoupling capacitors as close as possible to the power balls (preferably directly under the power balls) using short, wide connecting traces.

Placing decoupling capacitors at a distance degrades performance, which can result in interoperability problems and specification compliance violations.

Table 3. USB power, ground, and reference guidelines

Pin	Guideline
vss	Connect all vss pins directly to internal PCB ground plane
vdd	Connect all vdd pins to 100 nF capacitor under ball using short wide trace
USB_TXRTUNE	43.2 Ω resistor to ground

7 TDR test traces

Add test traces to all PCB designs on all signal layers.

It is simple to add a single trace of nominal impedance between 8 to 15 cm long on each signal layer (it does not have to be straight) to all designs, and can it always be placed where it will not impact the functional design, for example, usually along the board perimeter.

Include a test point pattern that matches your TDR probe. Test traces are invaluable in validating PCB impedance parameters.

8 Layer order check

Include a visual feature (stair step numbered windows) to verify layer ordered in all PCB layouts. This is most commonly located along one edge of the board.

Appendix A Low-inductance capacitor layout in high-frequency applications

Figure 5 shows several decoupling capacitor layouts.

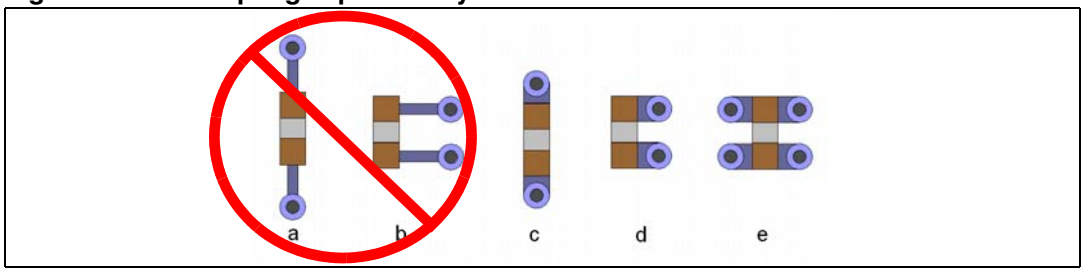
Do *not* use layouts **a** or **b**. These layouts have inherently high inductance, and thus a high impedance at high frequencies.

Use layout **d** or **e** for high frequency decoupling applications. These layouts have low inductance.

- Where space allows, use the 4-via layout (e), which has the lowest inductance but requires more board area.
- Where space does not permit the 4-via layout, the 2-via layout (d) is a good compromise.

Use layout **c** as a last resort when there is no space for either layout **d** or **e**.

Figure 5. Decoupling capacitor layouts



A.1 0402 package compact land pattern

An area-efficient compact land pattern facilitates PCB layout of decoupling capacitors. *Figure 6* shows a commonly used land pattern.

Figure 6. 0402 package compact land pattern

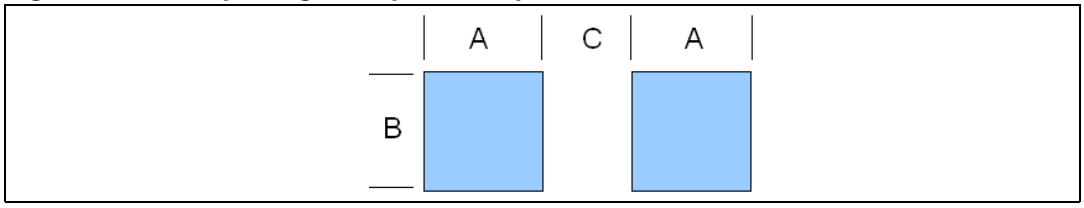


Table 4. 0402 package compact land pattern dimensions

Dimension	Distance (mil)
A	20
B	20
C	15

A.2 0402 package low inductance layout

Figure 2 shows a low inductance layout for a 0402 decoupling capacitor using 2 vias with a 10 mil drill size. Note that:

- Vias are placed close to the lands.
- Vias of opposite polarity are place close together.
- The trace connecting land to via is wide.

Figure 7. 0402 package low inductance layout

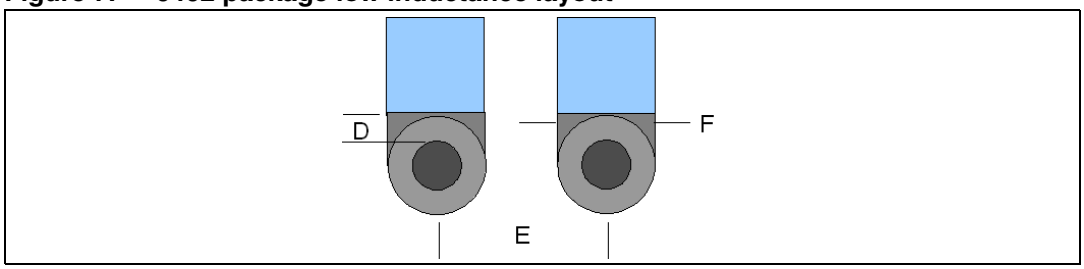


Table 5. 0402 packages low inductance layout dimensions

Dimension	Distance (mil)
D (land to hole)	Typically 8 to 10(1)
E (hole to hole)	Typically 30(2)
F (trace width)	20

1. The land to hole separation is determined by the PCB fabrication tolerances.
2. Minimize this distance, consistent with PCB fabrication tolerances. If the capacitor is placed within a BGA ball field, make dimension E the same as the ball pitch.

Revision history

Table 6. Document revision history

Date	Revision	Changes
14-Mar-2012	1.0	Initial release
06-Apr-2012	2.0	Update ST Corporate template