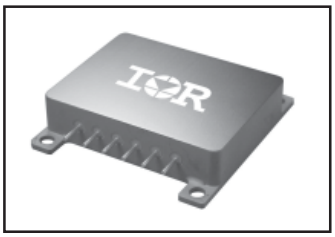
International
IOR Rectifier

PD-97819

D28XXD-SERIES

28V Input, Regulated Dual Outputs

HIGH RELIABILITY, RADIATION TOLERANT, LOW POWER, DC-DC CONVERTER



Description

The D-Series of DC-DC converters are low power radiation tolerant, high reliability devices designed for hostile radiation environments such as those encountered by geostationary earth orbit satellites, deep space probes and communication systems. Features include small size, high efficiency, low weight, and a good tolerance to total ionizing dose, single event effects, and environmental stresses such as temperature extremes, mechanical shock, and vibration. All components are fully derated to meet the requirements of EEE-INST-002 and MIL-STD-1547B. Extensive documentation including worst case analysis, radiation susceptibility, thermal analysis, stress analysis, and reliability analysis are available.

The D-Series converters have two outputs, each is independently regulated. Two versions exist; One version providing two positive outputs and one version providing one negative and one positive output. The D-Series converters incorporate a fixed frequency flyback power converter and internal EMI filter that meets the requirements for most major satellite power buses. The converters can be remotely turned on and off via an inhibit pin. Additional inhibit pins are also included to control the outputs individually. This feature facilitates turn-on outputs sequencing if desired. Each converter is encased in a cold rolled steel hermetic package. The package measures 1.80"L x 1.40"W x 0.42"H and weighs less than 55 grams. The package utilizes rugged ceramic feed-through copper pins and is hermetically sealed using parallel seam welding. Two package options are available. Please refer to page 9 for I/O configurations.

Environmental screening includes temperature cycling, constant acceleration, fine and gross leak, and burn-in as specified by MIL-PRF-38534 for class H hybrids.

Non-flight versions of the D-Series converters are available for system development purposes. Variations in electrical specifications and screening to meet custom requirements can be accommodated.

Features

- Total Dose > 50K Rad(Si)
- SEE > 40MeV.cm²/mg
- Low Weight < 55 grams
- 18V to 50V DC Input Range
- Up to 10W Output Power
- Independently Regulated Outputs: ±5V, ±12V and ±15V
- -55°C to +125°C Operating Temperature Range
- 100MΩ @ 100VDC Isolation
- Input Under-Voltage Protection
- Meets Conducted Emission Requirements of Most Major Power Buses:
  100Hz - 100KHz: 80dBμArms
  100KHz - 10MHz: Log-linear Decrease
  10MHz - 50MHz: 40dBμArms
- Short Circuit and Overload Protection
- Meets the Derating Requirments of EEE-INST-002 and MIL-STD-1547B
- Synchronization Input / Output
- On/Off Control via Converters's Inhibit Pin and Individual Output's Inhibit Pin
- High CS Damping

Applications

- Launch Vehicles
- Communication Systems
- Geostationary or Low Earth Orbit Satellites

Circuit Description

The D-Series DC-DC converters utilize two-stage regulation with a flyback topology with a switching frequency of 250KHz for primary regulation and linear post regulation in the secondary for each of the outputs.

Output power is limited under any load fault condition to approximately 110% of rated output. An overload condition causes the converter output to behave like a constant current source with the output voltage dropping below nominal. The converter will resume normal operation when the load current is reduced below the current limit point.

This protects the converter from both overload and short circuit conditions. There are no latching elements to eliminate the possibility of falsely triggering the protection circuits during single event radiation exposure.

An under-voltage protection circuit prohibits the converter from operating when the line voltage is too low for safe operation. The converter will not start until the line voltage rises to approximately 16V.

An inhibit pin is provided to control converter operation. This inhibit pin is intended for operation with an open collector transistor drive or a relay closure to the input return. The pin may be left open for normal operation and has a nominal open circuit voltage of 4V. Also provided are the individual output on/off control pins (Pin 10-Output 1 Inhibit and Pin 9-Output 2 Inhibit).

Synchronization input pin is included allowing multiple converters to operate at a common switching frequency. Converters can be synchronized to a common frequency with an external clock. This may be used to eliminate beat frequency noise or to avoid generating noise at certain frequencies for noise sensitive systems.

Design Methodology

The D-Series is developed using a proven conservative design methodology, which includes selecting radiation tolerant and established reliability components and fully derating to the requirements of EEE-INST-002 and MIL-STD-1547B. Heavy derating of the radiation-hardened power MOSFET virtually eliminates the possibility of SEGR and SEB.

Specifications

Absolute Maximum Ratings		Recommended Operating Conditions	
Input voltage range	-0.5Vdc to +60Vdc	Input voltage range (Note 13)	18Vdc to 50Vdc
Output power	Internally limited	Output power	0 to Max. Rated
Lead temperature	+300°C for 10sec	Operating temperature	-55°C to +125°C
Operating case temperature (Note 12)	-55°C to +125°C	Operating temperature,	-55°C to +73°C
Storage temperature	-55°C to +135°C	derated (Note 13)	

Electrical Performance Characteristics

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 28V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Input voltage (V_{IN})			18	28	50	V
Output voltage (V_{OUT})						
D2805D	1	I_{OUT} = 100% rated load	±4.95	±5.00	±5.05	
D2812D	1	Note 4	±11.88	±12.00	±12.12	V
D2815D	1		±14.85	±15.00	±15.15	
D2805D	2,3	I_{OUT} = 100% rated load	±4.85		±5.15	
D2812D	2,3	Note 4, 14	±11.64		±12.36	V
D2815D	2,3		±14.70		±15.15	
Output power (P_{OUT})						
D2805D	1,2,3	V_{IN} = 18, 28, 50V, Note 2	0		5.0	
D2812D		Either Output	0		5.0	W
D2815D			0		5.0	
Output current (I_{OUT})						
D2805D	1,2,3	V_{IN} = 18, 28, 50V, Note 2	0		1.00	
D2812D		Either Output	0		0.42	A
D2815D			0		0.33	
Line regulation (VR_{LINE})	1,2,3	V_{IN} = 18, 28, 50V I_{OUT} = 0%, 50%, 100% rated	-0.05		0.05	%
Load regulation (VR_{LOAD})	1,2,3	I_{OUT} = 0%, 50%, 100% rated V_{IN} = 18, 28, 50V	-1.0		1.0	%
Cross regulation (VR_{CROSS})						
D2805D	1,2,3	V_{IN} = 18, 28, 50V, Note 1			5.0	
D2812D					5.0	mV
D2815D					5.0	
Input current (I_{IN})						
D2805D	1,2,3	I_{OUT} = 0, Pin 6 open			35	
D2812D					35	mA
D2815D					35	
		Pin 6 connected to Pin 2			10	
Switching frequency (F_S)	1,2,3	Sync. Input (Pin 4) open	225	250	275	kHz

For Notes to Electrical Performance Characteristic Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 28V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Synchronization input						
Frequency range			450		550	kHz
Pulse high level		External clock on sync In (Pin 4),	2.5		5.0	V
Pulse low level	1,2,3	Note 1	-0.5		0.5	V
Pulse transition time			40			V/µs
Pulse duty cycle			20		80	%
Output ripple (V_{RIP})						
D2805D		V_{IN} = 18, 28, 50V			20	
D2812D	1,2,3	I_{OUT} = 100% rated load			20	mV p-p
D2815D		Note 3			20	
Output ripple @ switch frequency		V_{IN} = 18, 28, 50V				
D2805D	1,2,3	I_{OUT} = 100% rated load		0.5	1.0	
D2812D		Note 1		0.5	1.0	mV rms
D2815D				0.5	1.0	
Efficiency (E_{FF})						
D2805D			55	58		
D2812D	1,2,3	I_{OUT} = 100% rated load	61	64		%
D2815D			62	65		
Inhibit input						
Open circuit voltage		Note 1			4.0	V
Drive current (sink)					600	µA
Voltage range					50	V
Current limit point						
D2805D		V_{OUT} = 90% of Nominal	105		145	
D2812D	1,2,3	Note 10	105		145	%
D2815D			105		145	
Power dissipation load fault (P_D)	1,2,3	Short Circuit, Overload, Note 5			8.0	W
Output response to step load changes (V_{TLD})						
D2805D			-15		15	
D2812D	4,5,6	Half Load to/ from Full Load, Note 6	-15		15	mV pk
D2815D			-15		15	
Recovery time, step load changes (T_{TLD})						
D2805D					500	
D2812D	4,5,6	Half Load to/from Full Load, Notes 6, 7			500	µs
D2815D					500	
Recovery time, step line changes (T_{TLN})	4,5,6	18V to/from 50V I_{OUT} = 100% rated load, Notes 1, 7, 8			100	µs

For Notes to Electrical Performance Characteristic Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T_C ≤ +85°C V_{IN} = 28V DC ± 5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Capacitive load (C_L) D2805D D2812D D2815D	1	I_{OUT} = 100% rated load No effect on DC performance Notes 1, 4 Each output			 220 33 33	µF
Turn-on response overshoot (V_{OS}) D2805D D2812D D2815D Turn-on delay (T_{DLY})	4,5,6	10% Load, Full Load Note 9			 25 25 25 10	 mV ms
Enable input (Inhibit) open circuit voltage Drive current (sink) Voltage range	1,2,3	Note 1	 0		 10 100 0.4	 V µA V
EMC conducted susceptibility (Line rejection)	1	I_{OUT} = 100% rated load Primary power sine wave injection of 2Vp-p, 100Hz to 50MHz, Note 1	80	90		dB
Electromagnetic Interference (EMI), conducted emission (CE)	1	I_{OUT} = 100% rated load, Note 1	Limits per Fig. 1			
Isolation	1	Input to Output or Any Pin to Case except Pin 3, test @ 100 VDC	100			MΩ
Device Weight					55	g
MTBF		MIL-HDBK-217F2, SF, 35°C	100.000			Hours

Notes: Specification and Electrical Performance Characteristics

1. Parameter is tested as part of design characterization or after design changes. Thereafter, parameter shall be guaranteed to the limits specified.
2. Parameter verified during line and load regulation tests.
3. Guaranteed for a D.C. to 20 MHz bandwidth. Tested using a 20 kHz to 10 MHz bandwidth.
4. Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's overload protection, causing erratic behavior during turn-on.
5. Overload power dissipation is defined as the device power dissipation with the load set such that V_{OUT} = 90% of nominal.
6. Load step transition time ≥ 100 µs
7. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady state value.
8. Line step transition time ≥ 100 µs.
9. Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the Inhibit Pin (Pin 6) to the point where V_{OUT} = 90% of nominal.
10. Current limit point expressed as a percentage of full rated load current.
11. For models with two positive outputs the envelope specification for the design is that each output voltage is limited to the range 1V to 5V.
12. Although operation at temperatures between +85°C and +125°C is guaranteed, no parameter limits are specified.
13. Meets the derating requirements of EEE-INST-002 and MIL-STD-1547B – except for ceramic capacitors with voltage stress below 10V will minimum be rated at 50V.
14. End of life is ± 3%

Device Screening

Test / Inspection	Method	/EM Suffix	Flight (No Suffix)
Element Evaluation	MIL-STD-38534 Class K equivalent with SEM		X
Nondestructive Bond Pull	MIL-STD-883, Method 2023		X
Internal Visual	MIL-STD-883, Method 2017		X
Temperature Cycling	MIL-STD-883, Method 1010		Condition C
Constant Acceleration	MIL-STD-883, Method 2001 (3Kg)		A, Y1 Axis only
Electrical	In accordance with device specificaton		X
PIND	MIL-STD-883, Method 2020		A
Burn-in (2 x 160 hours)	MIL-STD-883, Method 1015	48 Hours	320 Hours
Final Electrical (Group A)	In accordance with device specification	X	X
Seal	MIL-STD-883, Method 1014	Condition A	
Fine Leak			A1
Gross Leak			C
Radiographic	MIL-STD-883, Method 2012		N/A
External Visual	MIL-STD-883, Method 2009	X	X

Radiation Performance Characteristics

Test	Conditions	Min	Unit
Total Ionizing Dose (Gamma)	MIL-STD-883, Method 1019.5 Operating bias applied during exposure, Half Rated Load, V_{IN} = 28V	50	KRads (Si)
Single Event Effects SEU, SEL, SEGR, SEB	Heavy Ions (LET) Operating bias applied during exposure, Full Rated Load, V_{IN} = 18, 28, 50V	40	MeV•cm^2 / mg

***** Test performed at TAMU

International Rectifier currently does not have a DLA certified Radiation Hardness Assurance Program.

Fig. 1 - EMI Conducted Emission Performance Limit

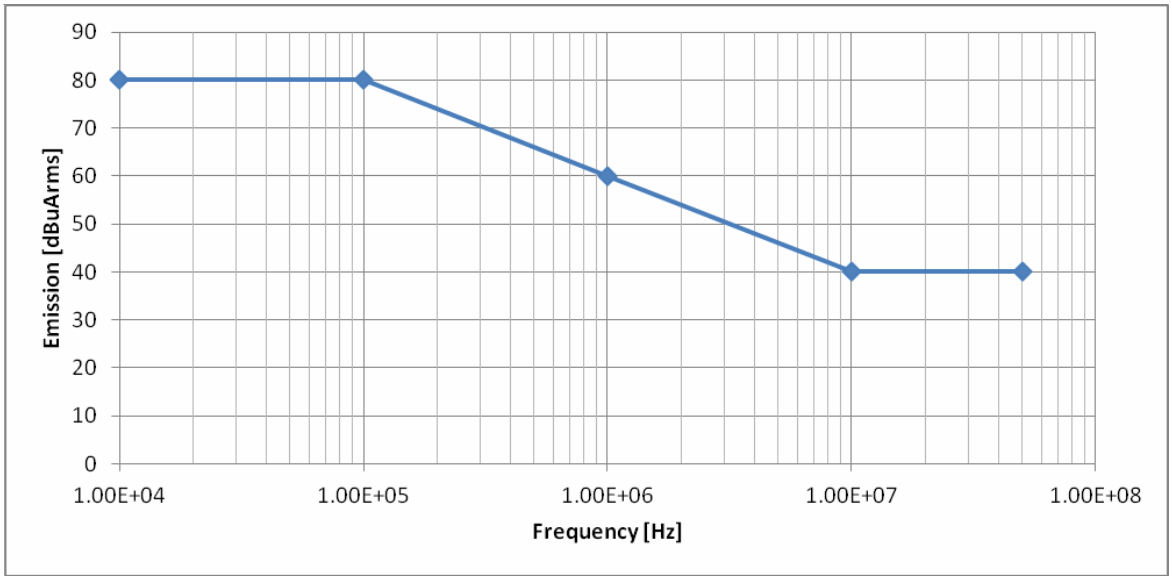
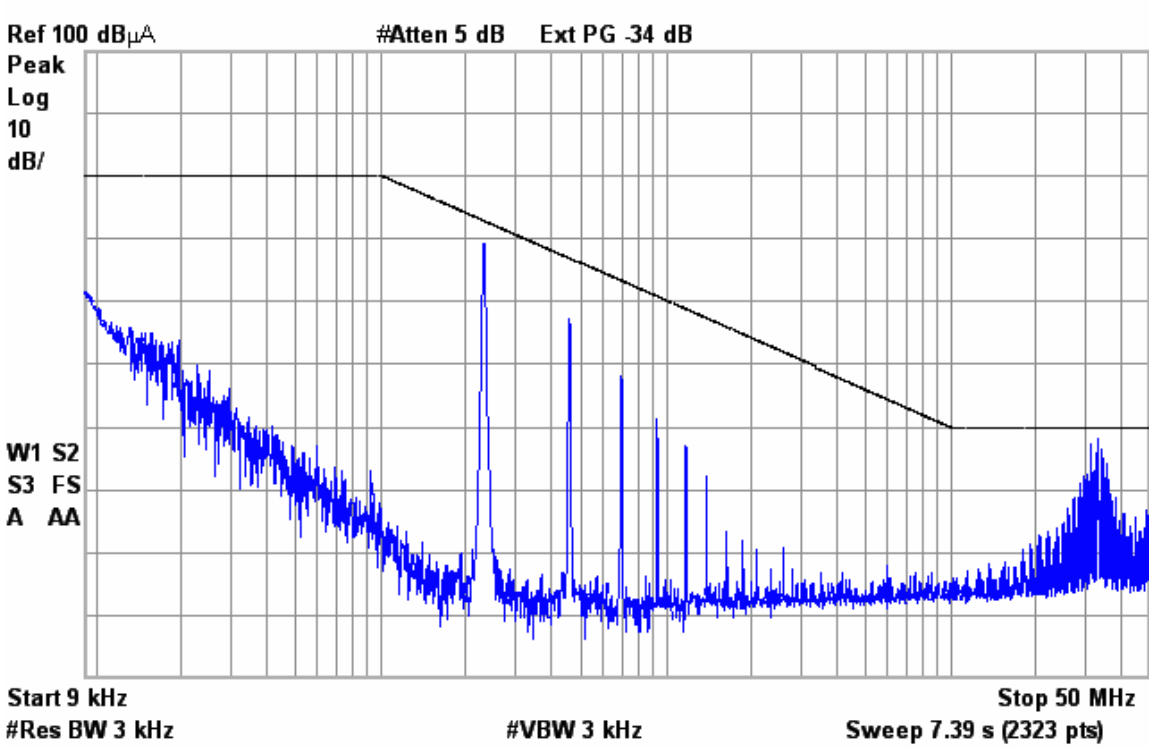
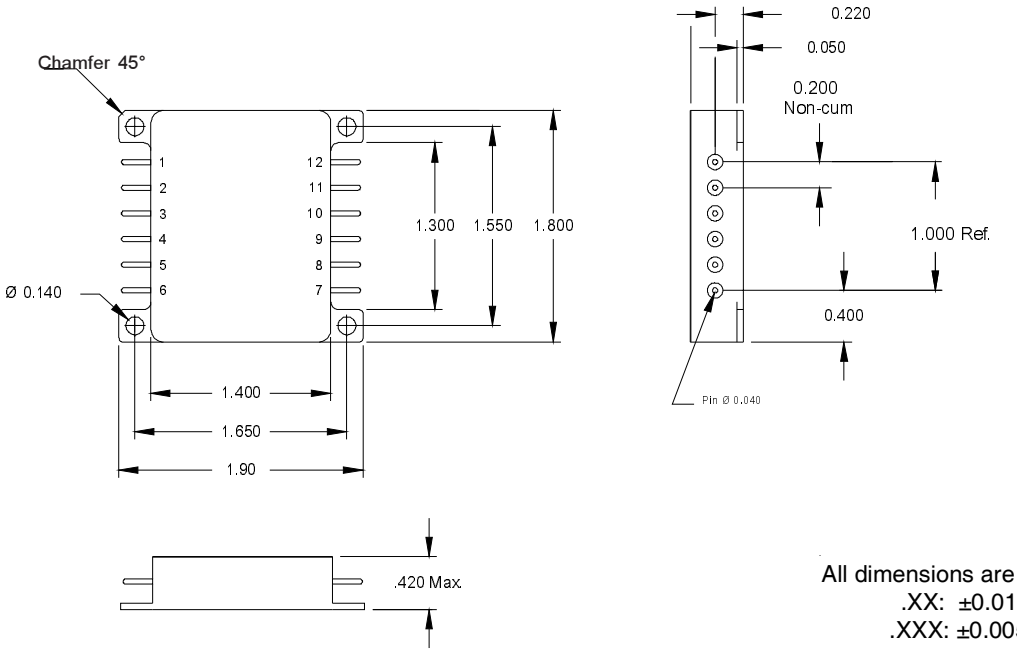


Fig. 2 - A Typical input EMI Conducted Emission Performance

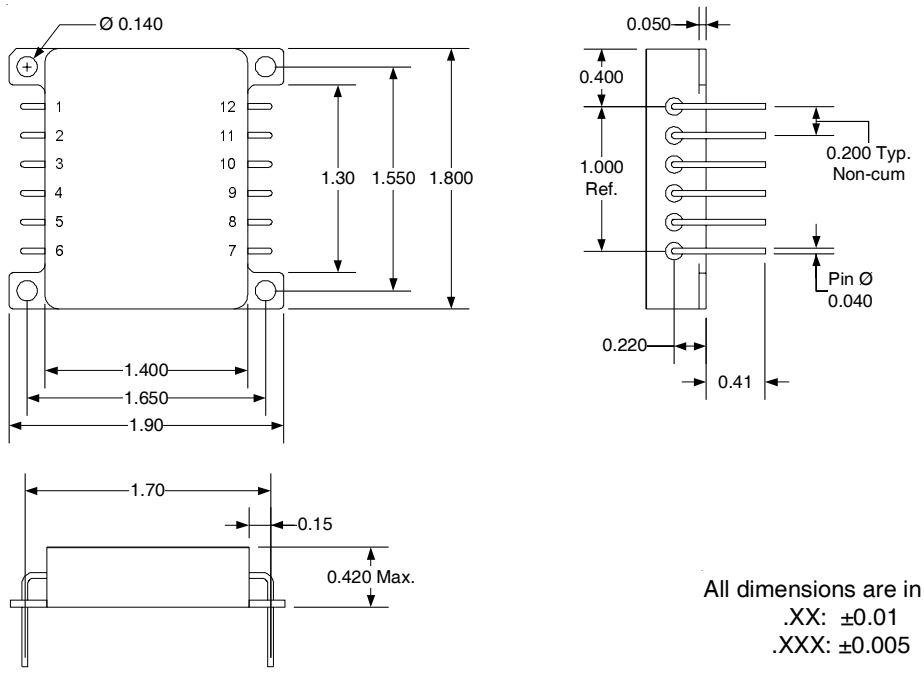


Mechanical Outline - Option A (Straight Pins)



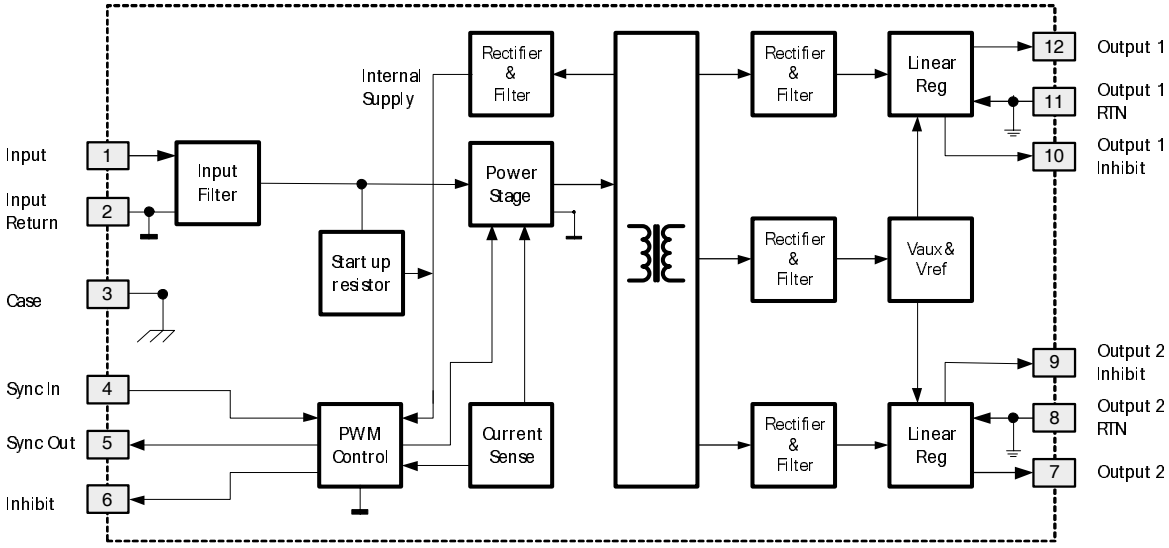
All dimensions are in inch.
.XX: ±0.01
.XXX: ±0.005

Mechanical Outline - Option B (Down Pins)



All dimensions are in inch.
.XX: ±0.01
.XXX: ±0.005

Block Diagram



Pin Designation

Pin #	Name
1	Input
2	Input Return
3	Case
4	Sync In
5	Sync Out
6	Inhibit
7	Output 2
8	Output 2 Return
9	Output 2 Inhibit
10	Output 1 Inhibit
11	Output 1 Return
12	Output 1

Note: Pins 9 and 10 are internally connected

Part Numbering

D 28 05 D A A /EM

Model
D = Two Outputs,
5W max each,
Radiation-tolerant Design

Input Voltage
28 = 28V

Output Voltage
05 = ±5V
12 = ±12V
15 = ±15V

Quality Level
EM = Engineering Model
H = Class H per MIL-PRF-38534

Lead Finish
A = Solder Dipped
C = Gold Plated
Blank = for EM, Lead finish as available

I/O Pin Option
A = Straight Pins
B = Down Pins

Output Configuration
D = One Positive, One Neagtive

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WORLD HEADQUARTERS: 101 N, Sepulveda Blvd., El Segundo, California 90245, USA Tel: (310) 252-7105
IR SAN JOSE: 2520 Junction Avenue, San Jose, California 95134, USA Tel: (408) 434-5000
Visit us at www.irf.com for sales contact information.