

# INTELLIGENT INTERACTIVE SYNTHESIZER

## SURFACE MOUNT MODEL: FSW190410-50

**WIDE BANDWIDTH**

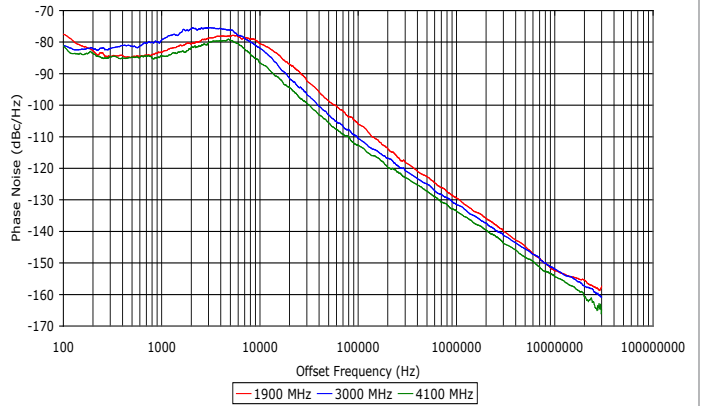
**1900 - 4100 MHz**

**FEATURES:**

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount



**Phase Noise**

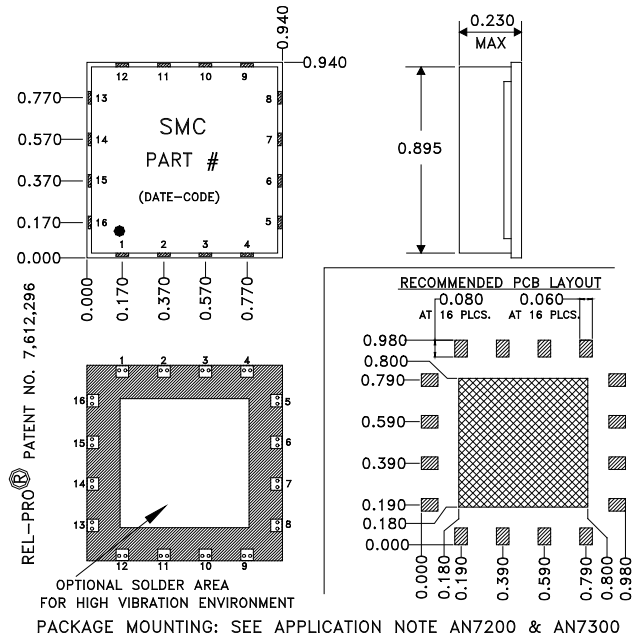


**SPECIFICATIONS (Rev. H 04/04/11)**

<b>Frequency</b>	1900 - 4100 MHz		
<b>Step Size</b>	500 kHz		
<b>Reference Input Frequency</b>	10 MHz <sup>1</sup>		
<b>Reference Input Voltage</b>	1 V p-p to 3.3 V p-p		
<b>Bias Voltage</b>	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	15
	VCO	+5	50
	Tune	+18	10
<b>Lock Detect Indicator</b>	CMOS 3.3 V		
<b>Output Power</b>	-3 dBm (Min.)		
<b>Spurious Suppression</b>	80 dB (Typ.)		
<b>Harmonic Suppression</b>	10 dB (Typ.)		
<b>Settling Time</b>	10 mSec (Typ.) <sup>2</sup>		
<b>Output Impedance</b>	50 Ohms (Nom.)		
<b>Typical Phase Noise</b>	Offset	Phase Noise	
	@ 1 kHz	-82dBc/Hz	
	@ 10 kHz	-82 dBc/Hz	
	@ 100 kHz	-109 dBc/Hz	
<b>Operating Temperature Range</b>	-20 to +70 °C		
<b>Programming</b>	See application note AN7100 for changing factory setting to desired reference frequency.		

<sup>1</sup> Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the factory default setting. 150 MHz (Max.)  
<sup>2</sup> From the rising edge of LE to stable lock detect

**Package #** 273LF



**Absolute Maximum Ratings**

<b>Storage Temp. Range</b>	-55 to +125 °C
<b>Bias Voltage (Digital)</b>	+5.25 V
<b>Bias Voltage (VCO)</b>	+5.5 V
<b>Bias Voltage (Tune)</b>	+20 V
<b>DC Voltage Applied to RF Out</b>	±25 V

Port Configuration		
Pin 1,2,3 - NC	Pin 8 - Vcc (Tune)	Pin 16 - Clock In
Pin 4 - Error flag	Pin 9 - Vcc (VCO)	All Others - Ground
Pin 5 - Latch Enable In	Pin 13 - RF Out	
Pin 6 - Ref. In	Pin 14 - Lock Detect Out *	
Pin 7 - Vcc (Digital)	Pin 15 - Data In	NC - No Connection

\* High when locked (source/sink 500 uA)

This product is manufactured under one or more of the following patents: Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623 | Pending: 60/493075; 60/501371 & 60/501790; 60/527957 & 60/528670; 60/563481; 60/564173; 60/589090; 60/601823; 60/605791; EV31369834; 11/259766; 60/622485 & 60/710310; 10/937525/60/736901; 60/732787; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 2,563,174; 7,580,693; 7,612,296; 2,524,751

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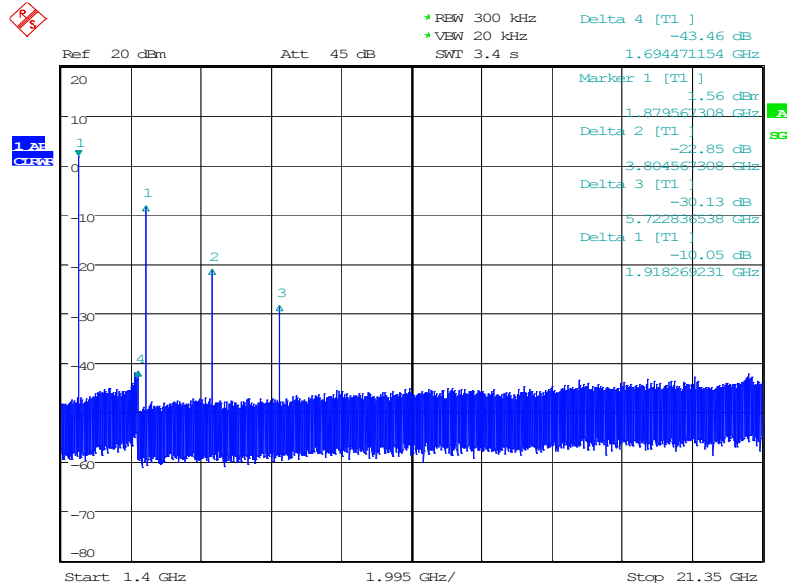
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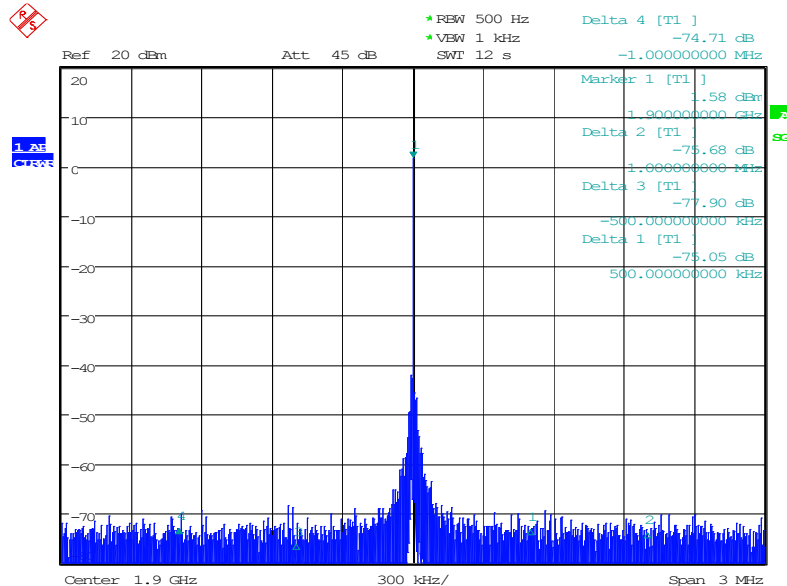
1900 - 4100 MHz

PERFORMANCE PLOTS

### HARMONIC SUPPRESSION



### REFERENCE SIDEBAND SUPPRESSION



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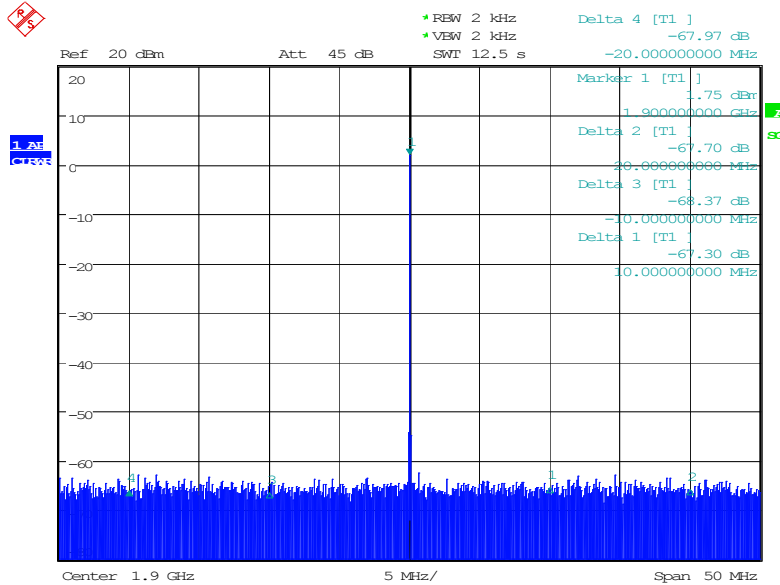
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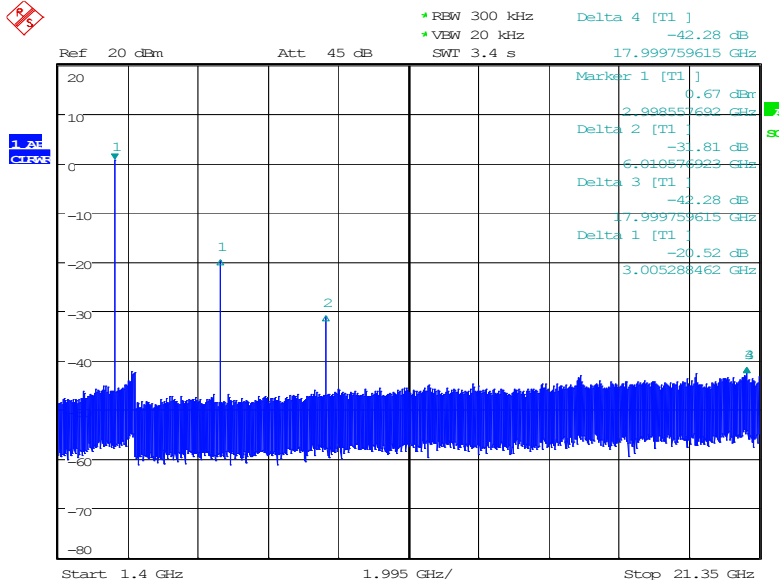
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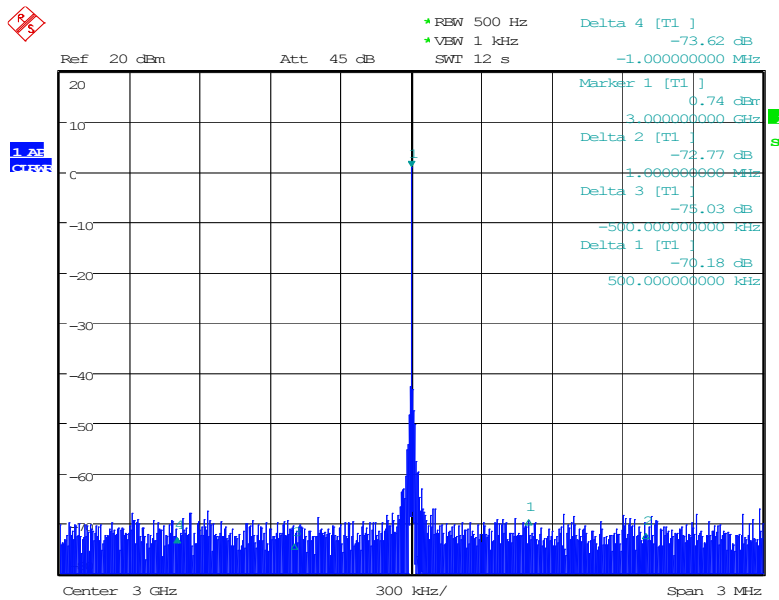
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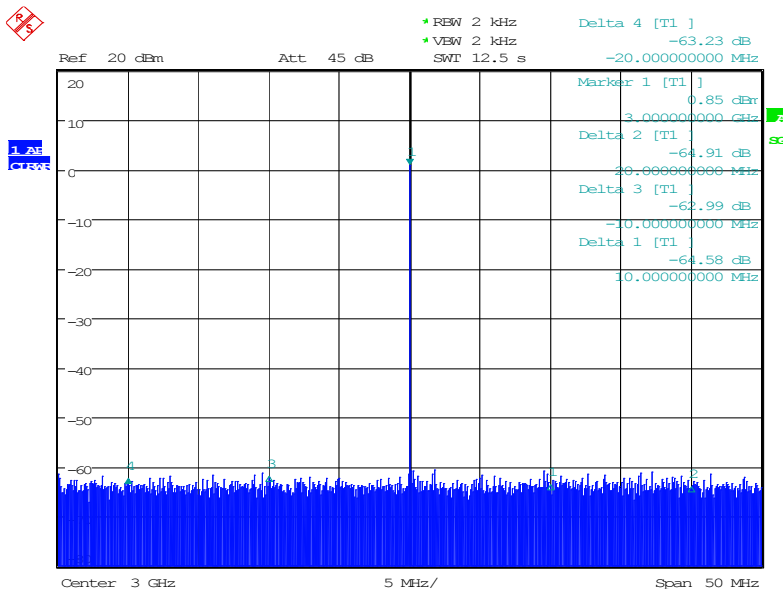
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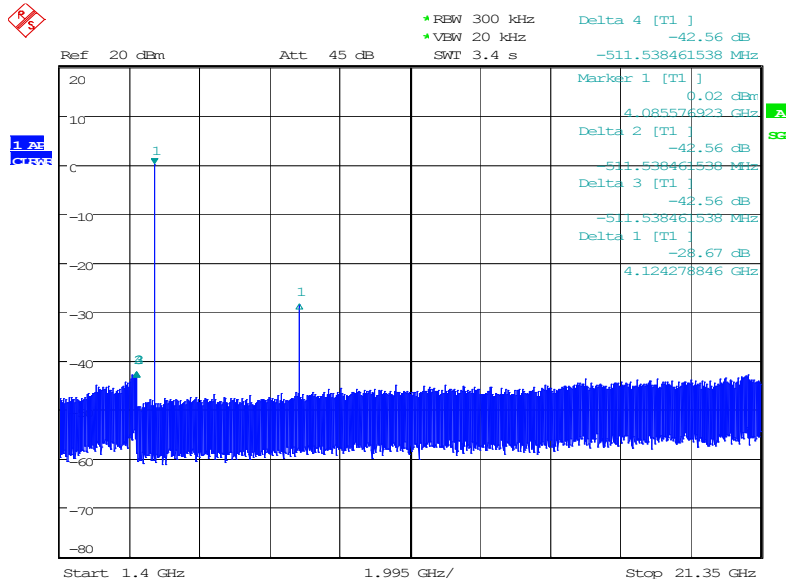
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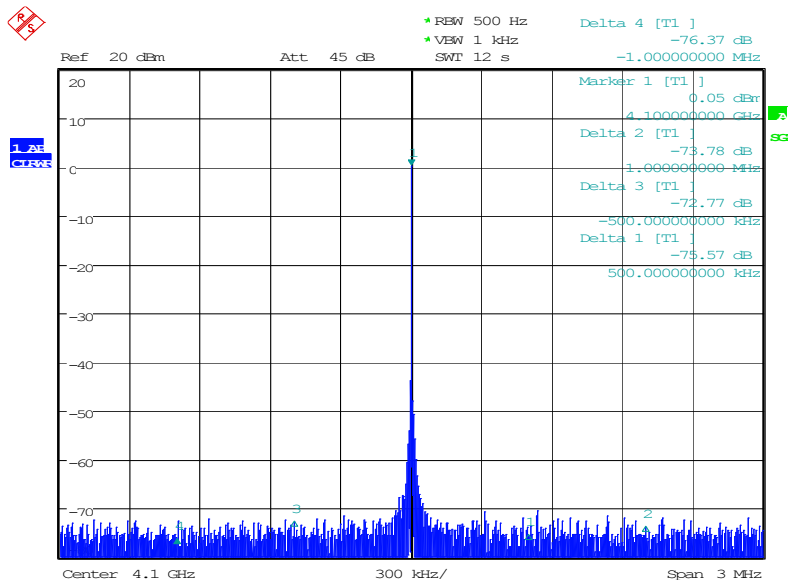
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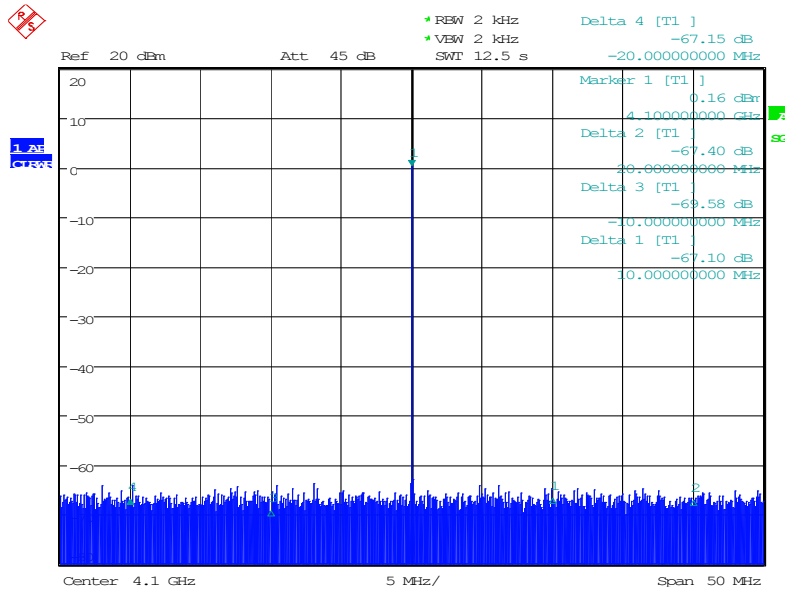
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