

For High-Output-Current Applications

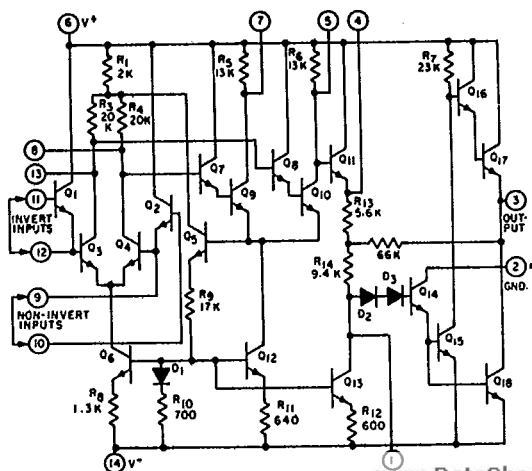
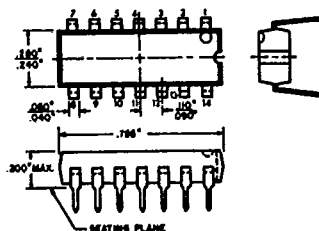
APPLICATIONS

- Comparator
- Integrator
- Differentiator
- Audio Amplifier
- Summing Amplifier
- Servo Driver
- DC Amplifier
- Multivibrator
- Narrow Band and Band Pass Amplifier

FEATURES

$V^+ = 15\text{ V}$
 $V^- = -15\text{ V}$

■ Output Current	78	mA min.
■ Input Offset Current ..	25	nA max.
■ Open Loop Differential Gain	87	dB min.
■ Output Voltage Swing.	23	V _{p-p} min.
■ Input Bias Current ...	180	nA max.
■ Power Output	220	mW min.
■ Common Mode Rejection Ratio	93	dB min.



* ("SEE OPERATION CONSIDERATIONS")

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Fig. 1 - Schematic diagram

ABSOLUTE-MAXIMUM RATINGS

ECG913

INPUT SIGNAL VOLTAGE

-13V, +10 V

DEVICE DISSIPATION:

Up to $T_A = 25^{\circ}\text{C}$

750 mW

Above $T_A = 25^{\circ}\text{C}$

Derate at 6.67 mW/ $^{\circ}\text{C}$

TEMPERATURE RANGE:

Operating

0°C to $+70^{\circ}\text{C}$

Storage

-65°C to $+150^{\circ}\text{C}$

MAXIMUM CURRENT RATINGS

MAXIMUM VOLTAGE RATINGS at $T_A = 25^{\circ}\text{C}$

ECG913

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+38 0
3				*	*	0 -38	*	*	*	*	*	*	*	+38 0
4					+5 -1	0 -22	*	*	*	*	*	*	*	+38 0
5						0 -38	*	+30 -1 Note 1	*	*	*	*	+30 -2 Note 1	*
6							+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0
7								+30 -2 Note 1	*	*	*	*	+20 -2 Note 1	+38 0
8									+30 -1 Note 2	+30 -2 Note 3	+30 -2 Note 3	+30 -1 Note 2	*	+38 0
9										+1 -5	*	+5 -5	+1 -30 Note 2	+38 -5
10											+10 -10	*	+2 -20 Note 3	+38 -10
11												+1 -5	+2 -30 Note 3	+38 -10
12													+1 -30 Note 2	+38 -5
13														*
14														Substrate

TERMINAL No.	I _{IN} mA	I _{OUT} mA
1	5	5
2	20	-
3	50	50
4	10	10
5	5	5
6	-	-
7	5	5
8	1	1
9	1	0.1
10	1	0.1
11	1	0.1
12	1	0.1
13	1	1
14	-	-

- Notes: 1 - This rating applies to the more positive terminal of terminals 8 and 13.
2 - This rating applies to the more positive terminal of terminals 9 and 12.
3 - This rating applies to the more positive terminal of terminals 10 and 11.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

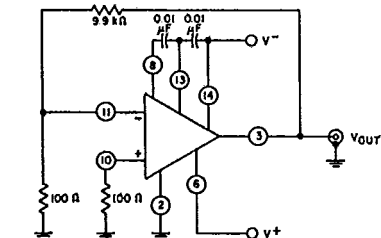
ELECTRICAL CHARACTERISTICS

Characteristics	Symbols	Test Conditions			LIMITS			Units
		Circuit	T _A = 25° C	Typical Characteristics Curves	DC Supply Voltage V ⁺ = 15 V V ⁻ = -15 V			
					Fig.	Fig.	Min.	
Input Offset Voltage	V _{IO}	2a		2b	—	2.9	5	mV
Input Offset Current	I _{IO}	3a		3b	—	9	25	nA
Input Bias Current	I _I	3a		3c	—	100	180	nA
Input Offset Voltage Sensitivity:								
Positive	ΔV _{IO} /ΔV ⁺	2a		—	—	0.2	0.5	mV/V
Negative	ΔV _{IO} /ΔV ⁻	2a		—	—	0.2	0.5	mV/V
Device Dissipation	P _T	2a		—	80	170	300	mW
Open-Loop Differential Voltage Gain	A _{OL}	—	f = 1 kHz	4	87	93	—	dB
Common-Mode Rejection Ratio	CMRR	—		5	93	105	—	dB
Common-Mode Input-Voltage Range	V _{ICR}	—		—	-9.7	6, -11	4.7	V
Maximum Output-Voltage Swing	V _O (P-P)	—	f = 1 kHz	R _L = 500 Ω R _L = 300 Ω	— 23	— 25	—	V _{P-P}
Input Impedance	Z _I	—		—	0.6	1	—	MΩ
Output Current	I _O	—		R _L = 500 Ω R _L = 300 Ω	— 76	— 83	—	mA- (P-P)
Power Output THD < 5%	P _c	—		R _L = 500 Ω R _L = 300 Ω	— 220	— 255	—	mW

ELECTRICAL CHARACTERISTICS

Typical Values

Input Offset Voltage Drift -55°C to 125°C	VI0ΔT	2a		2b	—	6.6	—	μV/ °C
Input Offset Current Drift -55°C to 25°C	II0ΔT	3a		3b	—	1	—	nA/ °C
25°C to 125°C					—	0.03	—	
60 dB Amplifier Bandwidth	BW	8a	CX, CY = 0.001 μF	8b c	350			kHz
Slew Rate	SR	9	(amplifier circuit only)	—	—	3	—	V/μs



PROCEDURE:
INPUT OFFSET VOLTAGE: MEASURE V_{OUT} AND RECORD INPUT
OFFSET VOLTAGE (V_{IO}) IN VOLTS AS $V_{OUT}/100$, THUS
 V_{IO} (IN VOLTS) = $\frac{V_{OUT}}{100}$

Fig. 2a - Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.

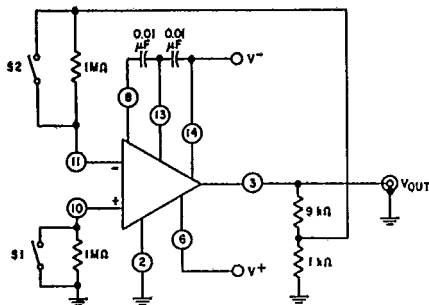


Fig. 3a - Input offset current and input bias current test circuit.

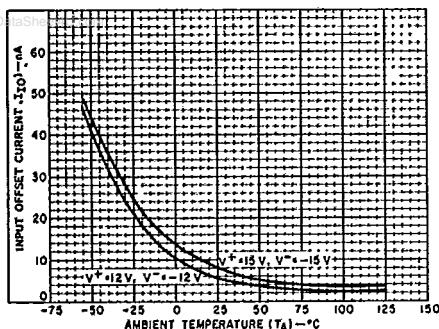


Fig. 3b - Typical input offset current vs. ambient temperature.

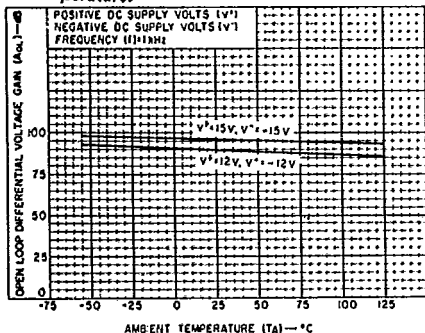


Fig. 4 - Typical open-loop differential voltage gain vs. ambient temperature.

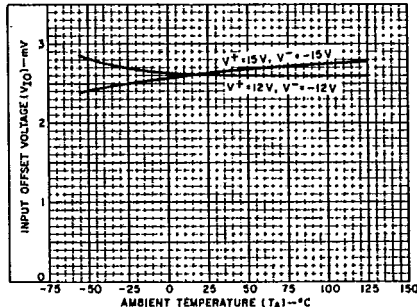


Fig. 2b - Typical input offset voltage vs. ambient temperature.

PROCEDURES:

A. Inverting Input Current

Set switch, S_1 in closed position and set switch, S_2 in open position.
Measure output voltage and convert this reading to inverting input current using the following relation:

$$I_I \text{ inverting (in } \mu\text{A)} = \frac{V_{OUT} \text{ (in volts)}}{10}$$

B. Non-inverting Input Current

Set switch, S_1 in open position and set switch, S_2 in closed position.
Measure output voltage and convert this reading to non-inverting input current using the following relation:

$$I_I \text{ non-inverting (in } \mu\text{A)} = \frac{-V_{OUT} \text{ (in volts)}}{10}$$

C. Input Offset Current

Set switches, S_1 and S_2 in open positions.
Measure output voltage and convert this reading to input offset current using the following relation:

$$I_{IO} \text{ (in } \mu\text{A)} = \frac{V_{OUT} \text{ (in volts)}}{10}$$

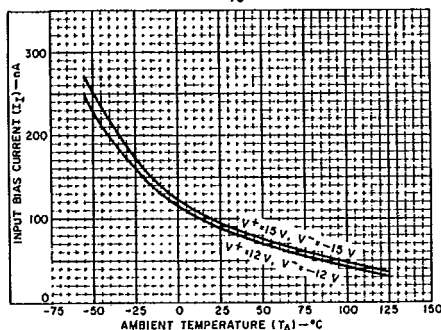


Fig. 3c - Typical input bias current vs. ambient temperature.

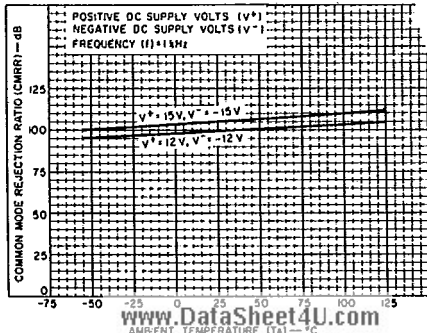


Fig. 5 - Typical common mode rejection ratio vs. ambient temperature.

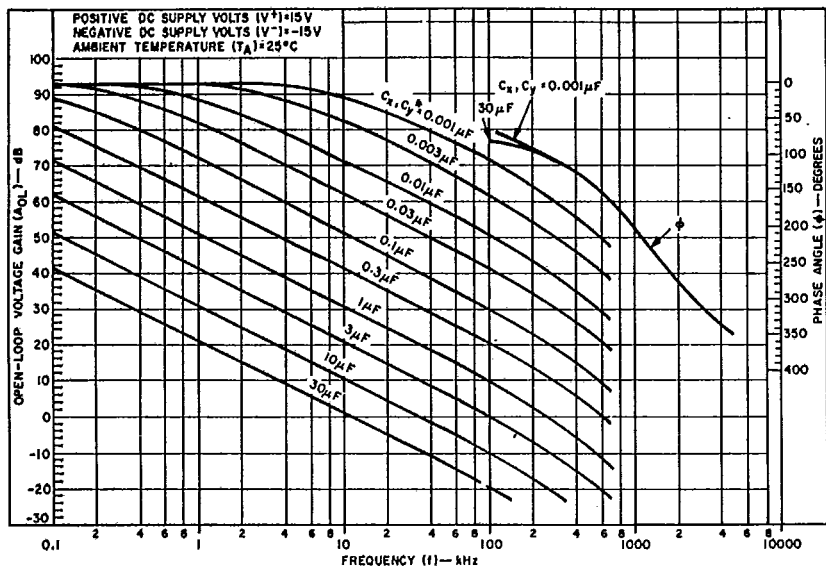


Fig. 8b - Typical phase compensation characteristics for ECG913 ($V^+ = 15\text{ V}$, $V^- = -15\text{ V}$).

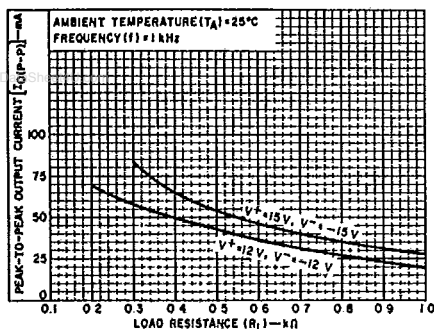


Fig. 6 - Typical peak-to-peak output current vs. load resistance.

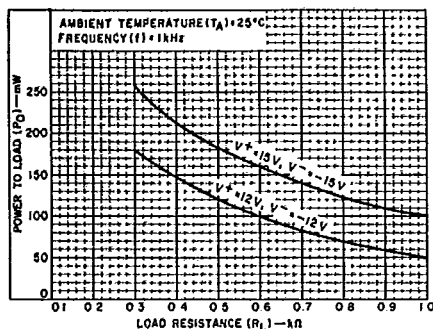


Fig. 7 - Typical power output vs. load resistance.

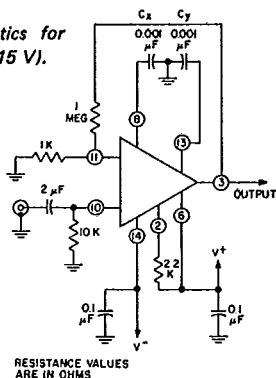


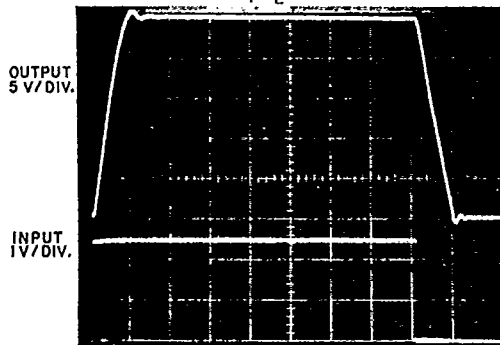
Fig. 8a - Typical 60-dB amplifier.

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network. As the closed loop gain approaches unity, the compensating capacitors required ($0.3\text{ }\mu\text{F}$

to $1.0\text{ }\mu\text{F}$) are bulky and costly. A capacitor one-half the value shown on the chart, connected between (terminals 8 and 13, and a $0.001\text{ }\mu\text{F}$ capacitor from either terminals 8 or 13 to ground or V^- is an acceptable alternative method. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of more readily available, lower-voltage disc capacitors which are smaller and cost less. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

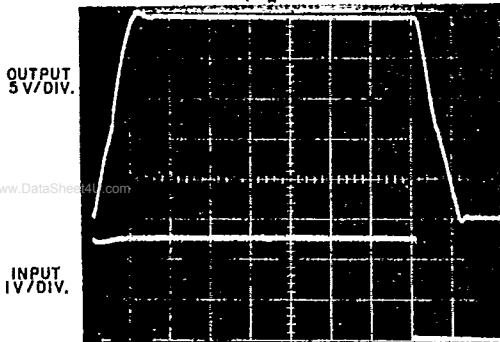
Figure 8a shows the amplifier circuit. The output is returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V^-) supply may result in more stable operation.

$$V^+ = 30\text{ V}, R_L = \infty$$

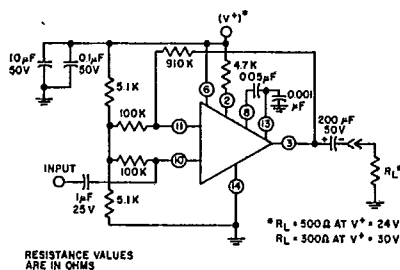
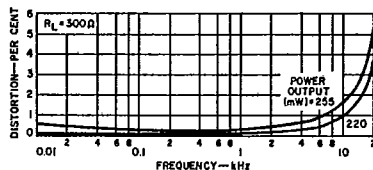


TIME—10 μ s/DIV,
(a)

$$V^+ = 30\text{ V}, R_L = 1\text{ k}\Omega$$



TIME—10 μ s/DIV,
(b)



RESISTANCE VALUES
ARE IN OHMS

Fig. 9 - Amplifier with single voltage supply and associated pulse response waveforms and distortion curves.

OPERATING CONSIDERATIONS The ECG913 operational amplifier has a very high peak-pulse current capability. The open-loop output impedance is typically less than 30 ohms at 10 kHz and the peak short circuit output current may exceed 100 milliamperes. To prevent possible damage to the chip because of excessive dissipation it is important that the output stage is not subjected to sustained high peak currents. To minimize the possibility of damage from accidental shorts, it is recommended that a 51-ohm

resistor be placed in series with the output circuit.

When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q14. This resistor may be increased to 4700 ohms; if its value is increased to 4700 ohms, it may be returned to the V^+ terminal.