ULTRA- LOW ON RESISTANCE, 6A LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated 6A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low ON-Resistance R_{ON} = 4.5mΩ (VBAIS=5V, VIN=1.05V)
- Low Threshold Control Input
- Quick Output Discharge Transistor
- Halogen Free Product

APPLICATIONS

- Telecom Systems
- Industrial Systems
- Consumer Electronics
- Notebooks / Netbooks

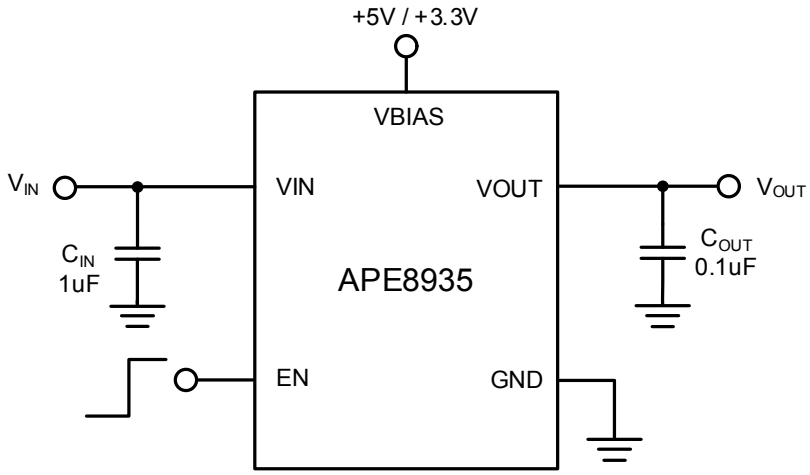
DESCRIPTION

The APE8935 is a small, ultra-low R_{ON} load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 6A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 330Ω on-chip load resistor is added for output quick discharge when switch is turned off.

The APE8935 is available in 8-pin DFN 3x3-8L package with smallest components.

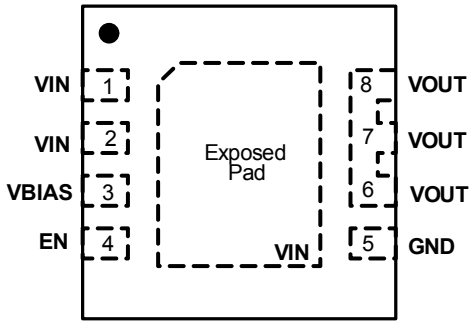
TYPICAL APPLICATION



ORDERING / PACKAGE INFORMATION

APE8935X
└ Package Type
GN3: DFN 3x3-8L

Top View
DFN 3x3-8L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN	-0.3V to 6V
VOUT	VIN+0.3V
EN	-0.3V to 6V
VBIAS	-0.3 to 6V
I_{MAX}	6A
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
DFN 3x3-8L	43°C/W

RECOMMENDED OPERATING CONDITIONS

VIN	0.8V to 5.5V
VBIAS	2.5V to 5.5V (VBIAS≧VIN)
VOUT	V_{IN}
CIN	≧0.1uF
Junction Temperature (T_J)	125°C
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(V_{IN}=0.8V to 5.5V, V_{BIAS}=5V, C_{IN}=1uF, C_{OUT}=0.1uF, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	V_{BIAS}=V_{EN}=5V, V_{IN}=1.05V, I_{OUT}=0A			30	50	uA
		V_{BIAS}=V_{EN}=5V, V_{IN}=1.5V, I_{OUT}=0A			30	50	uA
Shutdown Current	I_{SD}	V_{EN}=GND				1	uA
ON Resistance(Note1)	R_{ON}	V_{BIAS}=V_{EN}=5V, V_{IN}=1.05V, I_{OUT}=200mA	T_A=25°C		4.5	5	mΩ
			-40~85°C(NOTE1)		5.5	6	
		V_{BIAS}=V_{EN}=5V, V_{IN}=1.5V, I_{OUT}=200mA	T_A=25°C		4.5	5	mΩ
			-40~85°C(NOTE1)		5.5	6	
Output Pull-Down Resistance	R_{OPD}	V_{IN}=5V, V_{EN}=0V			330	400	Ω
EN Input Leakage Current	I_{EN}	V_{EN}=5V or GND				1	uA
EN Threshold	V_{IH}	on		1.3			V
	V_{IL}	off				0.5	V

Note1: Make sure $V_{BAIS} \geqq V_{IN}$ for optimum R_{ON} performance.

SWITCHING SPECIFICATIONS

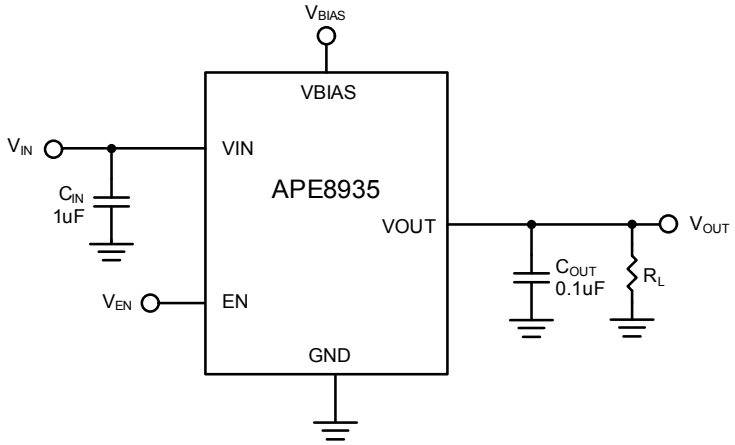


Fig.1 Test Circuit

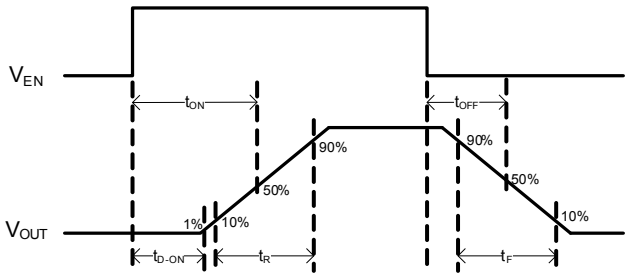


Fig.2 ON/OFF Waveforms

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Turn-on Time	t_{ON}	V_{BIAS}=V_{EN}=5V, R_L=10Ω	V_{IN}=1.05V		905		us
			V_{IN}=1.5V		940		us
Turn-off Time	t_{OFF}	V_{BIAS}=V_{EN}=5V, R_L=10Ω	V_{IN}=1.05V		5.4		us
			V_{IN}=1.5V		5.2		us
VOUT Rise Time	t_R	V_{BIAS}=V_{EN}=5V, R_L=10Ω	V_{IN}=1.05V	308	440	572	us
			V_{IN}=1.5V	381	545	708	us
VOUT Fall Time	t_F	V_{BIAS}=V_{EN}=5V, R_L=10Ω	V_{IN}=1.05V		1.7		us
			V_{IN}=1.5V		1.8		us
VOUT Turn-on Delay Time	t_{D-ON}	V_{BIAS}=V_{EN}=5V, R_L=10Ω	V_{IN}=1.05V	388	555	721	us
			V_{IN}=1.5V	381	545	708	us

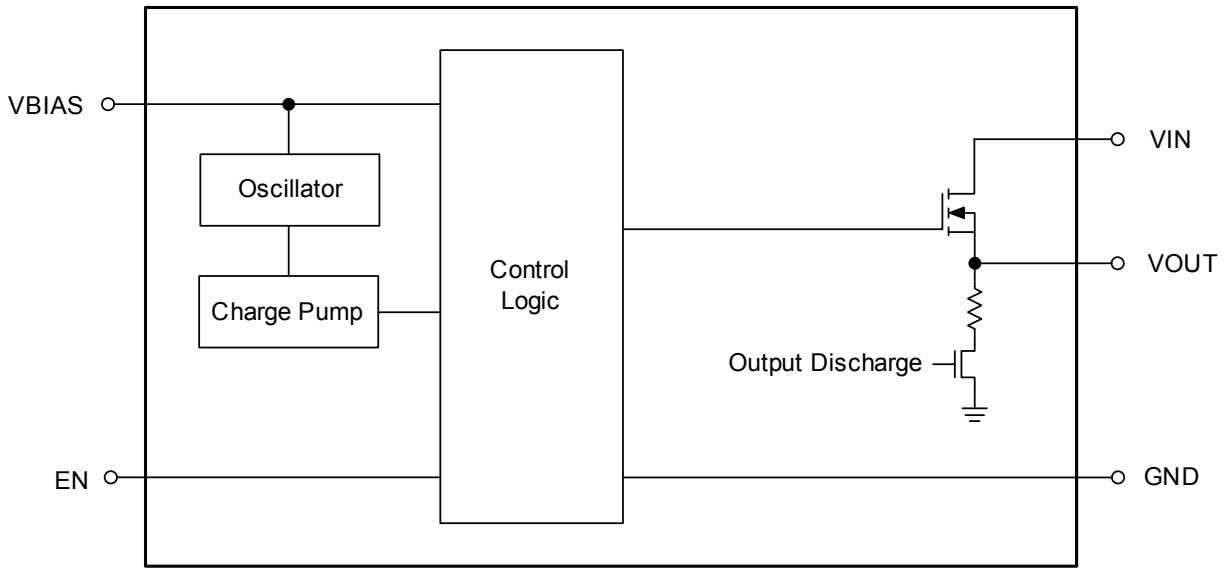
SWITCHING SPECIFICATIONS (Continued)

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Turn-on Time	t_{ON}	V_{BIAS}=V_{EN}=5V, I_{OUT}=6A	V_{IN}=1.05V		1345		us
			V_{IN}=1.5V		1480		us
Turn-off Time	t_{OFF}	V_{BIAS}=V_{EN}=5V, I_{OUT}=6A	V_{IN}=1.05V		4.8		us
			V_{IN}=1.5V		4.8		us
VOUT Rise Time	t_R	V_{BIAS}=V_{EN}=5V, I_{OUT}=6A	V_{IN}=1.05V	602	860	1118	us
			V_{IN}=1.5V	616	880	1144	us
VOUT Fall Time	t_F	V_{BIAS}=V_{EN}=5V, I_{OUT}=6A	V_{IN}=1.05V		0.5		us
			V_{IN}=1.5V		0.7		us
VOUT Turn-on Delay Time	t_{D-ON}	V_{BIAS}=V_{EN}=5V, I_{OUT}=6A	V_{IN}=1.05V	497	710	923	us
			V_{IN}=1.5V	495	708	920	us

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN	Input Power Supply
3	VBIAS	Bias Voltage
4	EN	Switch control input, active high. Do not leave floating.
5	GND	Ground
6, 7, 8	VOUT	Switch output
Exposed pad	VIN	Input Power Supply

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Condition: VBIAS=VEN=5V, RL=10Ω, Cin=1uF, Cout=0.1uF, ch1:EN, ch2:VOUT, ch4:I_{IN}

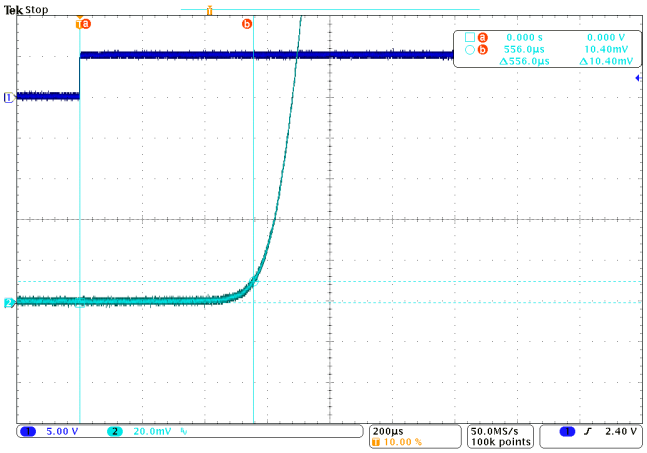


Fig.1 Waveform for t_{D-ON}, VIN=1.05V

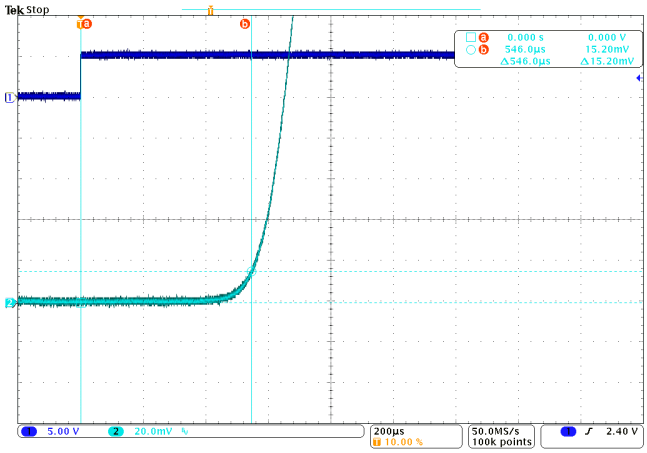


Fig.2 Waveform for t_{D-ON}, VIN=1.5V

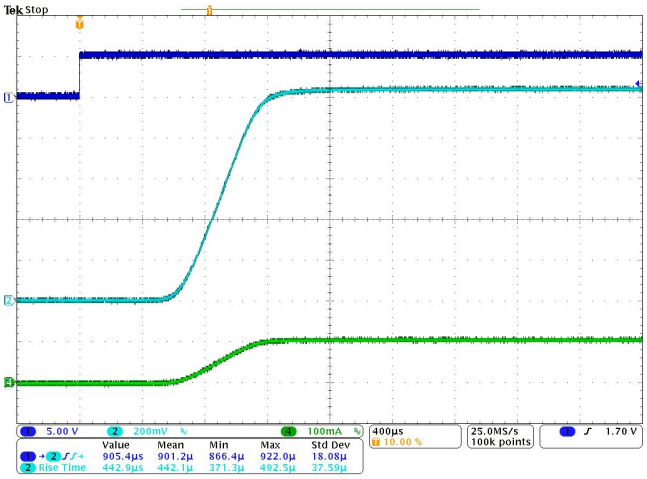


Fig.3 Waveform for t_{ON} and t_R, VIN=1.05V

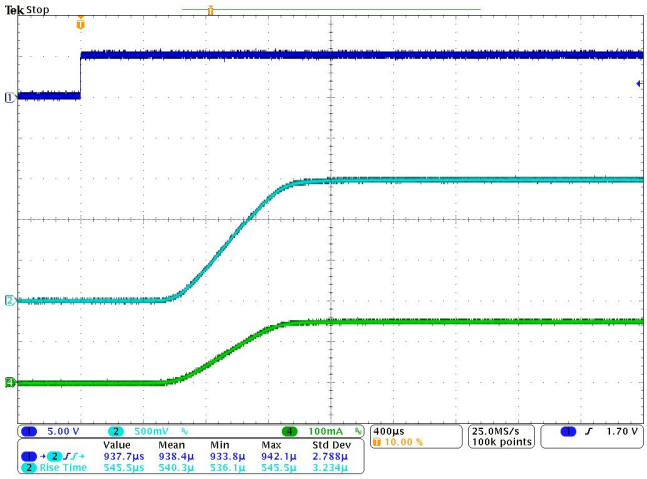


Fig.4 Waveform for t_{ON} and t_R, VIN=1.5V

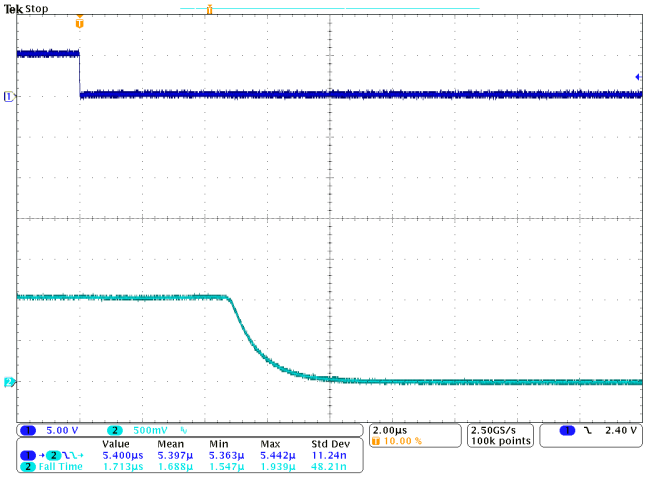


Fig.5 Waveform for t_{OFF} and t_F, VIN=1.05V

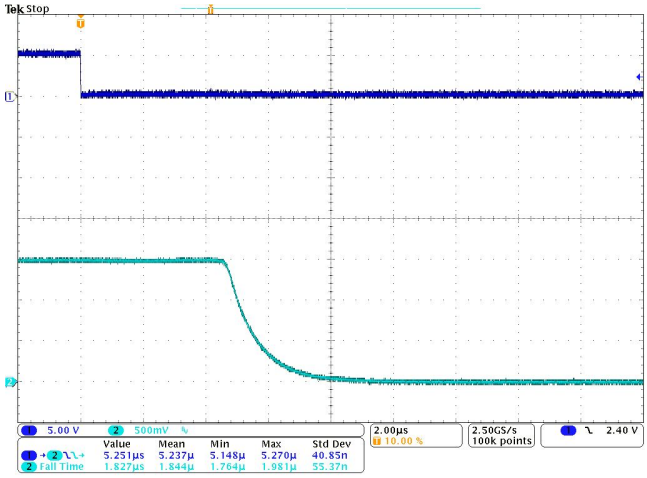


Fig.6 Waveform for t_{OFF} and t_F, VIN=1.5V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: VBIAS=VEN=5V, IOUT=6A, Cin=1uF, Cout=0.1uF, ch1:EN, ch2:VOUT, ch4:I_{IN}

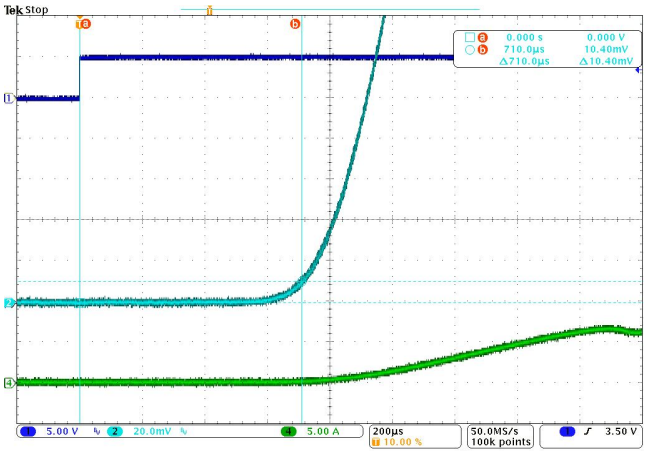


Fig.7 Waveform for t_{D-ON}, VIN=1.05V

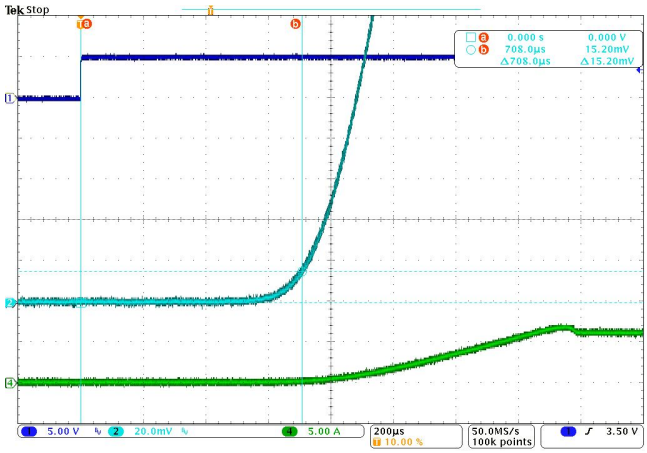


Fig.8 Waveform for t_{D-ON}, VIN=1.5V

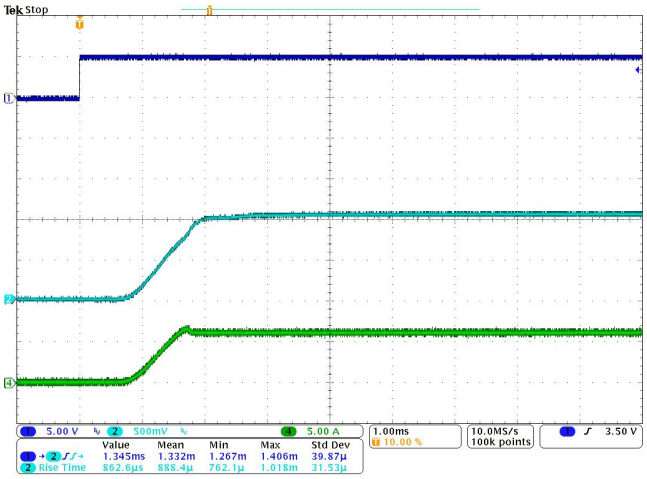


Fig.9 Waveform for t_{ON} and t_R, VIN=1.05V

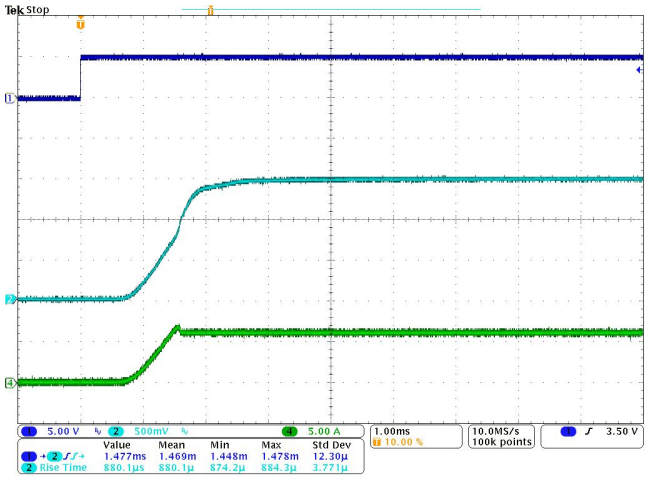


Fig.10 Waveform for t_{ON} and t_R, VIN=1.5V

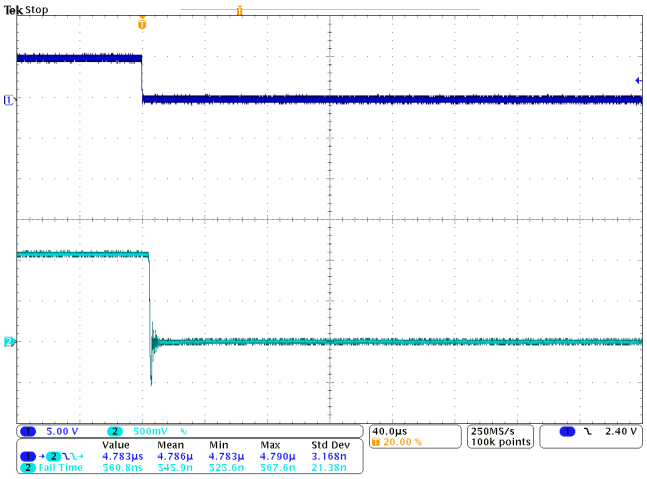


Fig.11 Waveform for t_{OFF} and t_F, VIN=1.05V

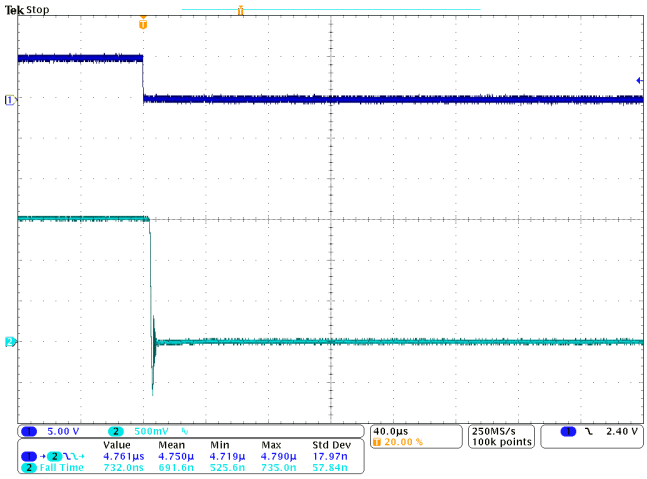


Fig.12 Waveform for t_{OFF} and t_F, VIN=1.5V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

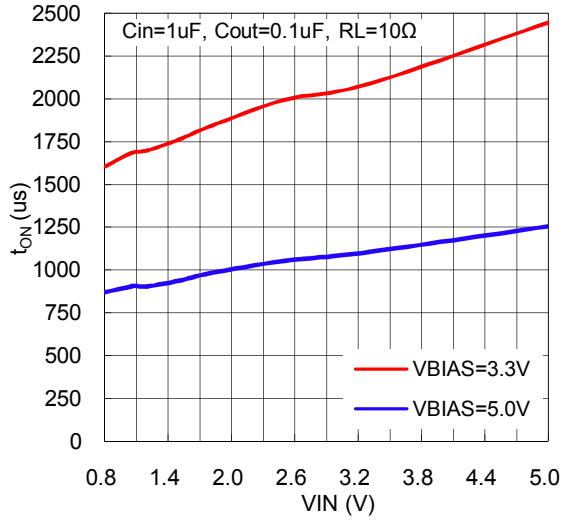


Fig.13 t_{ON} vs. VIN

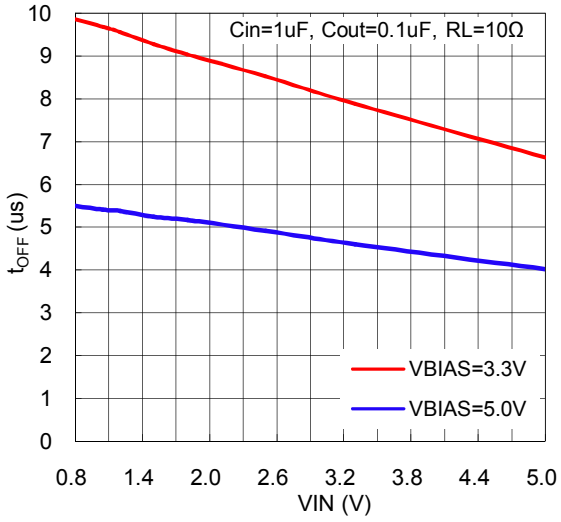


Fig.14 t_{OFF} vs. VIN

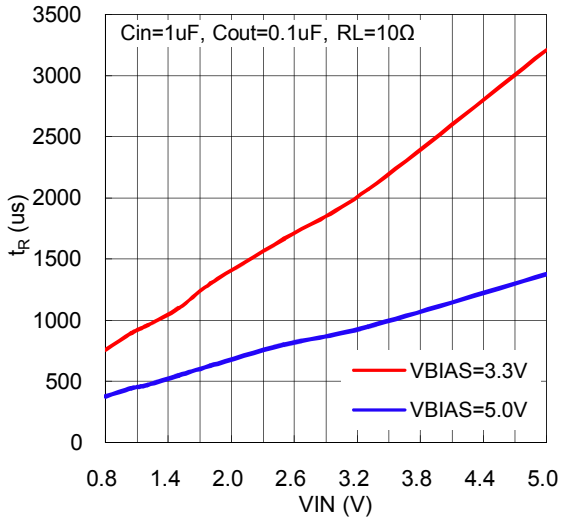


Fig.15 t_R vs. VIN

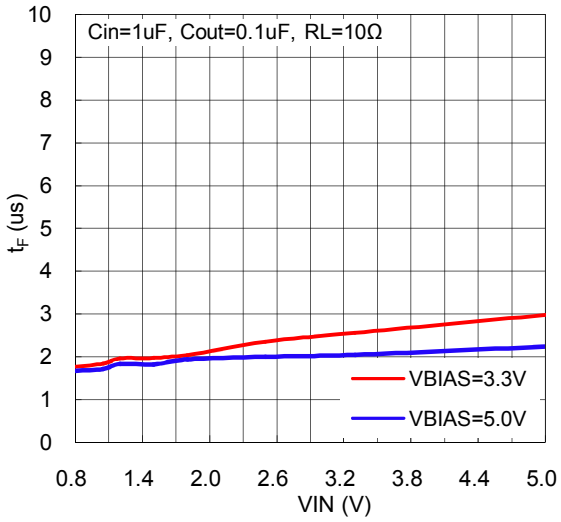


Fig.16 t_F vs. VIN

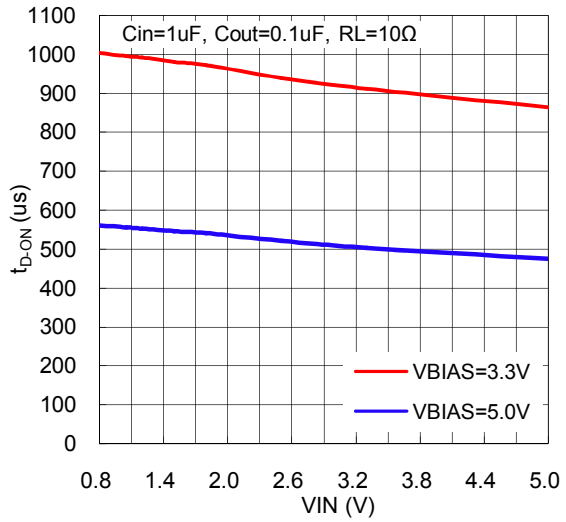


Fig.17 $t_{D\text{-}ON}$ vs. VIN

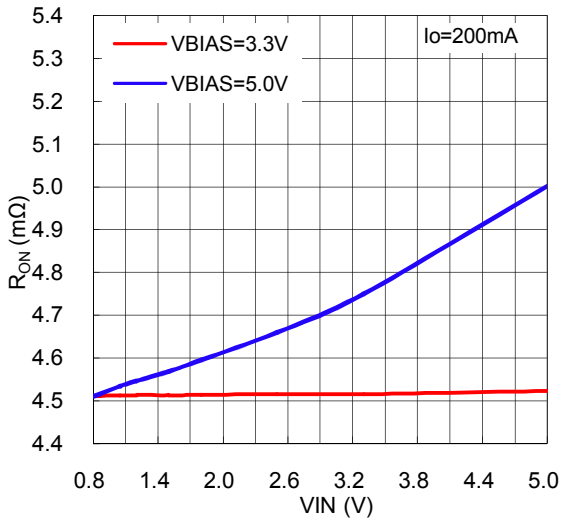


Fig.18 R_{ON} vs. VIN

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

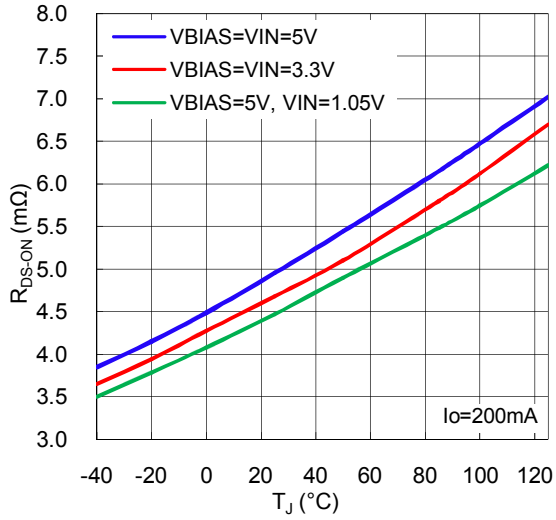


Fig.19 R_{ON} vs. Temperature

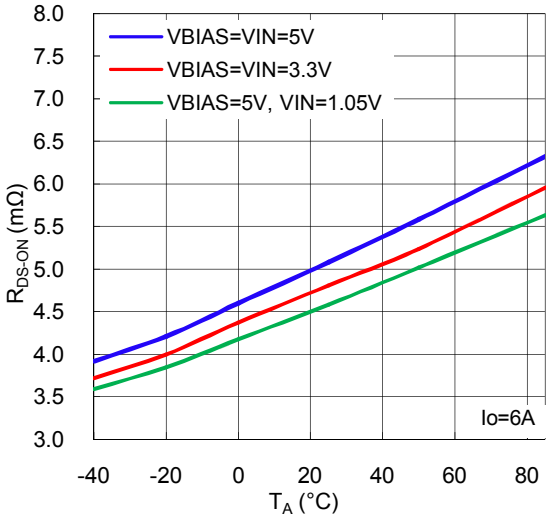


Fig.20 R_{ON} vs. Temperature

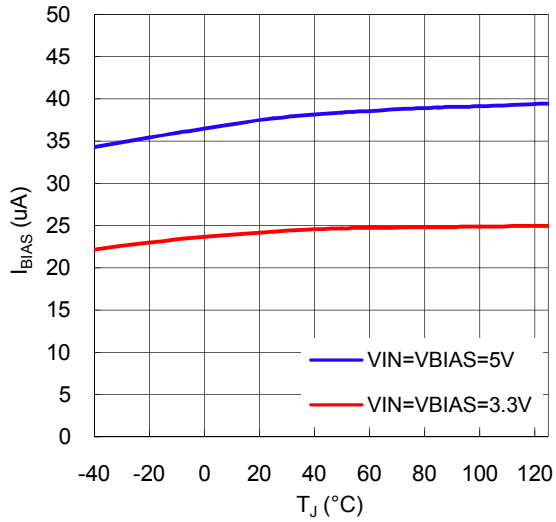


Fig.21 Quiescent Current vs. Temperature

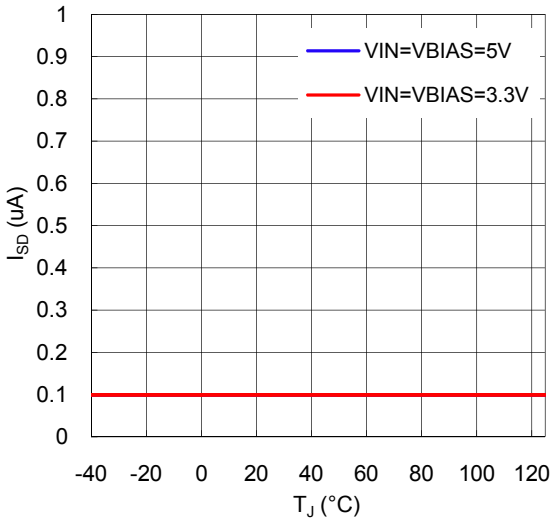


Fig.22 Shutdown Current vs. Temperature

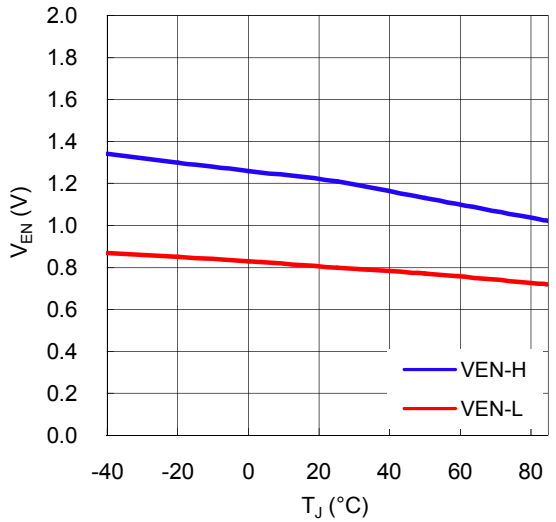


Fig.23 EN Threshold vs. Temperature

APPLICATION INFORMATION

On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.5V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

Layout Considerations

Follow the below guidelines for PCB layout to achieve stable operation. Take below figure for reference.

1. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
2. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.
3. Place the thermal vias under the exposed pad. This help for thermal diffusion away from the device.

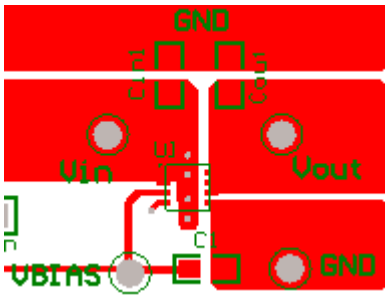


Fig.24 Reference layout

MARKING INFORMATION

DFN 3x3-8L