PCA9952/Q900; PCA9955/Q900

16-channel Fm+ I²C-bus 57 mA constant current LED driver, AEC-Q100 compliant

Rev. 1 — 26 April 2013 Product data sheet

1. General description

The PCA9952/Q900 and PCA9955/Q900 are I²C-bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LEDn output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LEDn output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9952/Q900 and PCA9955/Q900 operate with a supply voltage range of 3 V to 5.5 V and the constant current sink LEDn outputs allow up to 40 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

These devices have built-in open, short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the I²C-bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9952/Q900 and PCA9955/Q900 devices have Fast-mode Plus (Fm+) I²C-bus interface. Fm+ devices offer higher frequency (up to 1 MHz) or more densely populated bus operation (up to 4000 pF).

The PCA9952/Q900 is identical to PCA9955/Q900 except for the following differences:

- The PCA9952/Q900 has only three hardware address pins compared to four on PCA9955/Q900.
- The PCA9952/Q900 has an output enable pin ($\overline{OE}$) and the PCA9955/Q900 does not.

The active LOW output enable input pin ($\overline{OE}$), available only on PCA9952/Q900, blinks all the LEDn outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCA9952/Q900, PCA9955/Q900 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. On power-up, PCA9952/Q900, PCA9955/Q900 will have a unique Sub Call address to identify it as a 16-channel LED driver. This allows mixing of devices with different channel widths. Four

hardware address pins on PCA9955/Q900 allow up to 16 devices on the same bus. In the case of PCA9952/Q900, three hardware address pins allow up to 8 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCA9952/Q900, PCA9955/Q900 through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- Compliant with AEC-Q100
- 16 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LEDn output enable delay to reduce EMI and surge currents
- 16 constant current output channels can sink up to 57 mA, tolerate up to 40 V when OFF
- Output current adjusted through an external resistor
- Output current accuracy
  - ±6 % between output channels
  - ±8 % between PCA9952/Q900, PCA9955/Q900 devices
- Open/short load/overtemperature detection mode to detect individual LED errors
- 1 MHz Fast-mode Plus compatible I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LEDn output varying from fully off (default) to maximum brightness using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to ‘Change on STOP’).
- Active LOW Output Enable ($\overline{OE}$) input pin (only on PCA9952/Q900) allows for hardware blinking and dimming of the LEDs
- Four hardware address pins allow 16 PCA9955/Q900 devices to be connected to the same I²C-bus and to be individually programmed
- Four software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for ‘All Call’ so that all the PCA9952/Q900, PCA9955/Q900s on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that ⅓ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.

- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- No glitch on LED on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 500 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level B
- Packages offered: HTSSOP28

3. Applications

- Automotive lighting
- Single-string LED (white, RGB, or RGBA) display or backlight
- LED status information

4. Ordering information

Table 1. Ordering information

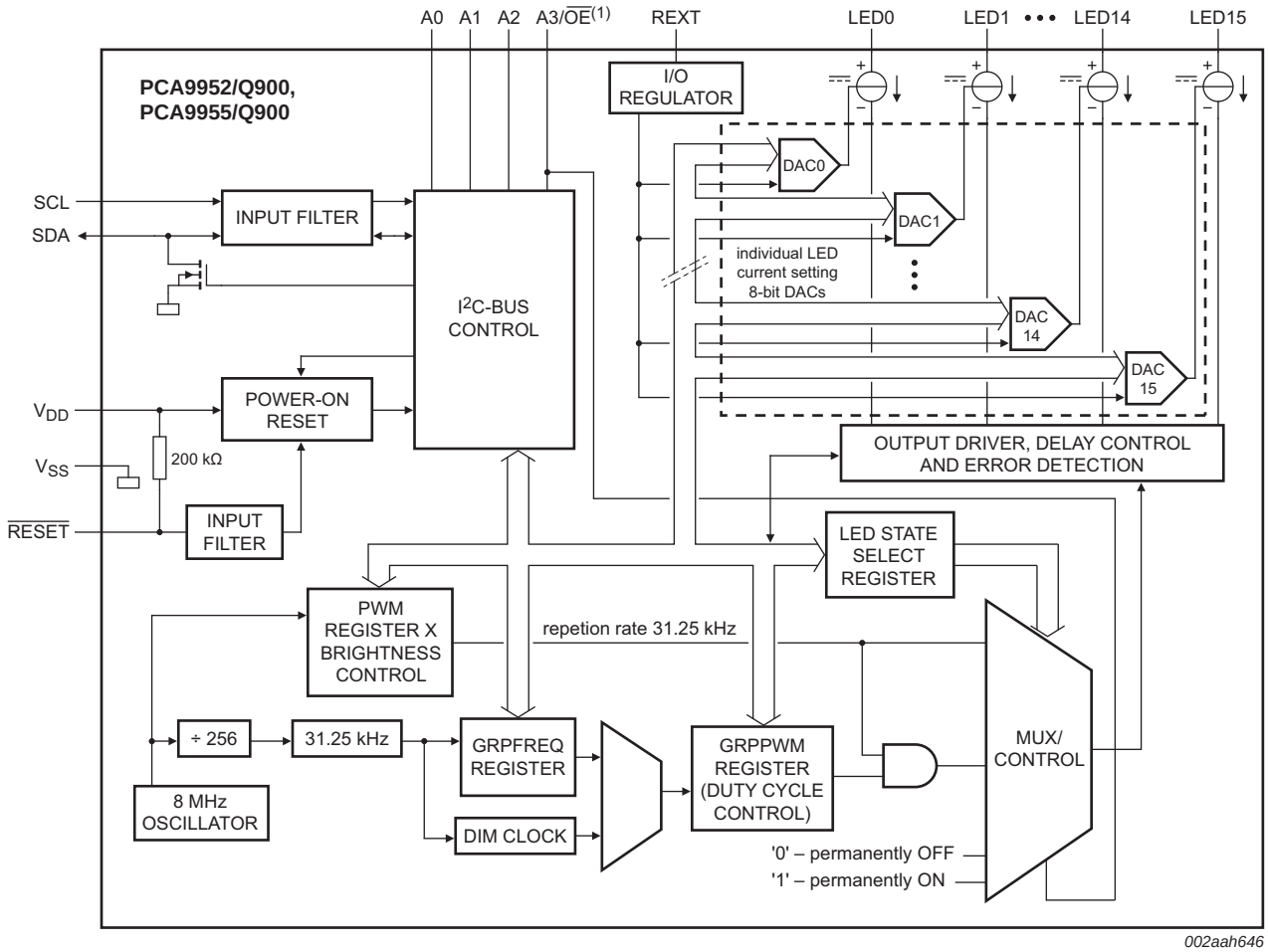
Type number	Topside marking	Package		
		Name	Description	Version
PCA9952TW/Q900	PCA9952	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-2
PCA9955TW/Q900	PCA9955	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-2

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9952TW/Q900	PCA9952TW/Q900,118	HTSSOP28	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9955TW/Q900	PCA9955TW/Q900,118	HTSSOP28	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram



Dim repetition rate = 122 Hz.

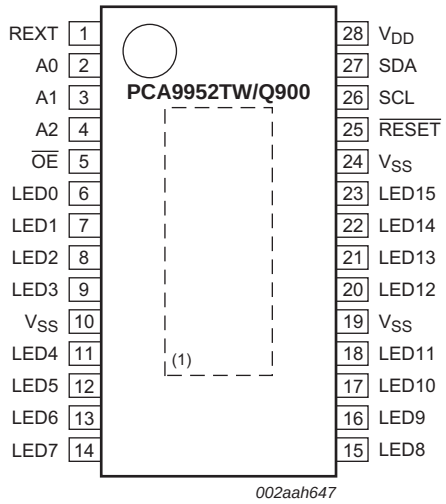
Blink repetition rate = 15 Hz to every 16.8 seconds.

(1) On PCA9955/Q900 this pin is address pin A3. On PCA9952/Q900 this pin is $\overline{OE}$.

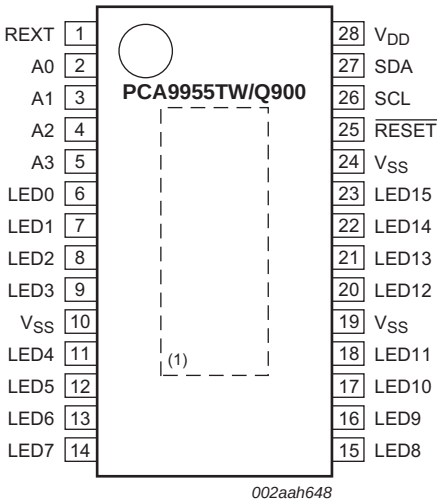
Fig 1. Block diagram of PCA9952/Q900, PCA9955/Q900

6. Pinning information

6.1 Pinning



a. PCA9952/Q900



b. PCA9955/Q900

(1) Thermal pad; connected to V_{SS}.

Fig 2. Pin configuration for HTSSOP28

6.2 Pin description

Table 3. PCA9955/Q900 pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
A0	2	I	address input 0[1]
A1	3	I	address input 1[1]
A2	4	I	address input 2[1]
A3	5	I	address input 3[1]
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12
LED13	21	O	LED driver 13
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{\text{RESET}}$	25	I	active LOW reset input
SCL	26	I	serial clock line
SDA	27	I/O	serial data line
V_{SS}	10, 19, 24[2]	ground	supply ground
V_{DD}	28	power supply	supply voltage

[1] In order to obtain the best system level ESD performance, a standard pull-up resistor (10 kΩ typical) is required for any address pin connecting to V_{DD}. For additional information on system level ESD performance, please refer to application notes AN10897 and AN11131.

[2] HTSSOP28 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

Table 4. PCA9952/Q900 pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
A0	2	I	address input 0[1]
A1	3	I	address input 1[1]
A2	4	I	address input 2[1]
$\overline{OE}$	5	I	active LOW output enable
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12
LED13	21	O	LED driver 13
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{RESET}$	25	I	active LOW reset input
SCL	26	I	serial clock line
SDA	27	I/O	serial data line
V_{SS}	10, 19, 24[2]	ground	supply ground
V_{DD}	28	power supply	supply voltage

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7. Functional description

Refer to Figure 1 “Block diagram of PCA9952/Q900, PCA9955/Q900”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCA9955/Q900 there are a maximum of 16 possible programmable addresses using the 4 hardware address pins.

For PCA9952/Q900 there are a maximum of 8 possible programmable addresses using the 3 hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCA9955/Q900 is shown in Figure 3. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW externally. Figure 4 shows the I²C-bus slave address of the PCA9952/Q900.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

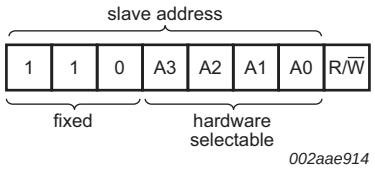


Fig 3. PCA9955/Q900 slave address

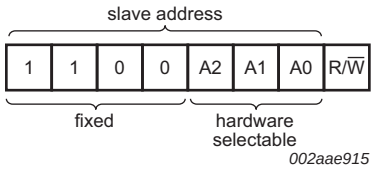


Fig 4. PCA9952/Q900 slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled. PCA9952/Q900, PCA9955/Q900 sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.10 “ALLCALLADR, LED All Call I²C-bus address” for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCA9952/Q900, PCA9955/Q900s on the I²C-bus will acknowledge the address if sent by the I²C-bus master.

7.1.3 LED bit Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: ECh or 1110 110X
  - SUBADR2 register: ECh or 1110 110X
  - SUBADR3 register: ECh or 1110 110X
- Programmable through I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 16-channel driver.

See Section 7.3.9 “LED bit Sub Call I²C-bus addresses for PCA9952/Q900, PCA9955/Q900” for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9952/Q900, PCA9955/Q900, which will be stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register will be accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF). The AIF is active by default at power-up.

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 5. Control register

When the Auto-Increment Flag is set (AIF = logic 1), the seven low-order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 5. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 41h). D[6:0] roll over to 00h after the last register 41h is accessed.
1	0	1	Auto-Increment for individual brightness registers only (0Ah to 19h). D[6:0] roll over to 0Ah after the last register (19h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF15 control registers (00h to 31h). D[6:0] roll over to 00h after the last register (31h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (08h to 19h). D[6:0] roll over to 08h after the last register (19h) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 5 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF15 registers must be programmed with different settings during the same I²C-bus communication.

AIF + AI[1:0] = 111b is used when the 16 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that will be addressed (read or write operation), and can be anywhere between 00h and 41h (as defined in Table 6). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 5 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence will be (in hexadecimal):
10 → 11 → … → 19 → 0A → 0B → … → 19 → 0A → 0B → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 0 and if the Control register = 1010 0010, then the register addressing sequence will be (in hexadecimal):
22 → 23 → … → 41 → 00 → 01 → … → 19 → 0A → 0B → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence will be (in hexadecimal):
05 → 06 → … → 19 → 0A → 0B → … → 19 → 0A → 0B → … as long as the master keeps sending or reading data.

Remark: Writing to registers marked 'not used' will return NACK.

7.3 Register definitions

Table 6. Register summary[1]

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	read/write	LEDn output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	read/write	LEDn output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	read/write	LEDn output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	read/write	LEDn output state 3
06h	0	0	0	0	1	1	0	-	read/write	not used[1]
07h	0	0	0	0	1	1	1	-	read/write	not used[1]
08h	0	0	0	1	0	0	0	GRPPWM	read/write	group duty cycle control
09h	0	0	0	1	0	0	1	GRPFREQ	read/write	group frequency
0Ah	0	0	0	1	0	1	0	PWM0	read/write	brightness control LED0
0Bh	0	0	0	1	0	1	1	PWM1	read/write	brightness control LED1
0Ch	0	0	0	1	1	0	0	PWM2	read/write	brightness control LED2
0Dh	0	0	0	1	1	0	1	PWM3	read/write	brightness control LED3
0Eh	0	0	0	1	1	1	0	PWM4	read/write	brightness control LED4
0Fh	0	0	0	1	1	1	1	PWM5	read/write	brightness control LED5
10h	0	0	1	0	0	0	0	PWM6	read/write	brightness control LED6
11h	0	0	1	0	0	0	1	PWM7	read/write	brightness control LED7
12h	0	0	1	0	0	1	0	PWM8	read/write	brightness control LED8
13h	0	0	1	0	0	1	1	PWM9	read/write	brightness control LED9
14h	0	0	1	0	1	0	0	PWM10	read/write	brightness control LED10
15h	0	0	1	0	1	0	1	PWM11	read/write	brightness control LED11
16h	0	0	1	0	1	1	0	PWM12	read/write	brightness control LED12
17h	0	0	1	0	1	1	1	PWM13	read/write	brightness control LED13
18h	0	0	1	1	0	0	0	PWM14	read/write	brightness control LED14
19h	0	0	1	1	0	0	1	PWM15	read/write	brightness control LED15
1Ah to 21h	-	-	-	-	-	-	-	-	read/write	not used[1]
22h	0	1	0	0	0	1	0	IREF0	read/write	output gain control register 0
23h	0	1	0	0	0	1	1	IREF1	read/write	output gain control register 1
24h	0	1	0	0	1	0	0	IREF2	read/write	output gain control register 2
25h	0	1	0	0	1	0	1	IREF3	read/write	output gain control register 3
26h	0	1	0	0	1	1	0	IREF4	read/write	output gain control register 4

Table 6. Register summary[1] *…continued*

Register number (hexadecimal)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
27h	0	1	0	0	1	1	1	IREF5	read/write	output gain control register 5
28h	0	1	0	1	0	0	0	IREF6	read/write	output gain control register 6
29h	0	1	0	1	0	0	1	IREF7	read/write	output gain control register 7
2Ah	0	1	0	1	0	1	0	IREF8	read/write	output gain control register 8
2Bh	0	1	0	1	0	1	1	IREF9	read/write	output gain control register 9
2Ch	0	1	0	1	1	0	0	IREF10	read/write	output gain control register 10
2Dh	0	1	0	1	1	0	1	IREF11	read/write	output gain control register 11
2Eh	0	1	0	1	1	1	0	IREF12	read/write	output gain control register 12
2Fh	0	1	0	1	1	1	1	IREF13	read/write	output gain control register 13
30h	0	1	1	0	0	0	0	IREF14	read/write	output gain control register 14
31h	0	1	1	0	0	0	1	IREF15	read/write	output gain control register 15
32h to 39h	-	-	-	-	-	-	-	-	read/write	not used[1]
3Ah	0	1	1	1	0	1	0	OFFSET	read/write	Offset/delay on LEDn outputs
3Bh	0	1	1	1	0	1	1	SUBADR1	read/write	I²C-bus subaddress 1
3Ch	0	1	1	1	1	0	0	SUBADR2	read/write	I²C-bus subaddress 2
3Dh	0	1	1	1	1	0	1	SUBADR3	read/write	I²C-bus subaddress 3
3Eh	0	1	1	1	1	1	0	ALLCALLADR	read/write	All Call I²C-bus address
3Fh	0	1	1	1	1	1	1	RESERVED1	read/write	reserved[2]
40h	1	0	0	0	0	0	0	RESERVED2	read only	reserved[2]
41h	1	0	0	0	0	0	1	RESERVED3	read only	reserved[2]
42h	1	0	0	0	0	1	0	PWMALL	write only	brightness control for all LEDn
43h	1	0	0	0	0	1	1	IREFALL	write only	output gain control for all registers IREF0 to IREF15
44h	1	0	0	0	1	0	0	EFLAG0	read only	output error flag 0
45h	1	0	0	0	1	0	1	EFLAG1	read only	output error flag 1
46h to 7Fh	-	-	-	-	-	-	-	-	read only	not used[1]

[1] **Remark:** Writing to registers marked ‘not used’ will return a NACK.

[2] **Remark:** Writing to registers marked ‘reserved’ will not change any functionality in the chip.

7.3.1 MODE1 — Mode register 1

Table 7. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	read only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled.
6	AI1	R/W	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 5.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 5.
5	AI0	R/W	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 5.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 5.
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low-power mode. Oscillator off[2].
3	SUB1	R/W	0	PCA9952/Q900; PCA9955/Q900 does not respond to I²C-bus subaddress 1.
			1*	PCA9952/Q900; PCA9955/Q900 responds to I²C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9952/Q900; PCA9955/Q900 does not respond to I²C-bus subaddress 2.
			1	PCA9952/Q900; PCA9955/Q900 responds to I²C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9952/Q900; PCA9955/Q900 does not respond to I²C-bus subaddress 3.
			1	PCA9952/Q900; PCA9955/Q900 responds to I²C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9952/Q900; PCA9955/Q900 does not respond to LED All Call I²C-bus address.
			1*	PCA9952/Q900; PCA9955/Q900 responds to LED All Call I²C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking or dimming is possible when the oscillator is off.

7.3.2 MODE2 — Mode register 2

Table 8. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	O.K.
			1	overtemperature condition
6	FAULTTEST	R/W	0*	LED fault test complete
			1	start fault test
5	DMBLNK	R/W	0*	group control = dimming.
			1	group control = blinking.
4	-	read only	0*	reserved
3	OCH	R/W	0*	outputs change on STOP command
			1	outputs change on ACK

Table 8. MODE2 - Mode register 2 (address 01h) bit description *…continued*

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
2	-	read only	1*	reserved
1	-	read only	0*	reserved
0	-	read only	1*	reserved

7.3.3 LEDOUT0 to LEDOUT3, LED driver output state

Table 9. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	R/W	00*	LED7 output state control
		5:4	LDR6	R/W	00*	LED6 output state control
		3:2	LDR5	R/W	00*	LED5 output state control
		1:0	LDR4	R/W	00*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	R/W	00*	LED11 output state control
		5:4	LDR10	R/W	00*	LED10 output state control
		3:2	LDR9	R/W	00*	LED9 output state control
		1:0	LDR8	R/W	00*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	R/W	00*	LED15 output state control
		5:4	LDR14	R/W	00*	LED14 output state control
		3:2	LDR13	R/W	00*	LED13 output state control
		1:0	LDR12	R/W	00*	LED12 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.4 GRPPWM, group duty cycle control

Table 10. GRPPWM - Group brightness control register (address 08h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
08h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LEDn outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.3.5 GRPFREQ, group frequency

Table 11. GRPFREQ - Group frequency register (address 09h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LEDn outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26}(s) \quad (2)$$

7.3.6 PWM0 to PWM15, individual brightness control

Table 12. PWM0 to PWM15 - PWM registers 0 to 15 (address 0Ah to 19h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
0Bh	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
0Ch	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
0Dh	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
0Eh	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
0Fh	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
10h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
11h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
12h	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
13h	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
14h	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle

Table 12. PWM0 to PWM15 - PWM registers 0 to 15 (address 0Ah to 19h) bit description
…continued

Address	Register	Bit	Symbol	Access	Value	Description
15h	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
16h	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle
17h	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
18h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
19h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LEDn output off) to FFh (99.6 % duty cycle = LEDn output at maximum brightness). Applicable to LEDn outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LEDn output pins.

7.3.7 IREF0 to IREF15, LEDn output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

Table 13. IREF0 to IREF15 - LEDn output gain control registers (address 22h to 31h) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
22h	IREF0	7:0	R/W	00h*	LED0 output current setting
23h	IREF1	7:0	R/W	00h*	LED1 output current setting
24h	IREF2	7:0	R/W	00h*	LED2 output current setting
25h	IREF3	7:0	R/W	00h*	LED3 output current setting
26h	IREF4	7:0	R/W	00h*	LED4 output current setting
27h	IREF5	7:0	R/W	00h*	LED5 output current setting
28h	IREF6	7:0	R/W	00h*	LED6 output current setting
29h	IREF7	7:0	R/W	00h*	LED7 output current setting
2Ah	IREF8	7:0	R/W	00h*	LED8 output current setting
2Bh	IREF9	7:0	R/W	00h*	LED9 output current setting
2Ch	IREF10	7:0	R/W	00h*	LED10 output current setting
2Dh	IREF11	7:0	R/W	00h*	LED11 output current setting
2Eh	IREF12	7:0	R/W	00h*	LED12 output current setting
2Fh	IREF13	7:0	R/W	00h*	LED13 output current setting
30h	IREF14	7:0	R/W	00h*	LED14 output current setting
31h	IREF15	7:0	R/W	00h*	LED15 output current setting

7.3.8 OFFSET — LEDn output delay offset register

Table 14. OFFSET - LEDn output delay offset register (address 3Ah) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Ah	OFFSET	7:4	read only	0000*	not used
		3:0	R/W	1000*	LEDn output delay offset factor

The OFFSET register should not be changed while the LEDn output is on and pulsing.

The PCA9955/Q900 can be programmed to have turn-on delay between LEDn outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LEDn outputs are enabled will always be the same (channel 0 will enable first and channel 15 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

1111 = delay of 15 clock cycles (1.875 μs) between successive outputs

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

channel 14 turns on at time 14 μs

channel 15 turns on at time 15 μs

7.3.9 LED bit Sub Call I²C-bus addresses for PCA9952/Q900, PCA9955/Q900

Table 15. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 1 to 3 (address 3Bh to 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Bh	SUBADR1	7:1	A1[7:1]	R/W	1110 110*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
3Ch	SUBADR2	7:1	A2[7:1]	R/W	1110 110*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
3Dh	SUBADR3	7:1	A3[7:1]	R/W	1110 110*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Default power-up values are ECh, ECh, ECh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of ECh indicates that this device is a 16-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device acknowledging these addresses (MODE1 register) (0). When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.10 ALLCALLADR, LED All Call I²C-bus address

Table 16. ALLCALLADR - LED All Call I²C-bus address register (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
3Eh	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I²C-bus address allows all the PCA9952/Q900, PCA9955/Q900s on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 (power-up default state)). This address is programmable through the I²C-bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.3.11 RESERVED1

This register is reserved.

7.3.12 RESERVED2, RESERVED3

These registers are reserved.

7.3.13 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM0 through PWM15 registers.

Write to any of the PWM0 to PWM15 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

Table 17. PWMALL - brightness control for all LEDn outputs register (address 42h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
42h	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

7.3.14 IREFALL register: output current value for all LEDn outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LEDn outputs will be set to a current corresponding to this register value.

Write to IREF0 to IREF15 will overwrite the output current settings.

Table 18. IREFALL - Output gain control for all LEDn outputs (address 43h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7:0	IREFALL	write only	00h*	Current gain setting for all LEDn outputs.

7.3.15 LED driver constant current outputs

In LED display applications, PCA9952/Q900, PCA9955/Q900 provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±6 % and less than ±8 % between devices.

7.3.15.1 Adjusting output peak current

The PCA9952/Q900, PCA9955/Q900 scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output peak current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF15. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_LSB = \frac{900\ mV}{R_{ext}} \times \frac{1}{4} \quad (4)$$

$$I_O\_LED\_MAX = (255 \times I_O\_LED\_LSB) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \quad (5)$$

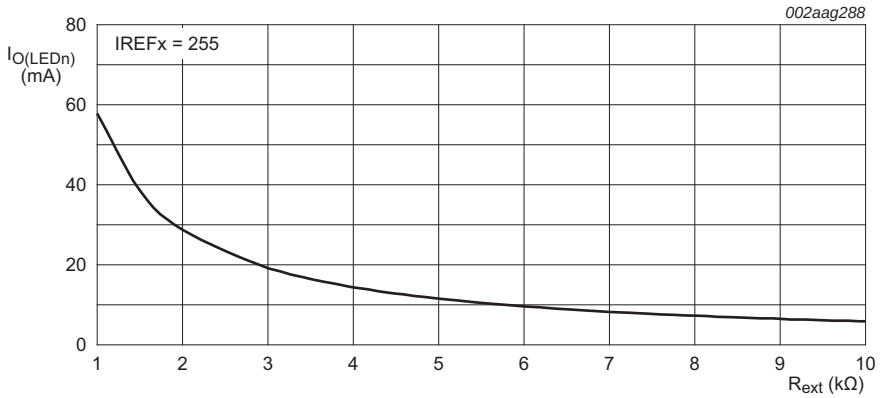
For a given IREFx setting, $I_O\_LED = IREFx \times \frac{900\ mV}{R_{ext}} \times \frac{1}{4}$.

Example 1: If R_{ext} = 1 kΩ, I_{O}_LED_LSB = 225 μA, I_{O}_LED_MAX = 57.375 mA.

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

Example 2: If R_{ext} = 2 kΩ, I_{O}_LED_LSB = 112.5 μA, I_{O}_LED_MAX = 28.687 mA.

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.

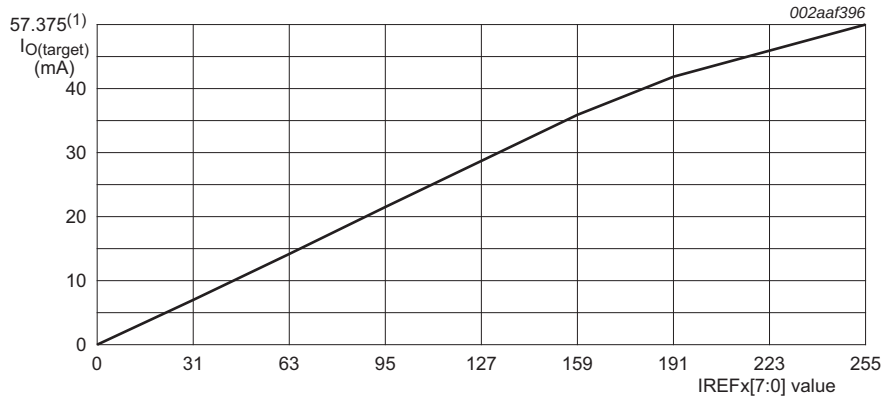


$I_{O(LEDn)}$ (mA) = IREFx × (0.9 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (0.9 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0.

Fig 6. Maximum I_{LED} versus R_{ext}



(1) Assuming R_{ext} = 1 kΩ.

Fig 7. $I_{O(target)}$ versus IREFx value

7.3.16 LED error detection

The PCA9952/Q900, PCA9955/Q900 is capable of detecting an LED open or a short condition at its LEDn output. To detect LED error status, user must initiate the LEDn output fault test. The LEDout channel under test must be ON to conduct this test.

Setting MODE2[6] = 1 initiates the FAULTTEST. The entire test sequence takes up to 52 μs. Once the test cycle begins, all outputs will be turned off (no matter where they are in the group or individual PWM cycle) until entire test sequence is finished and next register read or write is activated. Then each output will be enabled at its previously defined output current level based on IREFx for 1.25 μs. Only those channels with an LEDOUT value other than 00h will be tested. If the output is selected to be fully on, individual dim, or individual and group dim that channel will be tested; however, its operation will be affected for one entire 32 μs individual PWM cycle. At the end of the test cycle PCA9952/Q900, PCA9955/Q900 writes out the 16 error flag bits to EFLAGn.

Before reading the error flag register EFLAGn, user should verify if the FAULTTEST is complete by reading MODE2 register. MODE2[6] = 0 indicates that the test is complete and the error status is ready in EFLAG0 and EFLAG1.

The error flags in registers EFLAG0 and EFLAG1 can now be read.

Table 19. EFLAG0, EFLAG1 - Error flag registers (address 44h, 45h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
44h	EFLAG0	7:0	R only	00h*	Error flag 0; lower 8-bit channel error status
45h	EFLAG1	7:0	R only	00h*	Error flag 1; upper 8-bit channel error status

Remark: The LED open and short-circuit error status bits share the same error flag registers (EFLAG0/EFLAG1). If both LED open and short-circuit conditions exist on different LED outputs, the error status bits in error flag registers report only the open-circuits first and disregards the short-circuits. If only one of the two conditions (that is, LED open-circuits or short-circuits) exists, then the error status bits in error flag registers will report all of those faulted channels. For all unused LED outputs, user must program their LED outputs to the 'OFF' state (LDRx = 00) and IREFx value to 00h, and all unused LED output pins must be pulled up to V_{DD} with a recommended 100 kΩ shared resistor. The states of the unused LED channels have no effect upon the FAULTTEST and always return 0s in EFLAG0/EFLAG1 registers.

7.3.16.1 Open-circuit detection principle

The PCA9952/Q900, PCA9955/Q900 LED open-circuit detection compares the effective current level I_O with the open load detection threshold current $I_{th(det)}$. If I_O is below the threshold $I_{th(det)}$, the PCA9952/Q900, PCA9955/Q900 detects an open load condition. This error status can be read out as an error flag through the registers EFLAG0 and EFLAG1. For open-circuit error detection of an output channel, that channel must be ON.

Table 20. Open-circuit detection

State of output port	Condition of output current	Error status code	Description
OFF	I_O = 0 mA	0	detection not possible
ON	$I_O < I_{th(det)}$ [1]	1	open-circuit
	$I_O \geq I_{th(det)}$ [1]	channel n error status bit 0	normal

[1] $I_{th(det)} = 0.5 \times I_{O(target)}$ (typical). This threshold may be different for each I/O and only depends on IREFx and R_{ext}.

7.3.16.2 Short-circuit detection principle

The LED short-circuit detection compares the effective voltage level (V_O) with the shorted-load detection threshold voltages $V_{th(trig)}$. If V_O is above the $V_{th(trig)}$ threshold, the PCA9952/Q900, PCA9955/Q900 detects a shorted-load condition. If V_O is below the $V_{th(trig)}$ threshold, no error is detected or error bit is reset. This error status can be read out as an error flag through the registers EFLAG0 and EFLAG1. For short-circuit error detection, a channel must be on.

Table 21. Shorted-load detection

State of output port	Condition of output voltage	Error status code	Description
OFF	-	0	detection not possible
ON	$V_O \geq V_{th(trig)}$[1]	1	short-circuit
	$V_O < V_{th(trig)}$[1]	channel n error status bit 0	normal

[1] $V_{th} \approx 2.5$ V.

Remark: The error status does not distinguish between an LED short condition and an LED open condition. When an LED fault condition is noted, the LEDn outputs should be turned off to prevent heat dissipation in the chip and the repair should be done.

7.3.17 Overtemperature protection

If the PCA9952/Q900, PCA9955/Q900 chip temperature exceeds its limit ($T_{th(otp)}$, see Table 24), all output channels will be disabled until the temperature drops below its limit minus a small hysteresis (T_{hys}, see Table 24). When an overtemperature situation is encountered, the OVERTEMP flag (bit 7) is set in the MODE2 register. Once the die temperature reduces below the $T_{th(otp)} - T_{hys}$, the chip will return to the same condition it was prior to the overtemperature event and the OVERTEMP flag will be cleared.

7.4 Active LOW output enable input

Remark: Only the PCA9952/Q900 has the $\overline{OE}$ pin.

The active LOW output enable ($\overline{OE}$) pin on PCA9952/Q900 allows it to enable or disable all the LEDn outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LEDn outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LEDn outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9952/Q900 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9952/Q900, PCA9955/Q900 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9952/Q900, PCA9955/Q900 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 μs. The device will reset itself, and allow 2 ms for the device to fully wake up.

7.6 Hardware reset recovery

When a reset of PCA9952/Q900, PCA9955/Q900 is activated using an active LOW input on the $\overline{RESET}$ pin, a reset pulse width of 2.5 μs minimum is required. The maximum wait time after $\overline{RESET}$ pin is released is 1.5 ms.

7.7 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The maximum wait time after software reset is 1 ms.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call address ‘0000 000’ with the R/$\overline{W}$ bit set to ‘0’ (write) is sent by the I²C-bus master.
3. The PCA9952/Q900, PCA9955/Q900 device(s) acknowledge(s) after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{W}$ bit is set to ‘1’ (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte with 1 specific value (SWRST data byte 1):
   a. Byte 1 = 06h: the PCA9952/Q900, PCA9955/Q900 acknowledges this value only. If byte 1 is not equal to 06h, the PCA9952/Q900, PCA9955/Q900 does not acknowledge it.

   If more than 1 byte of data is sent, the PCA9952/Q900, PCA9955/Q900 does not acknowledge any more.
5. Once the correct byte (SWRST data byte 1) has been sent and correctly acknowledged, the master sends a STOP command to end the SWRST function: the PCA9952/Q900, PCA9955/Q900 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

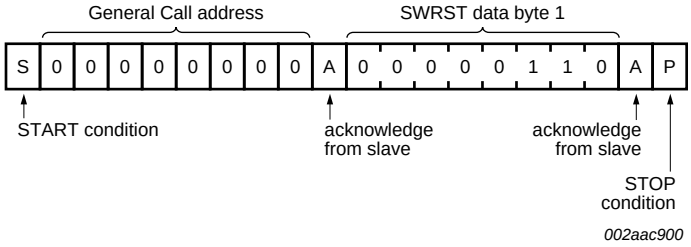


Fig 8. SWRST Call

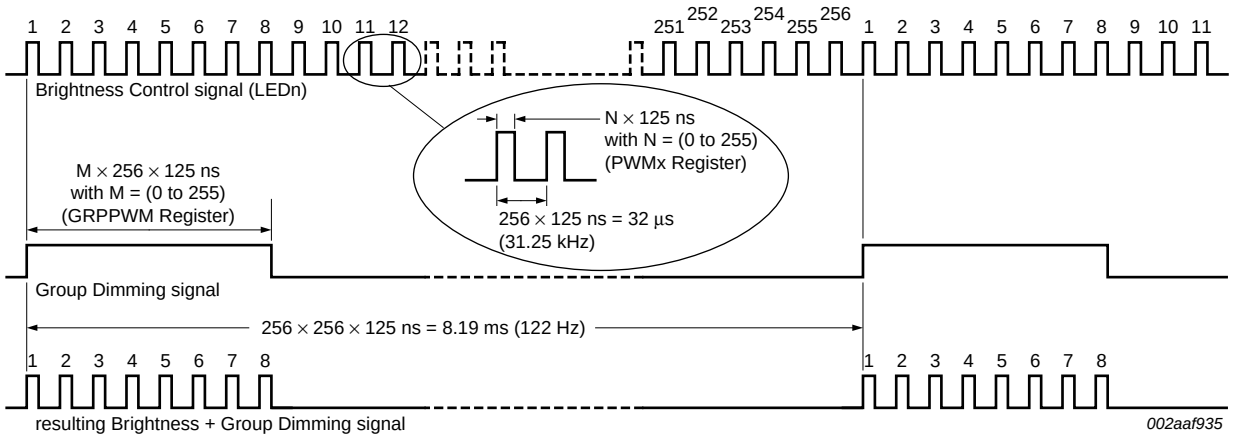
The I²C-bus master must interpret a non-acknowledge from the PCA9952/Q900, PCA9955/Q900 (at any time) as a 'SWRST Call Abort'. The PCA9952/Q900, PCA9955/Q900 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.8 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 16 LEDn outputs control registers LEDOUT0 to LEDOUT3):

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 125 ns.

Minimum pulse width for Group Dimming is 32 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 1 pulse of the LED Brightness Control signal (pulse width = N × 125 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 8.

Fig 9. Brightness + Group Dimming signals

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

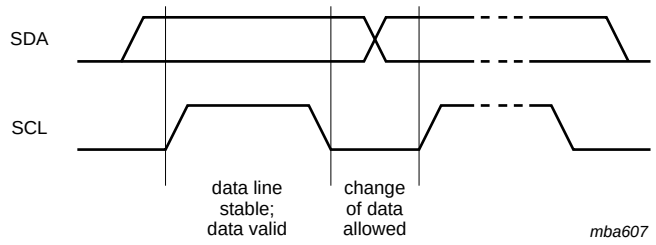


Fig 10. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 11).

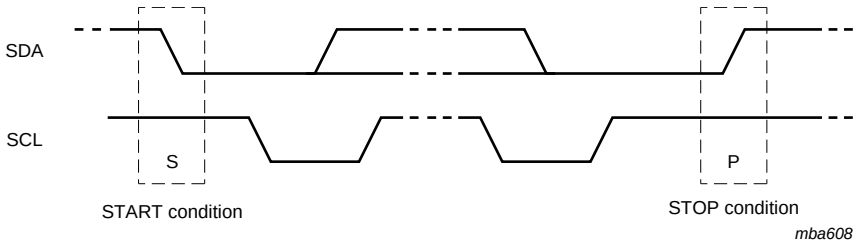


Fig 11. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 12).

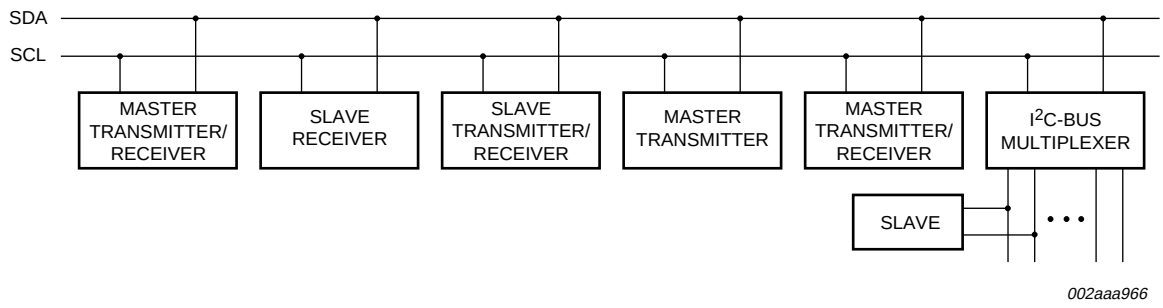


Fig 12. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

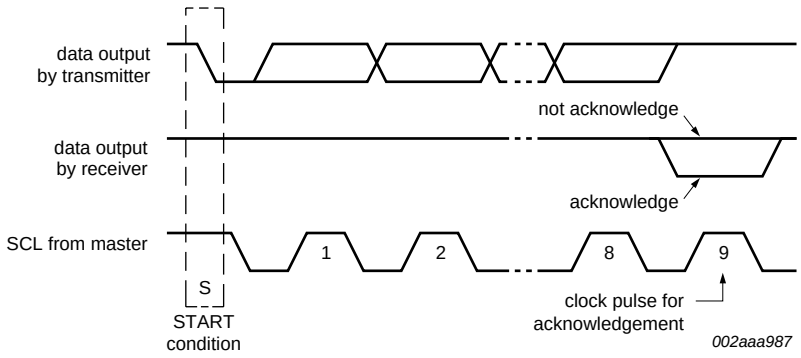
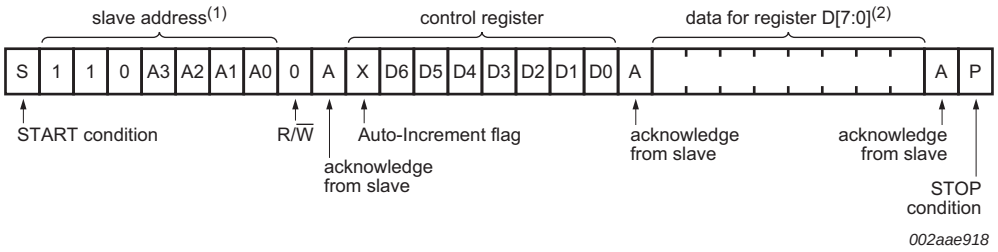


Fig 13. Acknowledgement on the I²C-bus

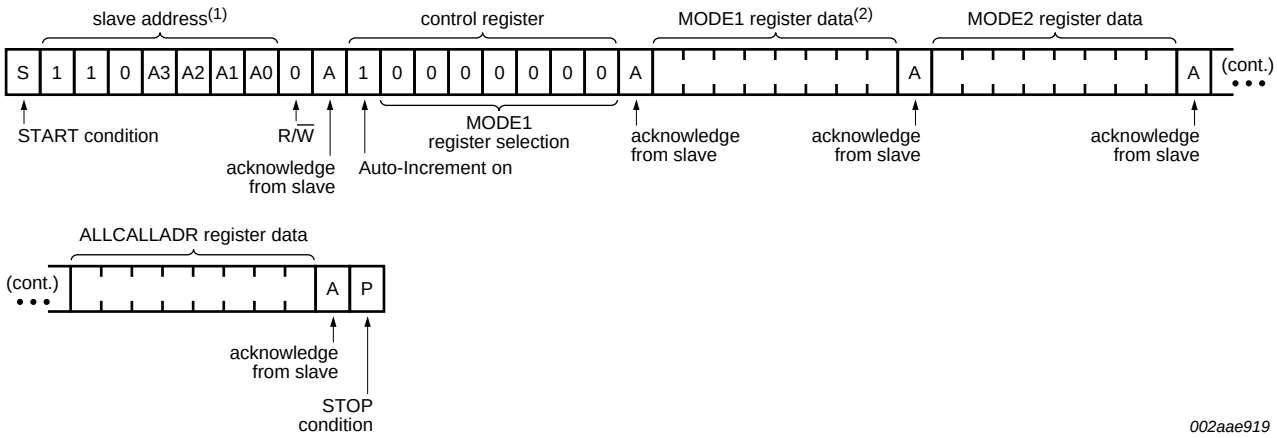
9. Bus transactions



(1) Slave address shown for PCA9955/Q900.

(2) See Table 6 for register definition.

Fig 14. Write to a specific register

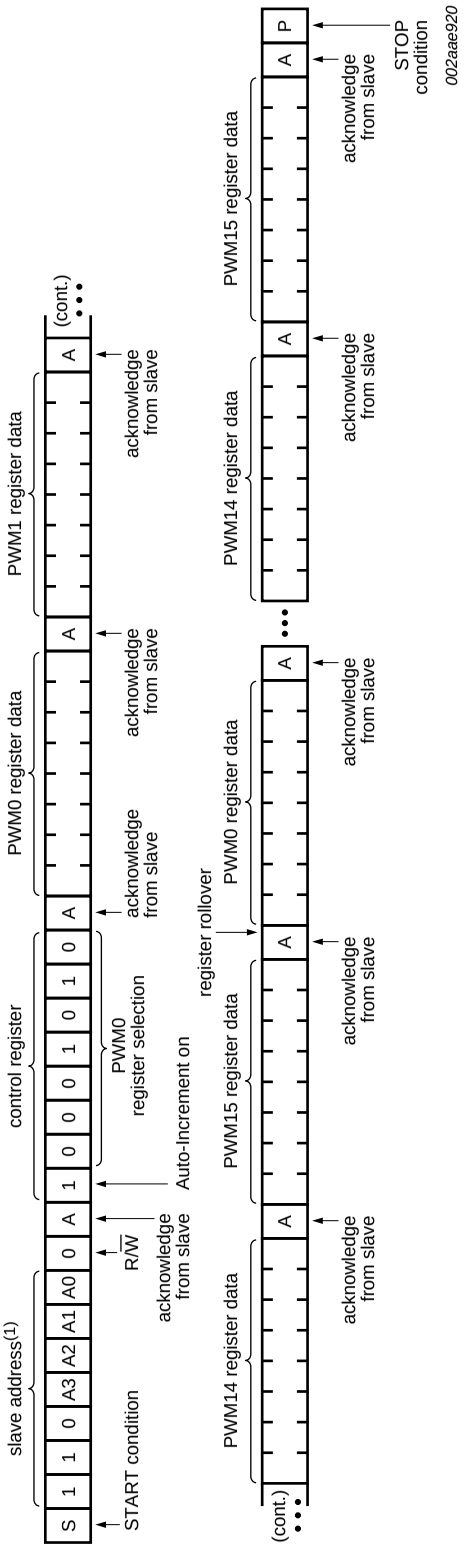


(1) Slave address shown for PCA9955/Q900.

(2) AI1, AI0 = 00. See Table 5 for Auto-Increment options.

Remark: Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options.

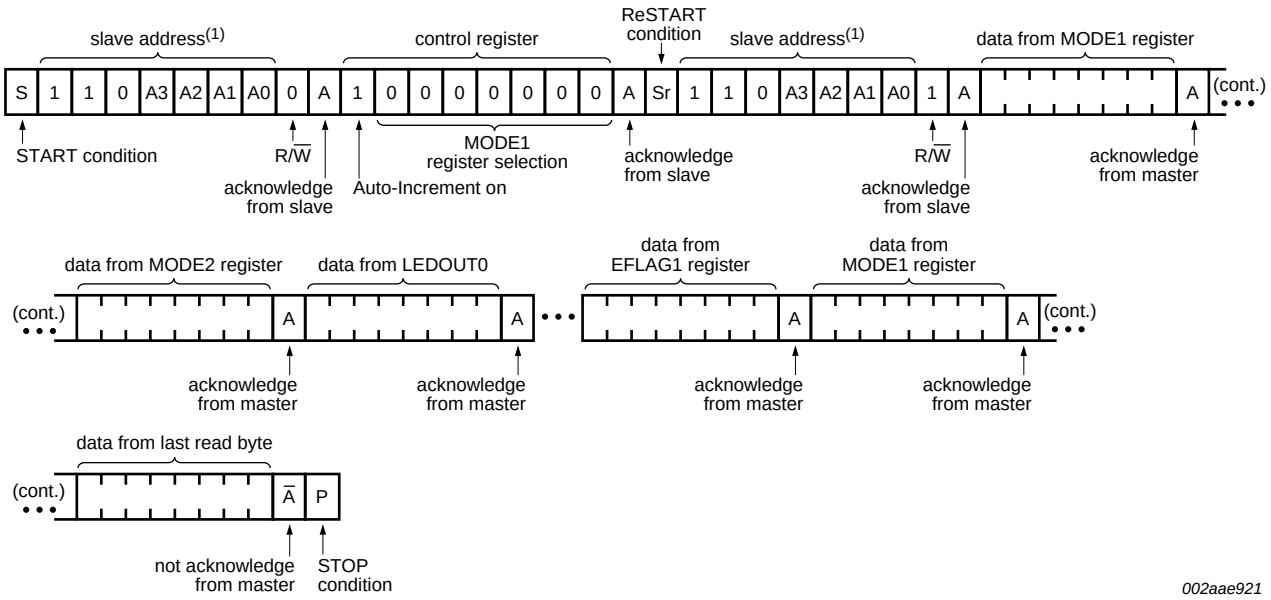
Fig 15. Write to all registers using the Auto-Increment feature



This example assumes that AIF + AI[1:0] = 101b.

(1) Slave address shown for PCA9955/Q900.

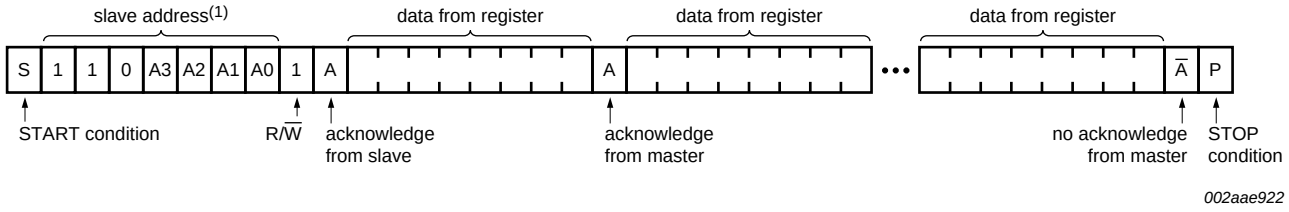
Fig 16. Multiple writes to Individual Brightness registers only using the Auto-Increment feature



This example assumes that the MODE1[5] = 0 and MODE1[6] = 0.

(1) Slave address shown for PCA9955/Q900.

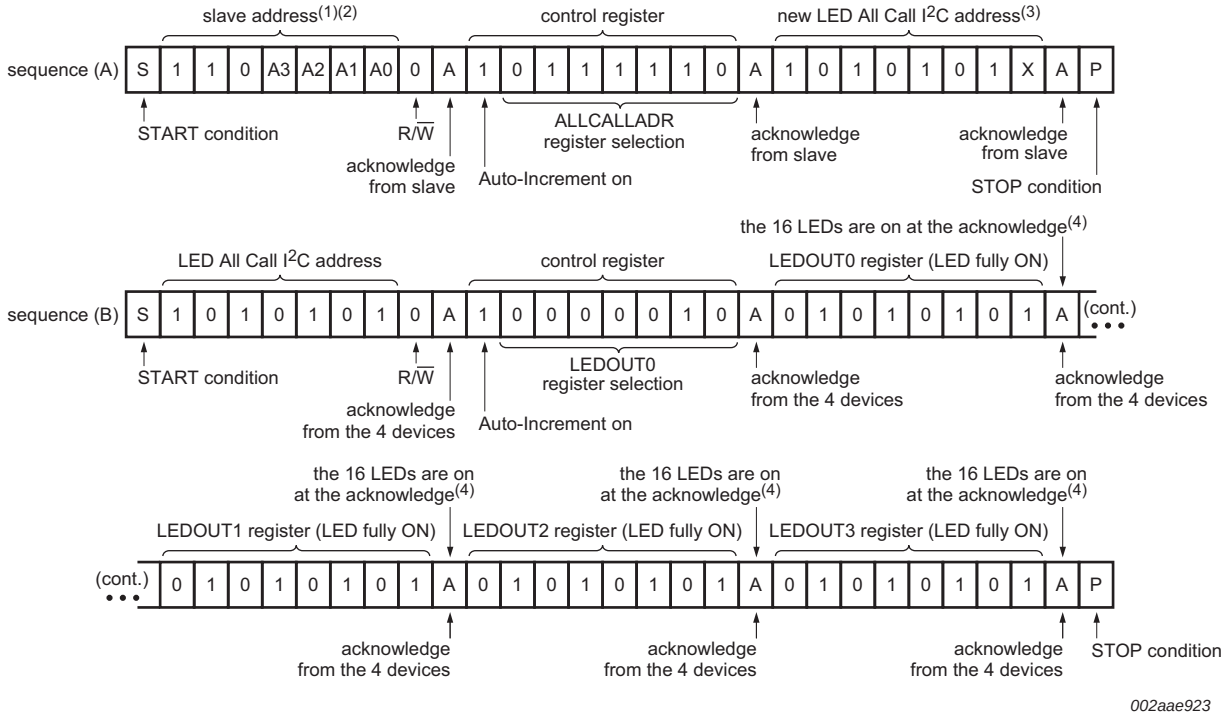
Fig 17. Read all registers using the Auto-Increment feature



Remark: A read operation can be done without doing a write operation before it. In this case, the data sent out is from the register pointed to by the control register (written to during the last write operation) with the Auto-Increment options in the MODE1 register (written to during the last write operation).

(1) Slave address shown for PCA9955/Q900.

Fig 18. Read of registers



(1) Slave address shown for PCA9955/Q900.

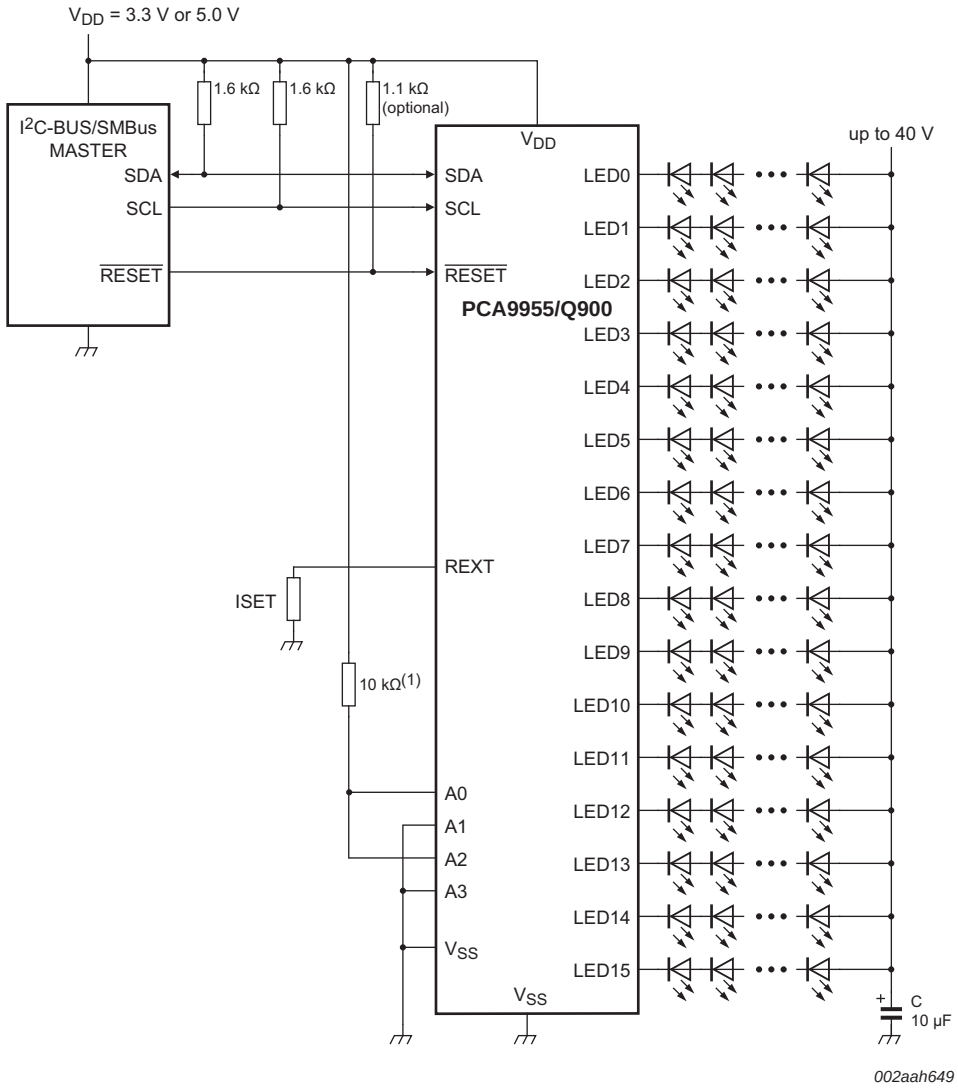
(2) In this example, several PCA9955/Q900s are used and the same sequence (A) (above) is sent to each of them.

(3) ALLCALL bit in MODE1 register is previously set to 1 for this example.

(4) OCH bit in MODE2 register is previously set to 1 for this example.

Fig 19. LED All Call I²C-bus address programming and LED All Call sequence example

10. Application design-in information



(1) A standard 10 kΩ pull-up resistor is required to obtain the best system level ESD performance.

Fig 20. Typical application (PCA9955/Q900)

10.1 Thermal considerations

Since the PCA9952/Q900, PCA9955/Q900 device integrates 16 linear current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device's overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED strings of the same type (e.g., 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each LED

string. Reducing this to a minimum (e.g., 0.8 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device will not go into thermal shutdown when operating under certain application conditions, its junction temperature (T_j) should be calculated to ensure that is below the overtemperature threshold limit (125 °C). The T_j of the device depends on the ambient temperature (T_{amb}), device's total power dissipation (P_{tot}), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (6)$$

where:

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance

P_{tot} = (device) total power dissipation

An example of this calculation is show below:

Conditions:

T_{amb} = 50 °C

$R_{th(j\text{-}a)}$ = 31 °C/W (per JEDEC 51 standard for multilayer PCB)

I_{LED} = 50 mA / channel

$I_{DD(max)}$ = 12 mA

V_{DD} = 5 V

LEDs per channel = 10 LEDs / channel

LED $V_{F(typ)}$ = 3 V per LED (30 V total for 10 LEDs in series)

LED V_F mismatch = 0.2 V per LED (2 V total for 10 LEDs in series)

$V_{reg(drv)}$ = 0.8 V (This will be present only in the LED string with the highest LED forward voltage.)

V_{sup} = LED $V_{F(typ)}$ + LED V_F mismatch + $V_{reg(drv)}$ = 30 V + 2 V + 0.8 V = 32.8 V

P_{tot} calculation:

P_{tot} = IC_power + LED drivers_power;

IC_power = ($I_{DD} \times V_{DD}$) + [(SCL_$V_{OL} \times I_{OL}$) + (SDA_$V_{OL} \times I_{OL}$)]

IC_power = (0.012 A × 5 V) + [(0.4 V × 0.03 A) + (0.4 V × 0.03 A)] = 0.084 W

LED drivers_power = [(16 − 1) × (I_{LED}) × (LED V_F mismatch + $V_{reg(drv)}$)] + ($I_{LED} \times V_{reg(drv)}$)

LED drivers_power = [15 × 0.05 A × (2 V + 0.8 V)] + (0.05 A × 0.8 V) = 2.14 W

P_{tot} = 0.084 W + 2.14 W = 2.224 W

T_j calculation:

$$T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$$

$$T_j = 50\ °C + (31\ °C/W \times 2.224\ W) = 118.94\ °C$$

This confirms that the junction temperature is below the minimum overtemperature threshold of 125 °C, which ensures the device will not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ($R_{th(j-a)}$) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a big enough PCB copper area to ensure proper thermal dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (e.g., 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

11. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} − 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage		V_{SS} − 0.5	40	V
$I_{O(LEDn)}$	output current on pin LEDn		-	65	mA
I_{SS}	ground supply current		-	1.0	A
I_{lu}	latch-up current	JESD [1]	-	90	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	3.2	W
		T_{amb} = 85 °C	-	1.3	W
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C
T_j	junction temperature		−20	+125	°C

[1] Class II, Level B for A1 (pin 3), A2 (pin 4). All other pins are Class II, Level A (±100 mA).

12. Thermal characteristics

Table 23. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HTSSOP28	[1]	31	°C/W

[1] Per JEDEC 51 standard for multilayer PCB.

13. Static characteristics

Table 24. Static characteristics

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			3	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; no load; f_{SCL} = 1 MHz					
		V_{DD} = 3.3 V		-	6.5	14	mA
		V_{DD} = 5.5 V		-	7.0	15	mA
I_{DD}	supply current	R_{ext} = open; LED[15:0] = off		-	0.7	14	mA
		R_{ext} = 2 kΩ; LED[15:0] = off		-	2	14	mA
		R_{ext} = 1 kΩ; LED[15:0] = off		-	3	15	mA
		R_{ext} = 2 kΩ; LED[15:0] = on		-	2	15	mA
		R_{ext} = 1 kΩ; LED[15:0] = on		-	3	16	mA
I_{stb}	standby current	on pin V_{DD}; no load; f_{SCL} = 0 Hz; MODE1[4] = 1; V_I = V_{DD}					
		V_{DD} = 3.3 V		-	100	600	µA
		V_{DD} = 5.5 V		-	100	700	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}		-	2.65	2.8	V
V_{PDR}	power-down reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	0.8	1.25	-	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 3 V		20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V		30	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
Current controlled outputs (LED[15:0])							
I_O	output current	V_O = 0.8 V; IREFx = FFh					
		R_{ext} = 1 kΩ		52	57.5	62	mA
		R_{ext} = 2 kΩ		25.5	28.5	31.5	mA
ΔI_O	output current variation	V_O = 0.8 V; IREFx = FFh					
		between bits (different ICs, same channel); R_{ext} = 1 kΩ		-	±2.5	±8	%
		between bits (2 channels, same IC); R_{ext} = 2 kΩ		-	±1.7	±5.8	%
$V_{reg(drv)}$	driver regulation voltage	minimum regulation voltage; IREFx = FFh; R_{ext} = 1 kΩ		0.8	1.0	40	V
$I_{L(off)}$	off-state leakage current	V_O = 40 V		−1.0	-	+1	µA
$V_{th(L)}$	LOW-level threshold voltage	open LED protection; Error flag will trip during verification test if $V_O \leq V_{th(L)}$		-	0.35	-	V
$V_{th(H)}$	HIGH-level threshold voltage	short LED protection; Error flag will trip during verification test if $V_O \geq V_{th(H)}$		-	2.5	-	V

Table 24. Static characteristics *...continued*

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Address inputs, $\overline{OE}$ input (PCA9952/Q900 only), $\overline{RESET}$ input						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF
Overtemperature protection						
$T_{th(otp)}$	overtemperature protection threshold temperature	rising	125	145	160	°C
		hysteresis	-	20	-	°C

[1] V_{DD} must be lowered to 0.8 V in order to reset part.

14. Dynamic characteristics

Table 25. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	20 + 0.1C_b[5]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C_b[5]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns
$t_{w(rst)}$	reset pulse width		2.5	-	2.5	-	2.5	-	µs
t_{PLH}	LOW to HIGH propagation delay	$\overline{OE}$ to LEDn disable [7]	-	1.2	-	1.2	-	1.2	µs
t_{PHL}	HIGH to LOW propagation delay	$\overline{OE}$ to LEDn enable [7]	-	1.2	-	1.2	-	1.2	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

[7] Load resistor (R_L) for LEDn is 100 Ω pull-up to V_{DD}.

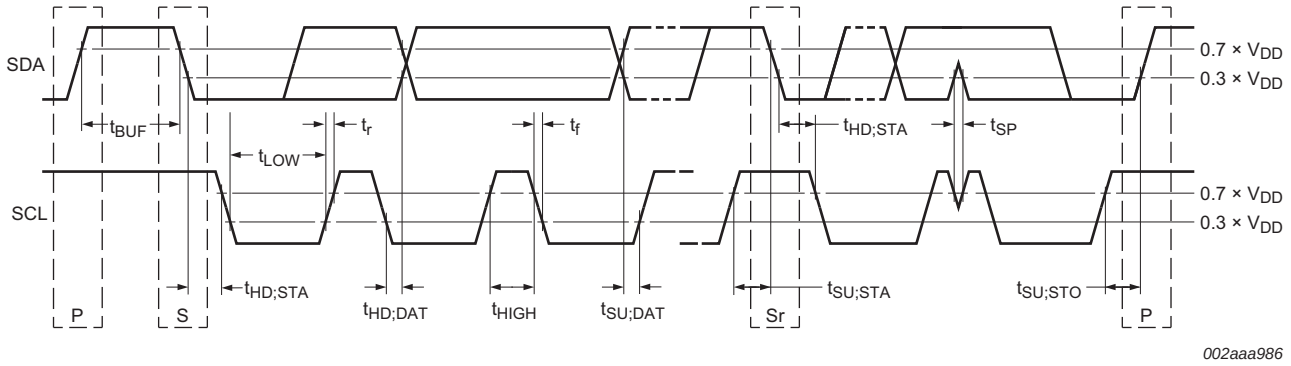
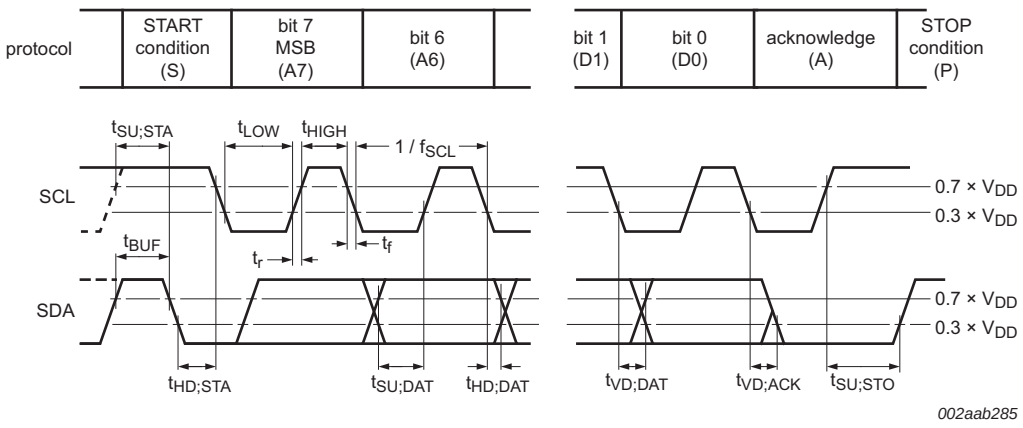


Fig 21. Definition of timing



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 22. I²C-bus timing diagram

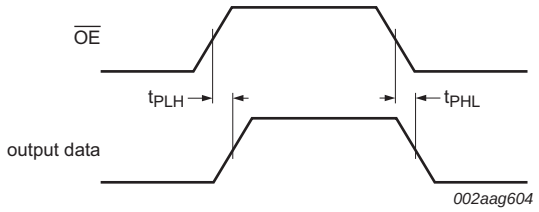
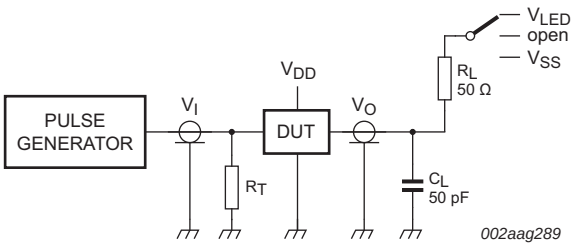


Fig 23. Output propagation delay

15. Test information



R_L = Load resistor for LEDn. R_L for SDA = 165 Ω (30 mA or less current).

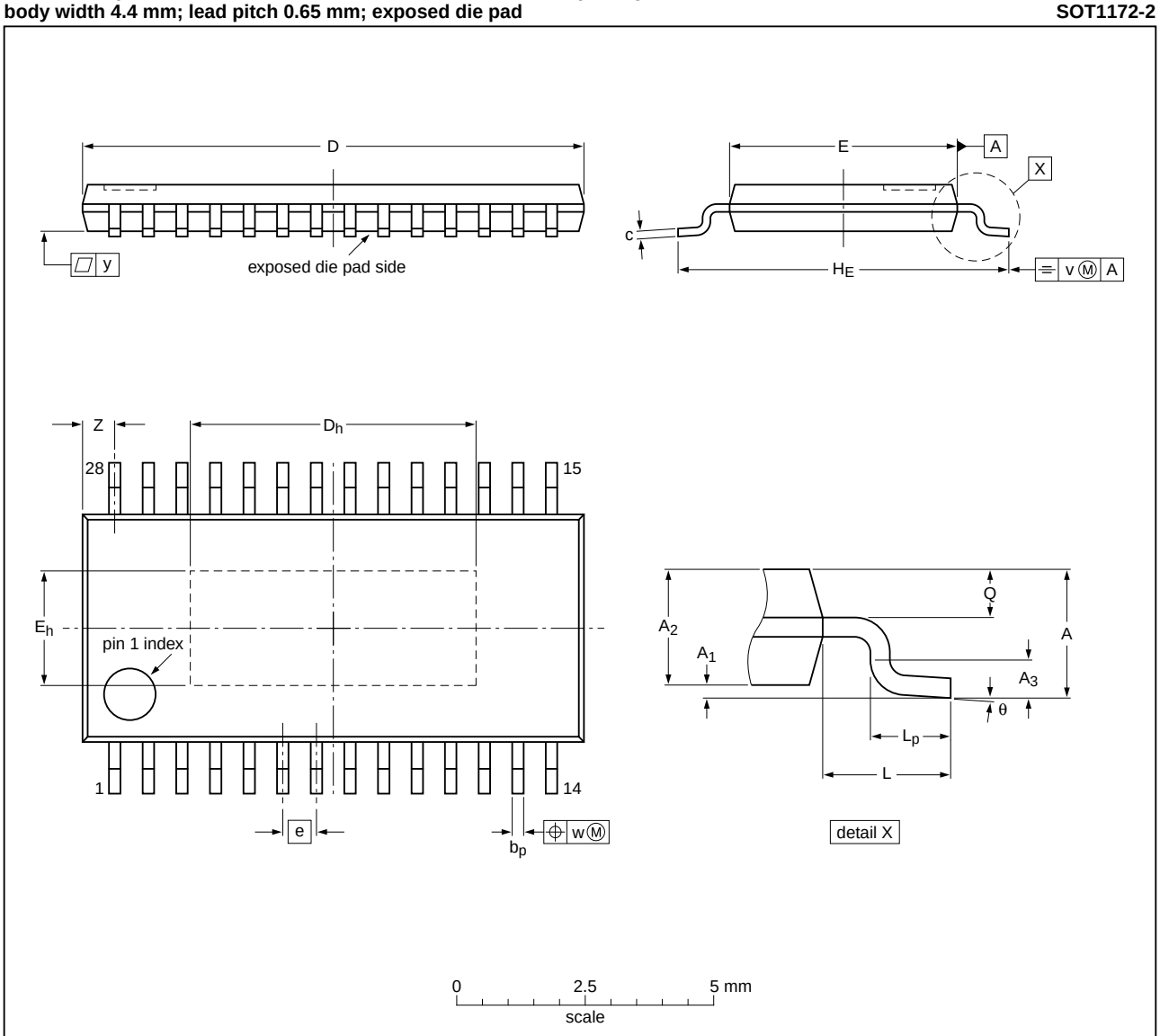
C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 24. Test circuitry for switching times

16. Package outline

HTSSOP28: plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad **SOT1172-2**



Dimensions

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	Q	v	w	y	Z	θ
max	1.1	0.15	0.95		0.30	0.20	9.8	5.6	4.5	2.3		6.6		0.75	0.40				0.80	8°
mm nom		0.10	0.90	0.25	0.22	0.15	9.7	5.5	4.4	2.2	0.65	6.4	1.0	0.62	0.37	0.2	0.13	0.1	0.63	4°
min		0.05	0.85		0.19	0.10	9.6	5.4	4.3	2.1		6.2		0.50	0.3				0.50	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot1172-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1172-2	- - -	MO-153	- - -			~~10-07-06~~ 10-07-13

Fig 25. Package outline SOT1172-2 (HTSSOP28)

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 26 and 27

Table 26. SnPb eutectic process (from J-STD-020D)

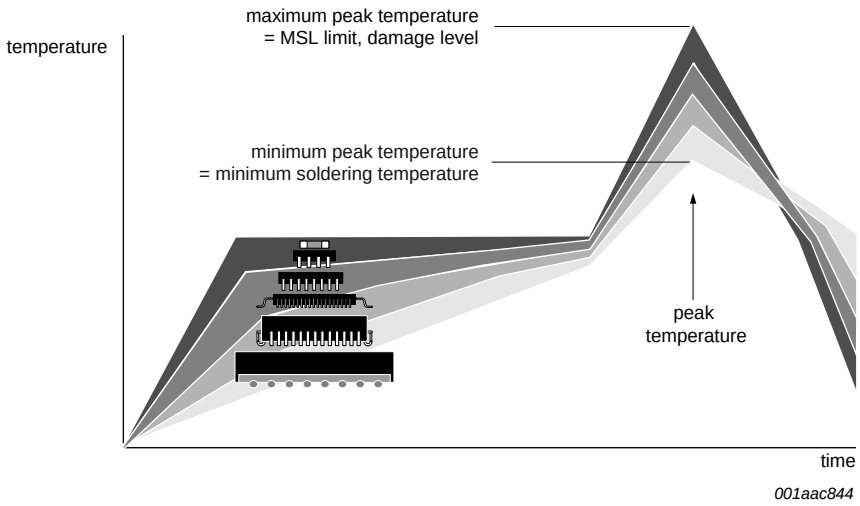
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 27. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 28. Abbreviations

Acronym	Description
ACK	Acknowledge
CDM	Charged-Device Model
DAC	Digital-to-Analog Converter
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

20. References

[1] **AN10897, "A guide to designing for ESD and EMC" —** NXP Semiconductors

[2] **AN11131, "How to improve system level ESD performance" —** NXP Semiconductors

21. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9952Q900_PCA9955Q900 v.1	20130426	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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