élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Features

- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—V_{OS} = 1.5 mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2019CN	−40°C to +85°C	P-DIP	MDP0006

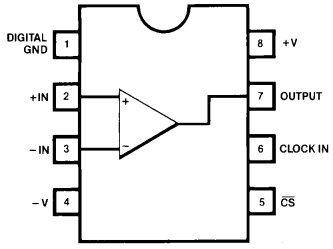
General Description

The EL2019 offers a new feature previously unavailable in a comparator before—a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: *Elantec's Processing-Monolithic Products*.

Connection Diagrams

8-Pin Plastic DIP



Top View

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_{OP}	Peak Output Current	50 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	I_O	Continuous Output Current	25 mA
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies	T_A	Operating Temperature Range	−40°C to +85°C
			T_J	Operating Junction Temperature	150°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_{ST}	Storage Temperature	−65°C to +150°C
I_{INS}	Input Current (Pins 5 or 6)	±5 mA			
P_D	Maximum Power Dissipation (Note 3 - See Curves)	1.25W			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{OS}	Input Offset Voltage V_{CM} = 0V, V_O Transition Point	25°C		1.5	6	I	mV
		T_{MIN}, T_{MAX}			8	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		±100	±400	I	nA
		T_{MIN}, T_{MAX}			±600	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	nA
		T_{MIN}, T_{MAX}			250	III	nA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	75	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	75	95		I	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	V
		T_{MIN}, T_{MAX}	±12			III	V
V_{uncer}	Input Uncertainty Range			30		V	µV/RMS
V_{OL}	Output Voltage Logic Low I_{OL} = 8 mA and I_{OL} = 0 mA)	25°C	−0.05	0.15	0.4	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	III	V
V_{OH}	Output Voltage Logic High						
	V_S = ±15V	25°C	3.5	4.0	4.65	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	III	V
	V_S = ±5V	25°C	2.4			I	V
	V_S = ±5V	T_{MIN}	2.4			III	V
	V_S = ±5V	T_{MAX}	2.4			III	V

TD is 3.6in

DC Electrical Characteristics $V_S = \pm 15V$, unless otherwise specified — Contd.

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{ODIS1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA						
	$V_S = \pm 15V$	25°C	4.65			I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			III	V
	$V_S = \pm 5V$	25°C		3.65		V	V
V_{ODIS2}	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $+15V$	All	−0.3	−1		II	V
V_{INH}	Clock or $\overline{CS}$ Inputs	25°C	2			I	V
	Logic High Input Voltage	T_{MIN}, T_{MAX}	2			III	V
I_{IN}	Clock or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ and $V_{IN} = 5V$	25°C			±200	I	µA
		T_{MIN}, T_{MAX}			±300	III	µA
V_{INL}	Clock or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	V
		T_{MIN}, T_{MAX}			0.8	III	V
I_{S+EN}	Positive Supply Current Enabled	25°C		8.8	13	I	mA
		T_{MIN}, T_{MAX}			14	II	mA
I_{S+DIS}	Positive Supply Current Disabled	25°C		4.9	6	I	mA
		T_{MIN}, T_{MAX}			7	II	mA
I_{S-EN}	Negative Supply Current Enabled	25°C		14.5	17	I	mA
		T_{MIN}, T_{MAX}			18	II	mA
I_{S-DIS}	Negative Supply Current Disabled	25°C		6.4	8.0	I	mA
		T_{MIN}, T_{MAX}			8.0	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
T_S	Setup Time 5 mV Overdrive		12	20	II	ns
T_H	Hold Time		−3	0	IV	ns
T_{OPOUT}	Clock to Output Delay		20	25	IV	ns
T_{OPMIN}	Minimum Clock Width		7		V	ns
T_{EN}	Output 3-State Enable Delay		40	70	IV	ns
T_{DIS}	Output 3-State Disable Delay		150	300	IV	ns

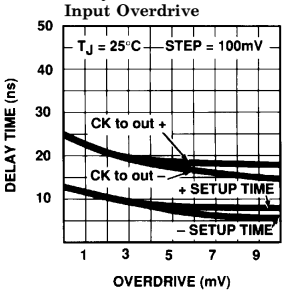
Note 1: $V_{CM} = +12V$ to $-12V$.
Note 2: $V_S = \pm 5V$ to $\pm 15V$.
Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

TD is 3.8in

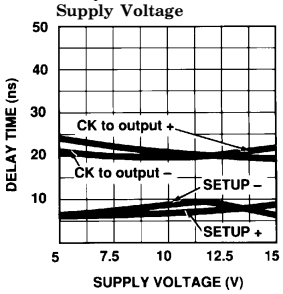
TD is 1.3in

Typical AC Performance Curves

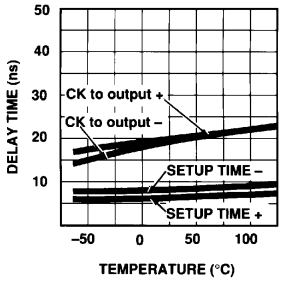
Delay Time vs Input Overdrive



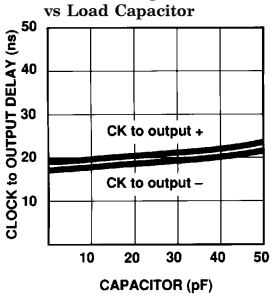
Delay Time vs Supply Voltage



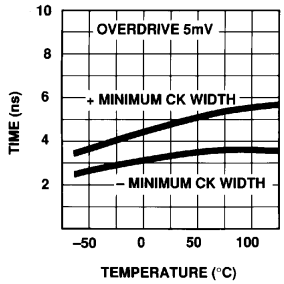
Delay Time vs Temperature



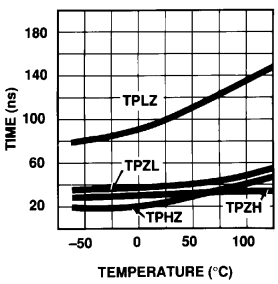
Clock to Output Delay vs Load Capacitor



Minimum Clock Width vs Temperature



Enabled/Disabled Times vs Temperature



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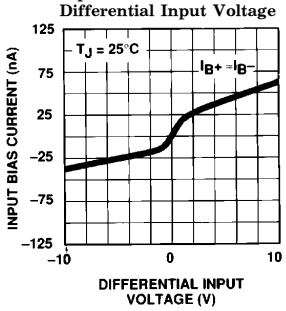
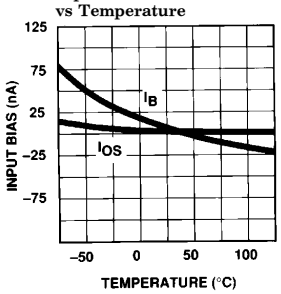
Typical AC Performance Curves — Contd.

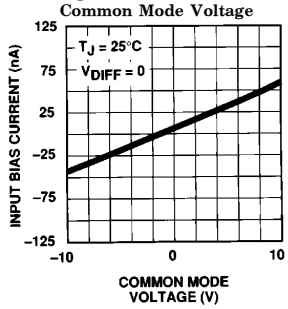
Input Bias Current vs Differential Input Voltage



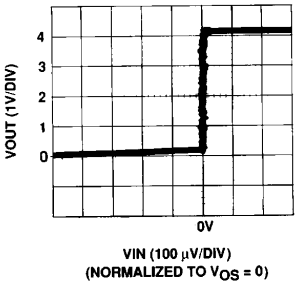
Input Bias Current vs Temperature



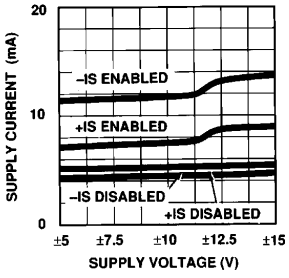
Input Bias Current vs Common Mode Voltage



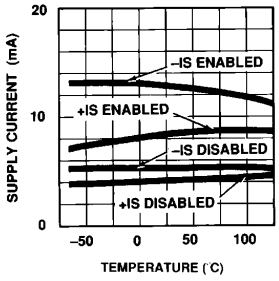
V_O/V_I Transfer Characteristics



Supply Current vs Supply Voltage



Supply Current vs Temperature



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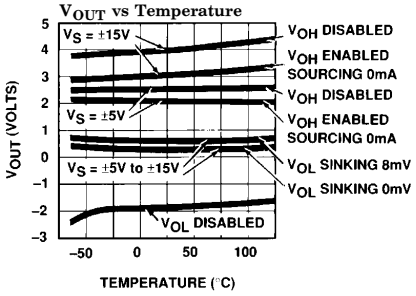
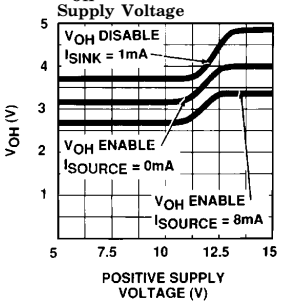
Typical AC Performance Curves — Contd.

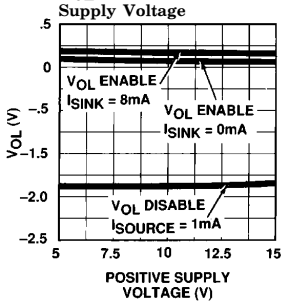
V_{OUT} vs Temperature



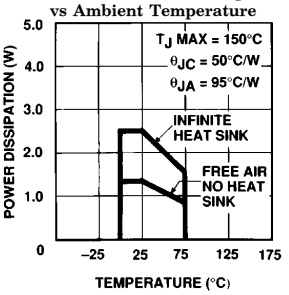
V_{OH} vs Positive Supply Voltage



V_{OL} vs Positive Supply Voltage



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



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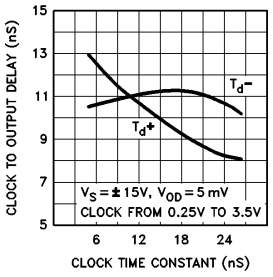
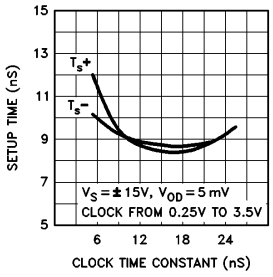
Typical AC Performance Curves — Contd.

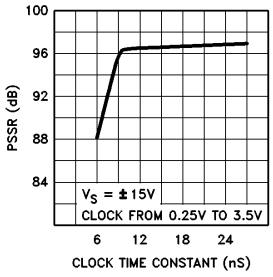
Clock to Output Delay vs Clock Time Constant



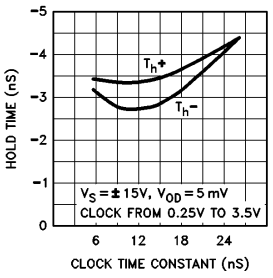
Set-up Time vs Clock Time Constant



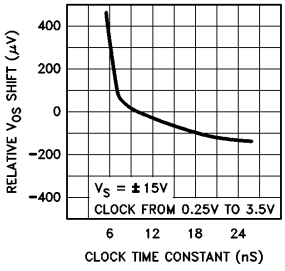
PSRR vs Clock Time Constant



Hold Time vs Clock Time Constant



Relative V_{OS} Shift vs Clock Time Constant



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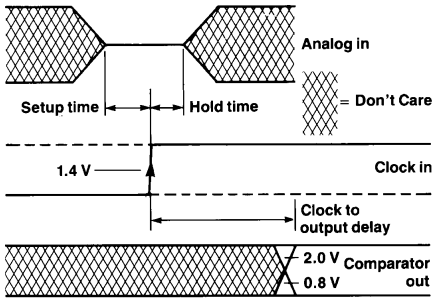
Timing Diagram



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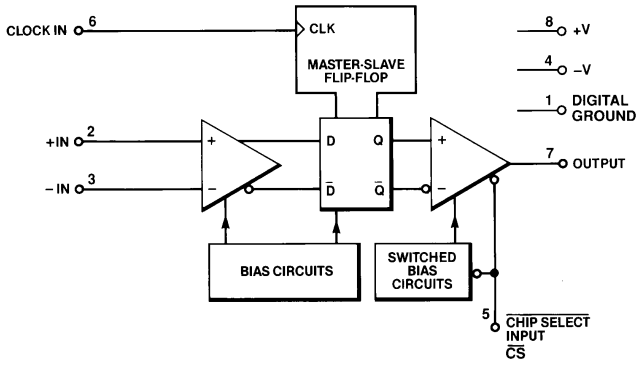
Note: Since the hold time is negative the input is a don't care at the clock time. This ensures that clock noise will not affect the measurement.

Block Diagram



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Function Table

Inputs (Time n − 1)				Internal Q (Time n)	Notes	Output (Time n)
+IN	−IN	$\overline{CS}$	CLK			
+	−	L	↓	H	Normal Comparator Operation	H
−	+	L	↓	L	With "D" Flip-Flop	L
+	−	H	↓	H	Normal Comparator Operation	High Z
−	+	H	↓	L	With "D" Flip-Flop; Power Down Mode	High Z
X	X	L	H	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	L	L	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	L	↑	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	H	H	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	L	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	↑	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z

TD is 2.7in

Application Hints

Device Overview

The EL2019 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. The EL2019 has an internal master/slave flip-flop between the input and output. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2019 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.01 μF monolithic ceramic recommended) within ¼ inch of the power supply leads. Good ground plane construction techniques improve stability, and the lead from pin 1 to ground should be short.

Front End

The EL2019 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V).

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device, or the supply voltage be raised to encompass the input signal in the common mode range.

Input Slew Rate

All comparators have input slew rate limitations. The EL2019 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators. This shows up as an increased set-up time.

Master Slave Flip-Flop

The built-in Master/Slave Flip-Flop only allows the output to change when a positive edge is received on the clock input. This feature has some major benefits to the user. First, the device cannot oscillate due to feedback from the output to the inputs. Second, the device *must* make a decision when it receives a clock input, and the difference between deciding on a "0" or a "1" is limited only by the input circuit noise, both internal and external to the EL2019. With low impedance sources and a good layout this uncertainty can be less than 30 μV/RMS. Since a 30 μV change on the input can cause a 4V change on the output this works out to an effective gain of 103 dB, more than adequate for a 16-bit analog to digital converter.

The hold time of the EL2019 is worst case 0 ns, and typically −3 ns. This means that the analog signal is sampled typically 3 ns *before* the clock time and, worst case, concurrent with the clock.

The EL2019 is sensitive to a large clock edge rates. More than a 500 V/μs edge rate at the clock input will induce V_{OS} shifts, reduce PSRR, and cause the device to operate incorrectly at low temperatures and low supply voltages. A good method to control the clock edge rate is to place a resistor in series and a capacitor to ground in parallel with the clock input. Generally, any time constant 10 ns or greater will suffice.

Elantec tests the EL2019 with a nominal 20 ns time constant, using a series 330Ω resistor and 61 pF of capacitance to ground (including strays). All clocks are generated by Schottky TTL and have a 0.25V to 3.5V swing.

Application Hints — Contd.

Output Stage

The output stage of the EL2019 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2019 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

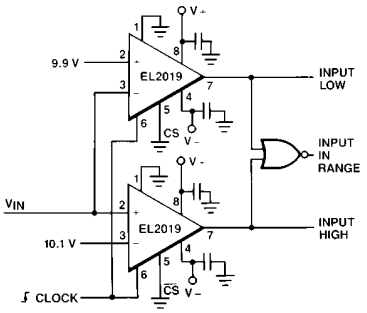
The EL2019 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in large ATE systems where there may be 1000 comparators, but only 10% are in use at any one time.

The EL2019 will work properly with the chip select input (pin 5) floating, however, good R.F. technique would be to ground this input if it is not used.

Due to the power saving feature and linear output stage, the EL2019 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2019 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

Typical Applications

A Wide Input Range Window Comparator



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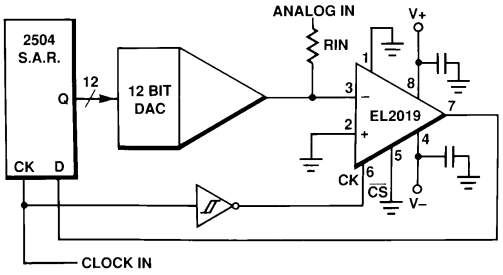
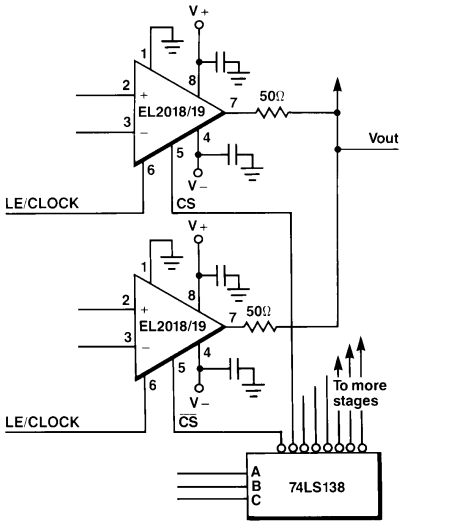
(V_{IN} Range +12V to −12V with V_S = ±15V)

The EL2019 makes an excellent comparator in most analog to digital converters, due to its high gain and fast response. Most 2504 based A to D designs can be modified to use the EL2019 simply by using an inverted clock to the EL2019 as shown below. This results in improved performance due to less jitter of the transition voltages.



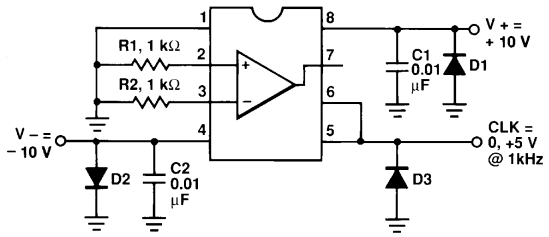
2019–11

Using the Power Down/ 3-State Feature



2019–10

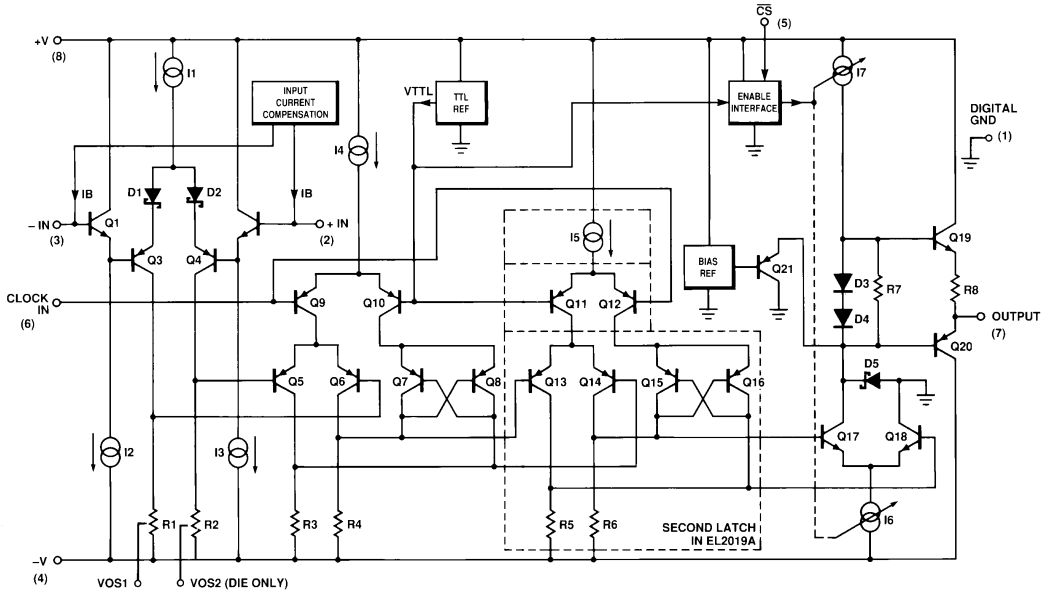
Burn-In Circuit



2019–12

Pin numbers are for DIP packages. All packages use the same schematic.

Equivalent Schematic



2019–13

TAB WIDE

EL2019 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +V
*                   |     |     |     -V
*                   |     |     |     |     Cpin
*                   |     |     |     |     |     CS
*                   |     |     |     |     |     |     output
*                   |     |     |     |     |     |     |
.subckt M2019       2     3     8     4     6     5     7
*
* Input Stage
*
i1 8 10 700µA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200µA
i3 12 4 200µA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700µA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
i5 8 40 500µA
q11 41 17 40 qp
q12 42 6 40 qp
q13 43 16 41 qp
q14 44 15 41 qp
q15 44 43 42 qp
q16 43 44 42 qp
r5 43 4 1K
r6 44 4 1K
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
```

TD is 6.8in

EL2019 Macromodel — Contd.

```
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 44 26 qn 5
q18 0 43 26 qn 5
q22 20 20 30 qn 5
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is = 2e-15 bf = 400 tf = 0.05nS cje = 0.3pF cjc = 0.2pF ccs = 0.2pF)
.model qp pnp (is = 0.6e-15 bf = 60 tf = 0.3nS cje = 0.5pF cjc = 0.5pF ccs = 0.4pF)
.model ds d(is = 2e-12 tt = 0.05nS eg = 0.62V vj = 0.58)
.model sw vswitch (von = 0.4V voff = 2.5V)
.ends
```

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BLANK

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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