

HT8658/HT8659 Voice Recorder (DRAM)

Features

- Single power supply: 4.5V~5.5V
- ADM coding algorithm
- DRAM options:
- 4×256K bits
- 3×1M bits
- A built-in 2 stage MIC amplifier
- A built-in low pass filter

- Data rate options (bits per second):
 - 32K bps
 - 22K bps
 - 16K bps
- 11K bps
- A status LED indicator
- Auto playback

Applications

- Message box
- Recorder

• Toys

General Description

The HT8658/HT8659 are single chip CMOS LSIs using an ADM coding technology. They are designed for applications on recording sounds. The HT8658 and HT8659 have almost the same functions apart from the reset time. The reset time of the HT8658 has to be over 4 seconds but of the HT8659 over 2 seconds.

Blocks within each chip include a DRAM interface circuit, signal amplifier, 8 bit ADC and internal low pass filter. Encoded data are stored

Pin Assignment

AS4

AS3

AS2

AS1

AS0

VDD

AIN

AO

BIAS

FOUT

CAS2B

CAS3B

VSS CAS1B

	0							
4	1	28 🗆	AS5		AS4 🗆	1	28 🗆	AS5
3 🗆	2	27	AS6		AS3 🗆	2	27 🗖	AS6
2	3	26 🗖	AS7		AS2	3	26 🗖	AS7
1	4	25 🗖	AS8		AS1 🗆	4	25 🗖	AS8
0	5	24 🗖	AS9		AS0 🗆	5	24	AS9
D	6	23 🗖	OSC1	,		6	23	OSC1
N	7	22	OSC2			7	22	OSC2
0	8	21	DATA		AO 🗆	8	21	DATA
s 🗆	9	20	RASB	E	BIAS 🗆	9	20	RASB
T	10	19 🗖	WRB	V	оит 🗆	10	19	WRB
s 🗆	11	18 🗖	RESB		vss 🗆	11	18	RESB
B	12	17	RECB	CA	S1B	12	17	RECB
B	13	16	PLYB	CA	S2B	13	16	PLYB
B	14	15	LEDB	CA	S3B 🗆	14	15	LEDB
нт	8658A/	8659A	•		НТ	8658B/	86591	В
	- 28 D					- 28 D	12	

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in external DRAMs and played back after the PLYB pin be triggered. Each IC provides four kinds of sampling rate to be selected, namely 32K/22K/16K/11K bps (bits per second). A higher sampling rate results in sounds of better quality but sacrifices the recording time. With such a powerful built-in circuit, only few components are required for normal applications. Each IC can be offered in a dice form or 28 pin dual-in-line package.



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Block Diagram



Pad Coordinates

Unit: mil

	OSC2	DATA [RASB [_	1	Pad No.	x	Y	Pad No.	X	Y
	29 28	27		26	25	WRB	1	-62.92	29.69	16	62.37	-70.76
					24	RESB	2	-62.92	19.30	17	62.37	-54.61
							3	-62.92	8.37	18	62.71	-44.84
AS9	Π						4	-62.92	-2.30	19	62.71	-34.81
AS8	2		*				5	-62.92	-13.22	20	62.71	-23.04
AS7	3		(0,0)		23	RECB	6	-62.92	-23.89	21	62.71	-13.94
AS6	4		+(0,0)		22	PLYB	7	-62.92	-34.81	22	62.71	-2.93
AS5	5				21	LEDB	8	-62.92	-45.48	23	62.71	8.88
AS4	6				20	CAS3B	9	-62.92	-56.40	24	62.71	58.69
AS3	7				19	CAS2B	10	-62.92	-67.07	25	62.71	70.34
AS2	8				18	CAS1B	11	-46.43	-70.76	26	50.98	70.34
AS1	9				17	VSS	12	-38.78	-70.76	27	-45.07	70.51
AS0	10	11 12		13 14 15	16		13	33.55	-70.76	28	-54.93	70.51
				 ≥ ⊒ ≲]	14	43.16	-70.76	29	-62.58	70.51
		βz		D AS	Ч		15	52.76	-70.76			

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Chip size: $138 \times 154 \text{ (mil)}^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.



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Pad Description

Pad No.	Pad Name	I/O	Internal Connection	Description
1	AS9	I/O	Pull-High CMOS	Input:For IC test onlyOutput:Address output for DRAM of 1Mb and column address strobe for DRAM of 256Kb
2	AS8	I/O	Pull-High CMOS	Input: For IC test only Output: Address output to DRAM
3	AS7	I/O	Pull-High CMOS	Input: For IC test only Output: Address output to DRAM
4	AS6	I/O	Pull-High CMOS	Input: For IC test only 1: For IC test only 0: Not applicable Output: Address output to DRAM
5	AS5	I/O	Pull-High CMOS	Input: DRAM type selection: 1: 256Kb (without external pull-low resistors) 0: 1Mb (with an external pull-low resistor) Output: Address output to DRAM
6	AS4	I/O	Pull-High CMOS	Input: Manual/Auto playback selection: 1: Manual (without external pull-low resistors) 0: Auto (with an external pull-low resistor) Output: Address output to DRAM
7,8	AS3,AS2	I/O	Pull-High CMOS	Input:DRAM chip number selection (refer to the functional description)Output:Address output to DRAM
9,10	AS1,AS0	I/O	Pull-High CMOS	Input:Sampling rate selection (refer to the functional description)Output:Address output to DRAM
11	VDD	Ι	_	Positive power supply
12	AIN	Ι	_	Pre-amplifier input pin
13	AO	0		Pre-amplifier output pin Amplifier gain should be adjusted between AIN and AO by a resistor.
14	BIAS	Ι	_	For internal OP bias de-coupling
15	VOUT	0	—	Audio signal output (non-filtered, output directly)
16	FOUT	0	_	Audio signal output through an internal low-pass filter
17	VSS	Ι	_	Negative power supply (GND)

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Pad No.	Pad Name	I/O	Internal Connection	Description
18~20	CAS1B~ CAS3B	0	CMOS	Column address strobe for DRAM1~DRAM3
21	LEDB	0	Open Drain NMOS	Status indicator when LSI is active
22	PLYB	Ι	Pull-High	Play/Pause trigger input (toggle function)
23	RECB	Ι	Pull-High	Record/Pause trigger input (toggle function)
24	RESB	Ι	Pull-High	Reset the system or the play counter
25	WRB	0	CMOS	Write enable signal output for DRAM interface
26	RASB	0	CMOS	Row address strobe output for DRAM interface
27	DATA	I/O	_	Encoded data I/O pin
28 29	OSC2 OSC1	O I	_	Oscillation external resistor connect pin

Absolute Maximum Ratings

Supply Voltage	–0.3 to 6V
Input Voltage	V _{SS} -0.3 Vto V _{DD} +0.3V

Storage Temperature	50°C to 125°C
Operating Temperature	–20°C to 70°C

Electrical Characteristics

Symbol	Danamatan	Т	est Condition	Min	Tum	Moy	Unit
Symbol	Farameter	VDD	Condition	IVIIII.	ryp.	Max.	Unit
VDD	Operating Voltage	_	_	4.5	5.0	5.5	V
I _{DD}	Operating Current	5V	No load, Fosc=384KHz	_	0.8	2.0	mA
ISTB	Stand-By Current	5V	_	_	40	100	μΑ
Iol	LED Sink Current	5V	V _{OL} =0.5V	3.0	5.0	_	mA
VIH	"H" Input Voltage	_	_	0.7V _{DD}	_	V _{DD}	V
V _{IL}	"L" Input Voltagse	_	_	0	_	$0.2 V_{DD}$	V
Fosc	System Frequency	5V	R _{OSC} =91K	_	384		KHz
Vout	Max. Vout Output Voltage	5V	R _L >50K	1.5	_	_	VP-P

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(Ta=25°C)

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Functional Description

The HT8658/HT8659 are single chip LSIs with an external DRAM (dynamic random access memory). They are designed for applications on recording sounds. The recording length is decided by the data rate along with the size of an external memory. The type as well as amount of DRAM, operation mode and sampling rate are determined by the connection of the AS0~AS6 pins. The HT8658/8659 provide 2 audio outputs. One is filtered by an internal low pass filter for the sake of improving sound quality in addition to minimizing external required components. The other is non-filtered and a voice signal can be filtered with an external circuit to decide the audio cut-off frequency as well as band width. The two chips have the same functions except the reset time as shown:

Name	Reset Time (Minimum)
HT8658	4 seconds
HT8659	2 seconds

Initial setting of operation mode

The HT8658/HT8659 load the statuses of the AS0~AS6 pins into a mode register after power is initially turned on or the system is reset. These pins are internally built with pull-high resistors so that all inputs with "1" are the default value of the mode register. External pull-low resistors which are tied to the AS0~AS6 pins defines the operation mode of the ICs as shown in the following table:

AS0	AS1	AS2	AS3	AS4	AS5	AS6	Function Description
0	0	Х	X	Х	Х	Х	Data rate: 32K bps
1	0	Х	Х	X	X	Х	Data rate: 22K bps
1	1	Х	Х	X	X	Х	Data rate: 16K bps
0	1	X	X	Х	Х	X	Data rate: 11K bps
X	Х	0	0	Х	Х	Х	DRAM chip number: 4 pcs
X	Х	1	0	Х	Х	Х	DRAM chip number: 3 pcs
X	Х	0	1	Х	Х	Х	DRAM chip number: 2 pcs
X	X	1	1	Х	Х	X	DRAM chip number: 1 pcs
X	Х	Х	Х	1	Х	1	Operation mode: Normal mode
X	Х	Х	Х	0	Х	1	Operation mode: Auto play back mode
X	Х	Х	Х	1	Х	0	Operation mode: Not applicable
X	Х	Х	X	0	Х	0	Operation mode: Not applicable
X	Х	Х	Х	Х	1	Х	DRAM type: 256Kb
X	X	X	X	X	0	X	DRAM type: 1Mb

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Notes: 1."0" connects an external pull-low resistor to ASn, where n=0~6.

2."1" connects no external pull-low resistor to ASn, where n=0~6.

3."X" means don't car.



Recording capacity

The HT8658/HT8659 offer 4 kinds of voice sampling rate, namely 32K, 22K, 16K and 11Kbps (based on a system frequency of 384KHz), selectable by the connection of the AS0 and AS1 pins. The voice sampling rate decides the recording capacity of the ICs in addition to the type and amount of DRAM. A higher sampling rate results in sounds of better quality but shortens the recording time.

Sampling Rate	DRAM Size (Maximum)	Recording Time
32K bps	1Mb×3	94 seconds
22K bps	1Mb×3	136 seconds
16K bps	1Mb×3	188 seconds
11K bps	1Mb×3	272 seconds

Recording Time

Memory selection

The HT8658/HT8659 provide a DRAM interface circuit. The type as well as amount of DRAM decides the recording length of the ICs at a designated sampling rate. There are 2 kinds of DRAM, namely 256Kb and 1Mb, selectable by the connection of the AS5 pin. The ICs can interface with a maximum of 4 DRAMs for the 256Kb type but 3 DRAMs for the 1Mb type. The amount of DRAMs is decided by the connection of the AS2 and AS3 pins.

AS5	AS3	AS2	Memory Size
1	1	1	256Kb×1
1	1	0	256Kb×2
1	0	1	256Kb×3
1	0	0	256Kb×4
0	1	1	1Mb×1
0	1	0	1Mb×2
0	0	1	1Mb×3
0	0	0	1Mb×3

Notes: 1. "0" connects an external pull-low resistor to ASn, where n=2,3, or 5.

> 2. "1" connects no external pull-low resistors to ASn, where n=2, 3 or 5.

Record function

The HT8658/HT8659 enter the recording state from the standby state when the memories are not full and the REC key is triggered as well. In the recording state, sounds input from an external microphone are coded by an internal ADM (adaptive delta modulation) algorithm and saved in an external memory until the memories are all full or the REC key is retriggered.

During recording, recording will pause and the recording counter stop counting by retriggering the REC key. At this time, if the memories are not full and the REC key is triggered again, the ICs will record sounds from the pause position. Once the memories are full, recording will be terminated and any retrigger to the REC key be ignored.

After recording is stopped, the HT8658/HT8659 will play back the recorded sounds automatically in the AUTO PLAY mode. They, on the other hand, will play back the recorded sounds by manually triggering the PLAY key in the normal mode.

Play function

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The HT8658/HT8659 provide 2 kinds of playing modes, namely normal mode and AUTO PLAY mode. In the normal mode, the ICs will play back the recorded sounds when recording is terminated and the PLAY key is triggered. In the AUTO PLAY mode, they will play back the recorded sounds automatically without manually triggering the PLAY key once recording is terminated. In the process of playing sounds, triggering the PLAY key will pause the playing back in addition to the playing counter. To resume playing back, simply retrigger the PLAY key. Playing back will start at the pause position.



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AS4	AS6	Function
1	1	Normal mode
0	1	AUTO PLAY mode
1	0	Not applicable
0	0	Not applicable

Notes: 1. "0" connects an external pull-low resistor to ASn, where n=4, 6.

2. "1" connects no external pull-low resistor to ASn, where n=4, 6.

System reset

The reset time of the HT8658 and HT8659 is different. The HT8658 will reset the system if the RES key is pressed more than 4 seconds and reset the playing counter if the RES key is pressed less than 4 seconds. The HT8659, on the other hand, will reset the system if the RES key is pressed over 2 seconds and reset the playing counter if the key is pressed less than 2 seconds. Once the playing counter is reset, the ICs will play back the recorded data from the beginning by triggering the PLAY key. All of the recorded data will be deleted after the system is reset.

Indicate function

The HT8658/HT8659 provide an LEDB pin to indicate the operation status of the LSI through an external LED display. The LEDB pin is of high impedance and an external LED is switched off in the standby state. LEDB, on the other hand, remains at a low level and LED is turned on in the recording state. In the playback state, LED flashes with the volume of output sounds. When the system is reset, it flashes at a 2Hz rate.

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Operation flowchart

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• HT8659



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• Normal mode operation (AS4=1, AS6=1)



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• Auto playback mode (AS4=0, AS6=1)



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Notes: 1. RECC: Recording counter

2. PLAYC: Playing-back counter

3. m,n: DRAM addresses



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Application Circuits

With a DRAM interface of 1Mb (Chip form)



* The IC substrate should be connected to VDD in PCB layout artwork.

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With a DRAM interface of 1Mb (Package form)



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With a DRAM interface of 256Kb (Chip form)



* The IC substrate should be connected to VDD in PCB layout artwork.

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With a DRAM interface of 256Kb (Package form)



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