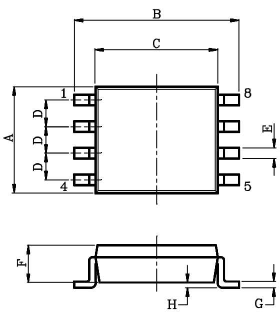
KIC7W126FK

SILICON MONOLITHIC CMOS DIGITAL INTEGRATED CIRCUIT

DUAL BUS BUFFER

The KIC7W126FK is a high speed C^2MOS DUAL BUS BUFFERS fabricated with silicon gate C^2MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C^2MOS low power dissipation. The require 3-state control input G to be set low to place the output into the high impedance.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIM	MILLIMETERS
A	2.0±0.1
B	3.1±0.1
C	2.3±0.1
D	0.5
E	0.2+0.05/−0.04
F	0.7±0.1
G	0.12±0.04
H	0 ~ 0.1

US8

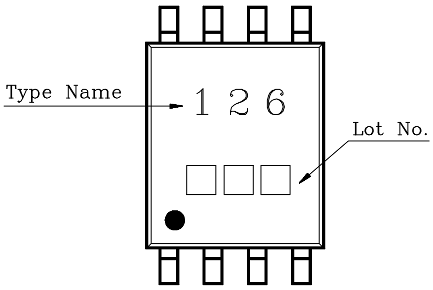
FEATURES

- High Speed : t_{pd}=10ns(Typ.) at V_{CC}=5V.
- Low Power Dissipation : I_{CC}=2μA(Max.) at Ta=25℃.
- High Noise Immunity : V_{NIH}=V_{NIL}=28% V_{CC}(Min.).
- Output Drive Capability : 15 LSTTL Loads.
- Symmetrical Output Impedance : $|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays : t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range : $V_{CC(opr)}$=2～6V.

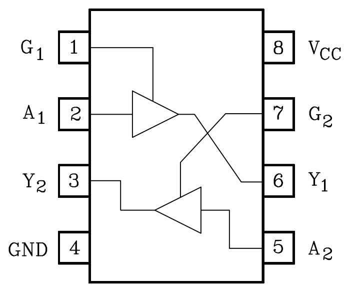
MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5～7	V
DC Input Voltage	V_{IN}	-0.5～V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5～V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±37.5	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65～150	℃
Lead Temperature (10s)	T_L	260	℃

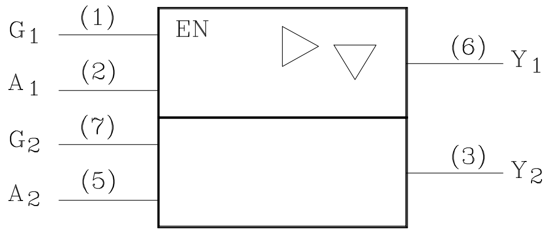
MARKING



PIN CONNECTION(TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X : Don't Care
Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	℃
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=-40~85℃ MIN.	Ta=-40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}	-	-		2.0	1.5	-	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	
					6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}	-	-		2.0	-	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	
					6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	-	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
					4.5	4.4	4.5	-	4.4	-	
					6.0	5.9	6.0	-	5.9	-	
				I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
				I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	-	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
					4.5	-	0.0	0.1	-	0.1	
					6.0	-	0.0	0.1	-	0.1	
				I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
				I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	-	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	-	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	-	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r=t_f=6ns)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	C_L	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=-40~85℃ MIN.	Ta=-40~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	-	-	50	2.0 4.5 6.0	- - -	20 6 5	60 12 10	- - -	75 15 13	ns
Propagation Delay Time	t_{pLH} t_{pHL}	-	-	50	2.0 4.5 6.0	- - -	30 11 10	90 18 15	- - -	115 23 20	ns
				150	2.0 4.5 6.0	- - -	42 14 12	130 26 22	- - -	165 33 28	ns
Output Enable Time	t_{pZL} t_{pZH}	-	R_L=1kΩ	50	2.0 4.5 6.0	- - -	30 11 10	90 18 15	- - -	115 23 20	ns
				150	2.0 4.5 6.0	- - -	42 14 12	130 26 22	- - -	165 33 28	ns
Output Disable Time	t_{pLZ} t_{pHZ}	-	R_L=1kΩ	50	2.0 4.5 6.0	- - -	24 12 10	100 20 17	- - -	125 25 21	ns
Input Capacitance	C_{IN}	-	-	-	-	-	5	10	-	10	pF
Output Capacitance	C_{OUT}	-	-	-	-	-	10	-	-	-	pF
Power Dissipation Capacitance	C_{PD}	-	(Note 1)	-	-	-	32	-	-	-	pF

Note 1 : C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation
: $I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2$ (per gate)