

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800AXX-5,-5S	50	13	25	13	90	655
M5M417800AXX-6,-6S	60	15	30	15	110	540
M5M417800AXX-7,-7S	70	20	35	20	130	475

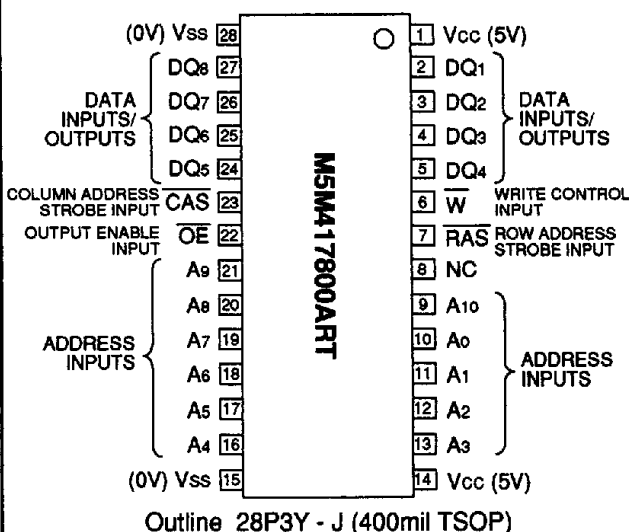
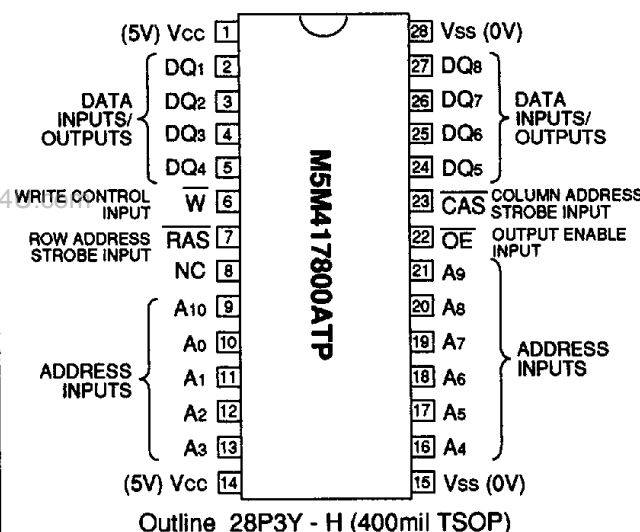
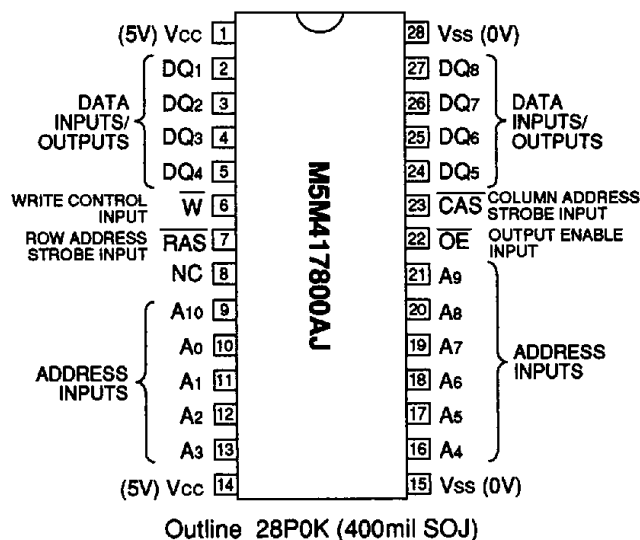
XX = J, TP, RT

- Standard 28 pin SOJ, 28 pin TSOP
- Single $5V \pm 10\%$ supply
- Low stand-by power dissipation
 - 5.5mW (Max) CMOS Input level
 - 2.2mW*(Max) CMOS Input level
- Low operating power dissipation
 - M5M417800AXX- 5, -5S 800.0mW (Max)
 - M5M417800AXX- 6, -6S 660.0mW (Max)
 - M5M417800AXX- 7, -7S 580.0mW (Max)
- Self refresh capability*
 - self refresh current 400.0 μ A (Max)
- Fast-page mode, Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A₀~A₁₀)
 - *Applicable to self refresh version (M5M417800AJ, TP, RT -5S, -6S, -7S : option only)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****FUNCTION**

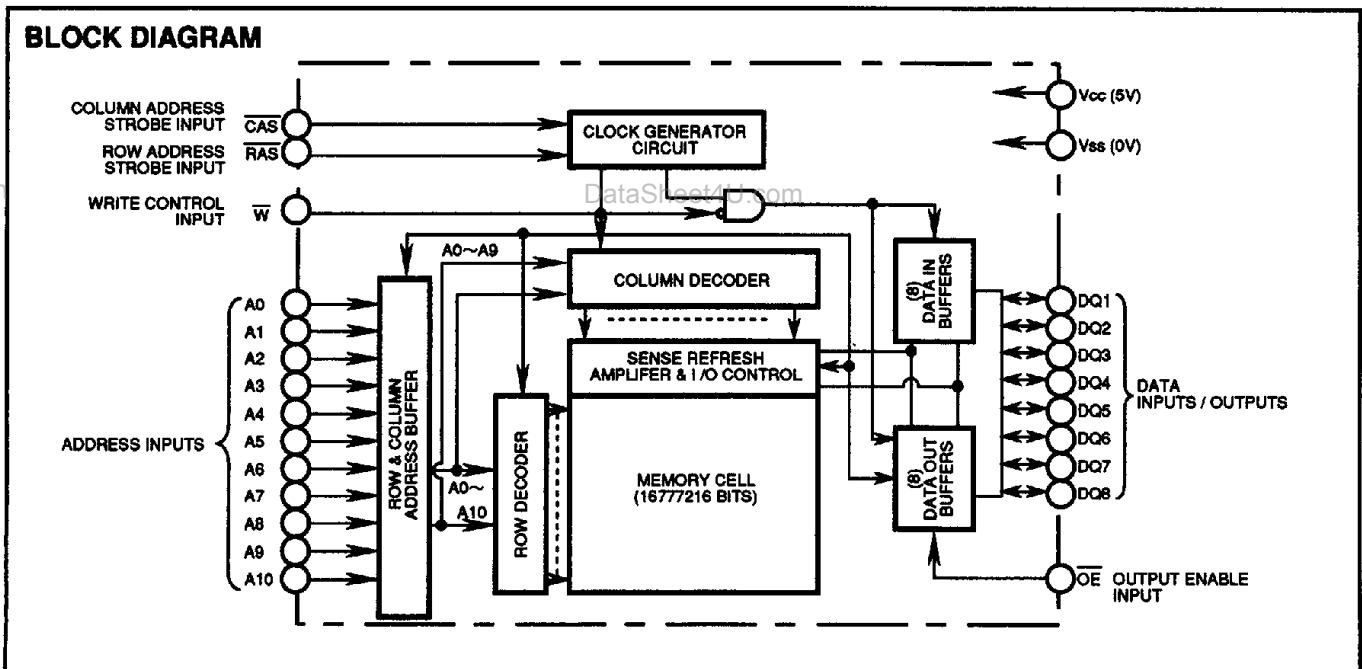
The M5M417800AJ, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other

functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	-1~7	V
V _i	Input voltage		-1~7	V
V _o	Output voltage		-1~7	V
I _o	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	4.5	5	5.5	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.0	V
V _{IL}	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to V_{ss}**ELECTRICAL CHARACTERISTICS** (T_a = 0~70°C, V_{cc} = 5V±10%, V_{ss} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} = -5mA	2.4		V _{cc}	V
V _{OL}	Low-level output voltage		I _{OL} = 4.2mA	0		0.4	V
I _{oz}	Off-state output current		Q floating, 0V ≤ V _{out} ≤ 5.5V	-10		10	μA
I _i	Input current		0V ≤ V _{in} ≤ 6.5V, Other inputs pins = 0V	-10		10	μA
I _{cc1} (AV)	Average supply current from V _{cc} operating (Note 3,4)	M5M417800A-5,-5S	RAS, CAS cycling trc = twc = min. output open			145	mA
		M5M417800A-6,-6S				120	
		M5M417800A-7,-7S				105	
I _{cc2}	Supply current from V _{cc} , stand-by		RAS = CAS = V _{IH} , output open			2	mA
			RAS = CAS ≥ V _{cc} - 0.5			1	
I _{cc3} (AV)	Average supply current from V _{cc} refreshing (Note 3)	M5M417800A-5,-5S	RAS cycling, CAS = V _{IH} trc = min. output open			145	mA
		M5M417800A-6,-6S				120	
		M5M417800A-7,-7S				105	
I _{cc4} (AV)	Average supply current from V _{cc} Fast-Page-Mode (Note 3,4)	M5M417800A-5,-5S	RAS = V _{IL} , CAS cycling trc = min. output open			80	mA
		M5M417800A-6,-6S				70	
		M5M417800A-7,-7S				60	
I _{cc6} (AV)	Average supply current from V _{cc} CAS before RAS refresh mode (Note 3)	M5M417800A-5,-5S	CAS before RAS refresh cycling trc = min. output open			145	mA
		M5M417800A-6,-6S				120	
		M5M417800A-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{cc1} (AV), I_{cc3} (AV), I_{cc4} (AV) and I_{cc6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I_{cc1} (AV) and I_{cc4} (AV) are dependent on output loading. Specified values are obtained with the output open.**CAPACITANCE** (T_a = 0~70°C, V_{cc} = 5V±10%, V_{ss} = 0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
C _i (A)	Input capacitance, address inputs	M5M417800AJ, TP, RT	V _i = V _{ss} f = 1MHz V _i = 25mVrms			5	pF
C _i ($\overline{\text{OE}}$)	Input capacitance, $\overline{\text{OE}}$ input					7	pF
C _i ($\overline{\text{W}}$)	Input capacitance, write control input					7	pF
C _i ($\overline{\text{RAS}}$)	Input capacitance, $\overline{\text{RAS}}$ input					7	pF
C _i ($\overline{\text{CAS}}$)	Input capacitance, $\overline{\text{CAS}}$ input					7	pF
C _{i/o}	Input/Output capacitance, data ports					8	pF

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FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

SWITCHING CHARACTERISTICS

(Ta = 0~70°C, Vcc = 5V±10%, Vss = 0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 6,8)		50		60		70	ns
tAA	Column address access time (Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 6,10)		30		35		40	ns
tOEa	Access time from $\overline{\text{OE}}$ (Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 11)	0	13	0	15	0	15	ns

Note 5 : An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.

7 : Assumes that $\text{trcd} \geq \text{trcd}(\text{max})$ and $\text{tasc} \geq \text{tasc}(\text{max})$.

8 : Assumes that $\text{trcd} \leq \text{trcd}(\text{max})$ and $\text{tradr} \leq \text{tradr}(\text{max})$. If trcd or tradr is greater than the maximum recommended value shown in this table, trac will increase by amount that trcd exceeds the value shown.

9 : Assumes that $\text{tradr} \geq \text{tradr}(\text{max})$ and $\text{tasc} \leq \text{tasc}(\text{max})$.

10 : Assumes that $\text{tcp} \leq \text{tcp}(\text{max})$ and $\text{tasc} \geq \text{tasc}(\text{max})$.

11 : tOFF (max) and tOEZ (max) defines the time at which the output achieves the high impedance state ($\text{Iout} \leq \pm 10 \mu\text{A}$) and is not reference to $\text{Voh}(\text{min})$ or $\text{Vol}(\text{max})$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta = 0~70°C, Vcc = 5V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits						Unit
		M5M4178A00-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		32		32		32	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note14)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	10		10		10		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	10		10		10		ns
tRAD	Column address delay time from RAS low (Note15)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	13		15		15		ns
tdZC	Delay time, data to CAS low (Note17)	0		0		0		ns
tdZO	Delay time, data to OE low (Note17)	0		0		0		ns
tcDD	Delay time, CAS high to data (Note18)	13		15		15		ns
tODD	Delay time, OE high to data (Note18)	13		15		15		ns
tr	Transition time (Note19)	1	50	1	50	1	50	ns

Note 12 : The timing requirements are assumed $t_T = 5\text{ns}$.

13 : $\text{Vih}(\text{min})$ and $\text{Vil}(\text{max})$ are reference levels for measuring timing of input signals.

14 : $\text{trcd}(\text{max})$ is specified as a reference point only. If trcd is less than $\text{trcd}(\text{max})$, access time is trac . If trcd is greater than $\text{trcd}(\text{max})$, access time is controlled exclusively by tcac or taa . $\text{trcd}(\text{min})$ is specified as $\text{trcd}(\text{min}) = \text{trah}(\text{min}) + 2t_H + \text{tasc}(\text{min})$.

15 : $\text{tradr}(\text{max})$ is specified as a reference point only. If $\text{tradr} \geq \text{tradr}(\text{max})$ and $\text{tasc} \leq \text{tasc}(\text{max})$, access time is controlled exclusively by taa .

16 : $\text{tasc}(\text{max})$ is specified as a reference point only. If $\text{trcd} \geq \text{trcd}(\text{max})$ and $\text{tasc} \geq \text{tasc}(\text{max})$, access time is controlled exclusively by tcac .

17 : Either tdzc or tdzo must be satisfied.

18 : Either tcdd or todd must be satisfied.

19 : t_T is measured between $\text{Vih}(\text{min})$ and $\text{Vil}(\text{max})$.

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****Read and Refresh Cycles**

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
trc	Read cycle time	90		110		130		ns
trAS	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	70	10000	ns
tcAS	$\overline{\text{CAS}}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	50		60		70		ns
trSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		20		ns
trCS	Read Setup time after $\overline{\text{CAS}}$ high	0		0		0		ns
trCH	Read hold time after $\overline{\text{CAS}}$ low (Note 20)	0		0		0		ns
trRH	Read hold time after $\overline{\text{RAS}}$ low (Note 20)	10		10		10		ns
trAL	Column address to $\overline{\text{RAS}}$ hold time	25		30		35		ns
toCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns
toRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns

Note 20 : Either trCH or trRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	50		60		70		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
twCS	Write setup time before CAS low (Note 22)	0		0		0		ns
twCH	Write hold time after CAS low	8		10		10		ns
tcWL	CAS hold time after W low	13		15		20		ns
trWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		15		ns
tOEh	OE hold time after W low	13		15		20		ns

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****Read-Write and Read-Modify-Write Cycles**

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note21)	131		155		180		ns
trAS	RAS low pulse width	91	10000	105	10000	120	10000	ns
tCAS	CAS low pulse width	54	10000	60	10000	70	10000	ns
tCSH	CAS hold time after RAS low	91		105		120		ns
trSH	RAS hold time after CAS low	54		60		70		ns
trCS	Read setup time before CAS low	0		0		0		ns
tcWD	Delay time, CAS low to W low (Note22)	36		40		45		ns
trWD	Delay time, RAS low to W low (Note22)	73		85		95		ns
tAWD	Delay time, address to W low (Note22)	48		55		60		ns
tcWL	CAS hold time after W low	13		15		20		ns
trWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before W low	0		0		0		ns
tDH	Data hold time after W low	10		10		15		ns
tOEH	OE hold time after W low	13		15		15		ns

Note 21 : trwc is specified as $trwc (min) = trac (max) + todd (min) + trwl (min) + trp (min) + 5tr$.

22 : twcs, tcwd, trwd and tawd and, tcpwd are specified as reference points only. If $twcs \geq twcs (min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $tcwd \geq tcwd (min)$, $trwd \geq trwd (min)$, $tawd \geq tawd (min)$ and $tcpwd \geq tcpwd (min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V_H) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tpc	Fast page mode read/write cycle time	35		40		45		ns
tpRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tras	RAS low pulse width for read write cycle (Note24)	85	125000	100	125000	115	125000	ns
tcp	CAS high pulse width (Note25)	8	12	10	15	10	15	ns
tcPRH	RAS hold time after CAS precharge	30		35		40		ns
tcpWD	Delay time, CAS precharge to $\overline{W}$ low (Note22)	53		60		65		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24 : tras (min) is specified as two cycles of CAS input are performed.

25 : tcp (max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		10		ns
tCHR	CAS hold time after RAS low	10		10		15		ns
tRSR	Read setup time before RAS low	10		10		10		ns
trHR	Read hold time after RAS low	10		10		15		ns

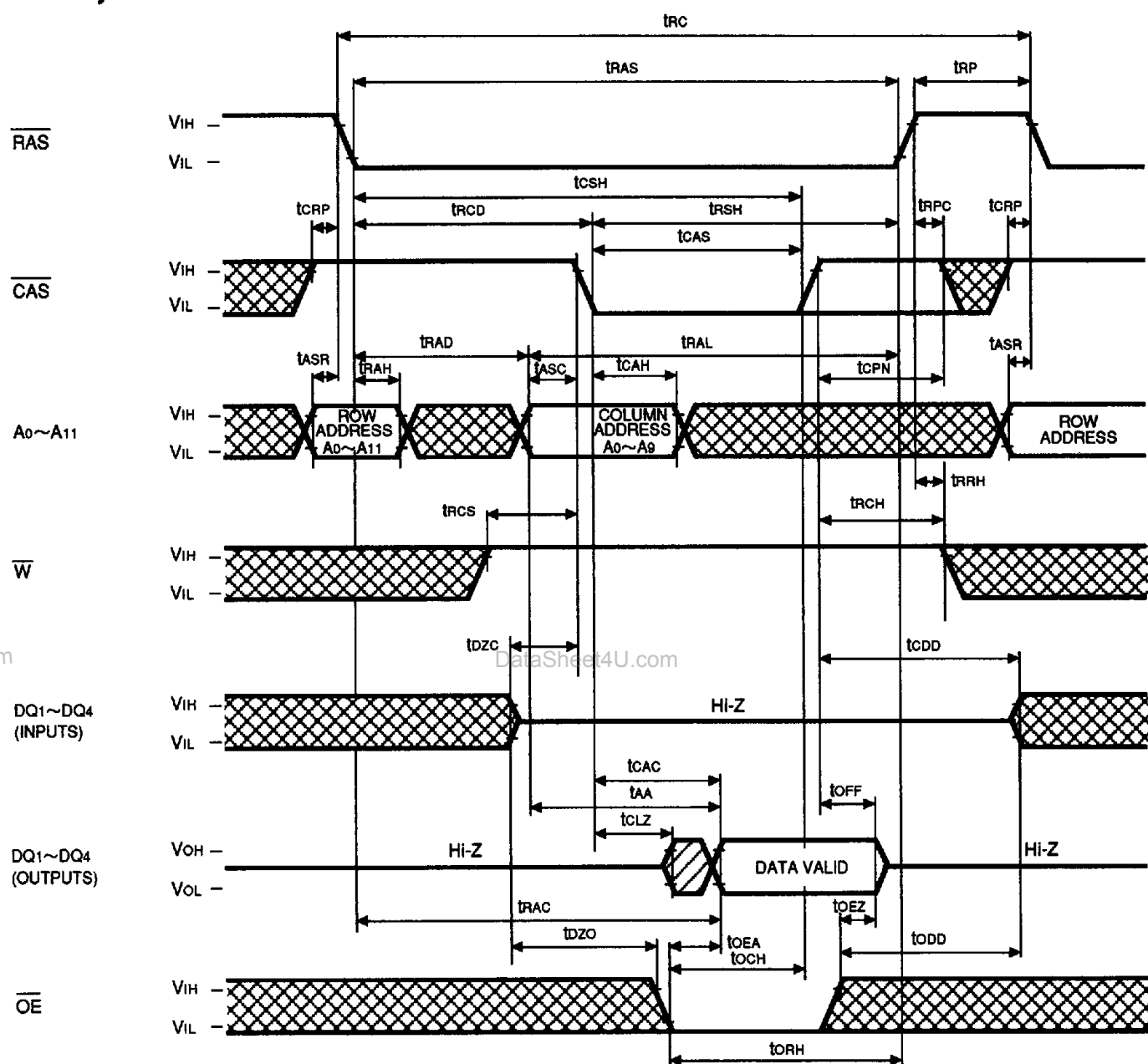
Note 26 : Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

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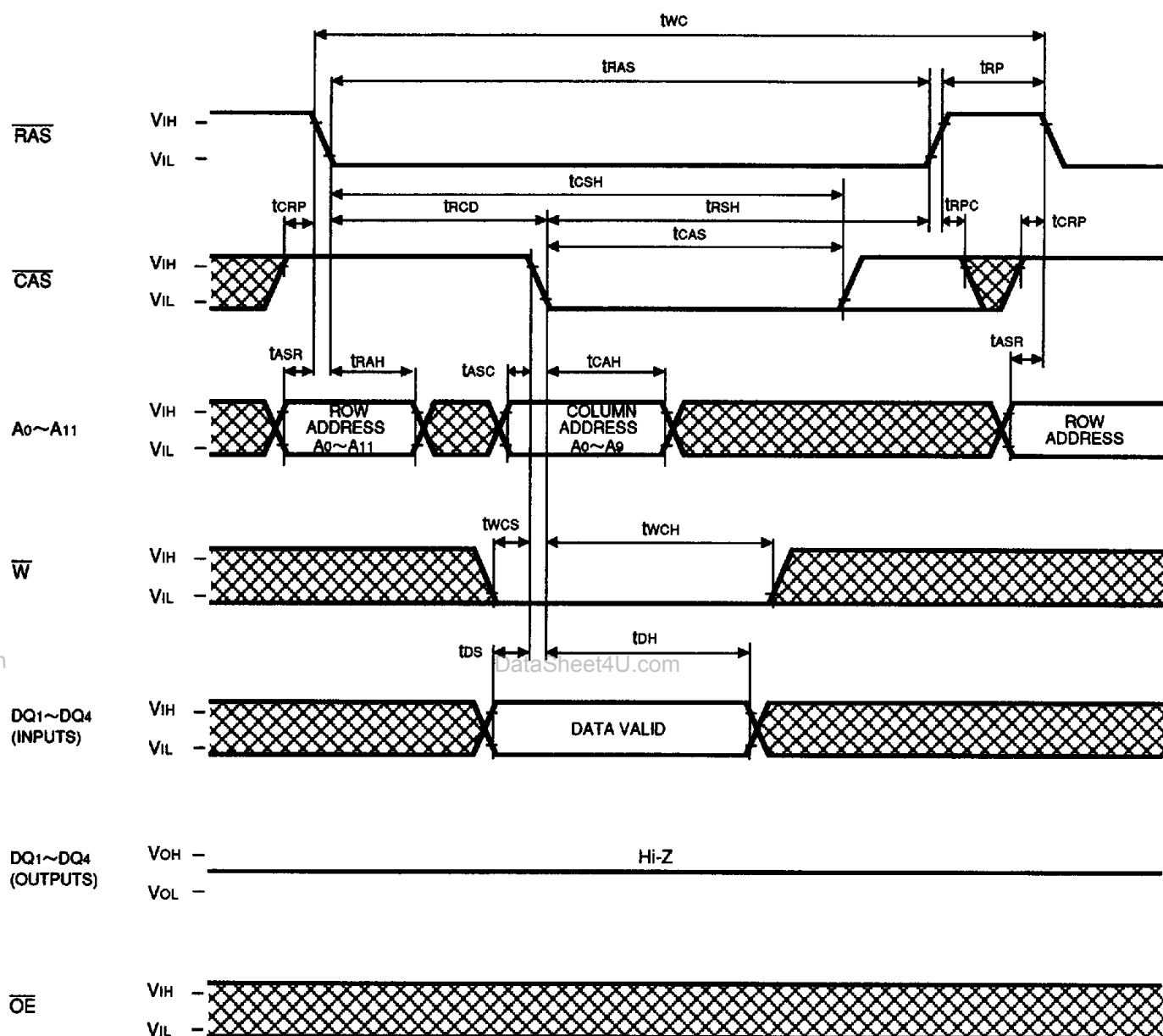
Timing Diagrams (Note 27)

Read Cycle



Note 27

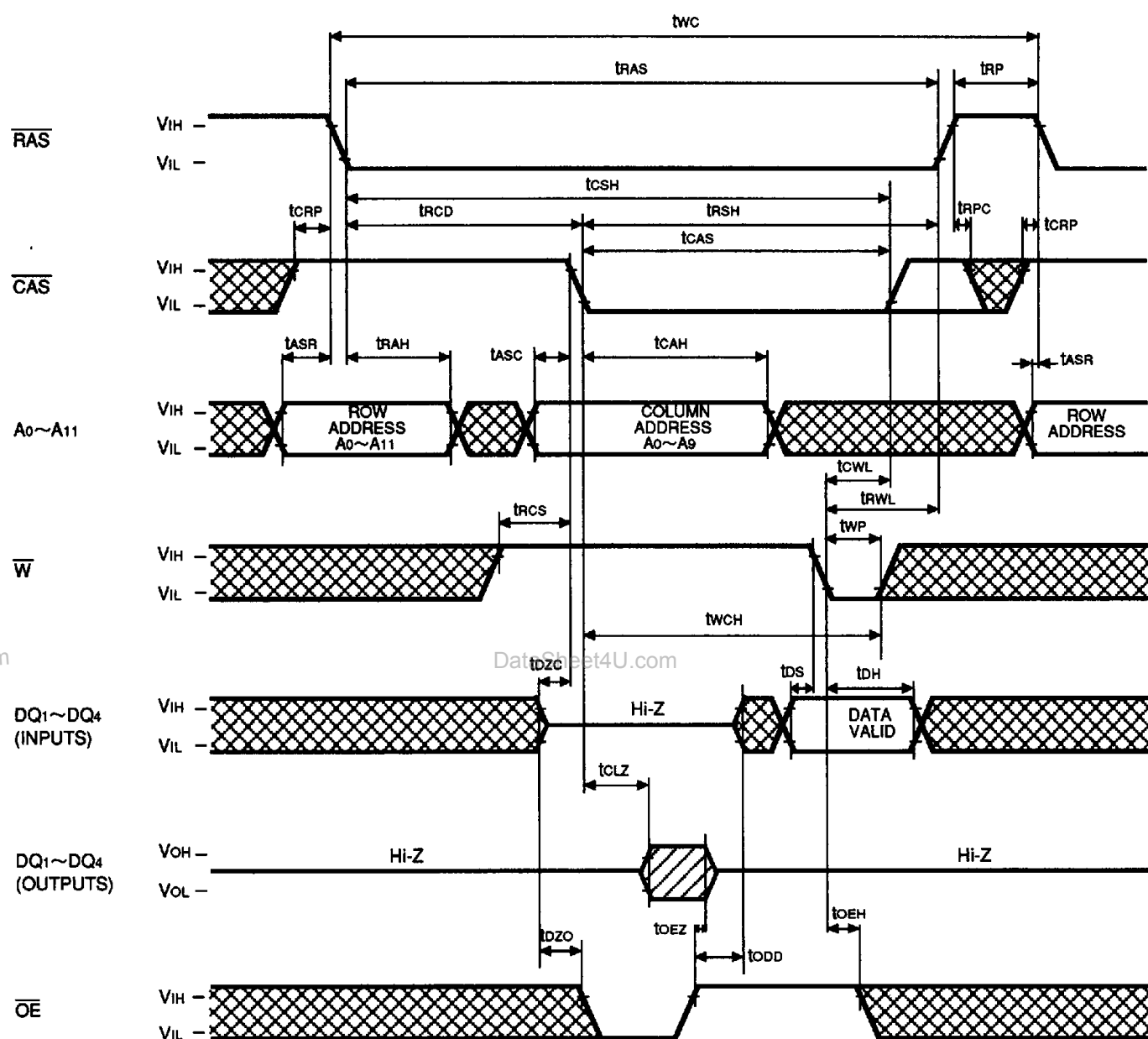
	Indicates the don't care input. $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$
	Indicates the invalid output.

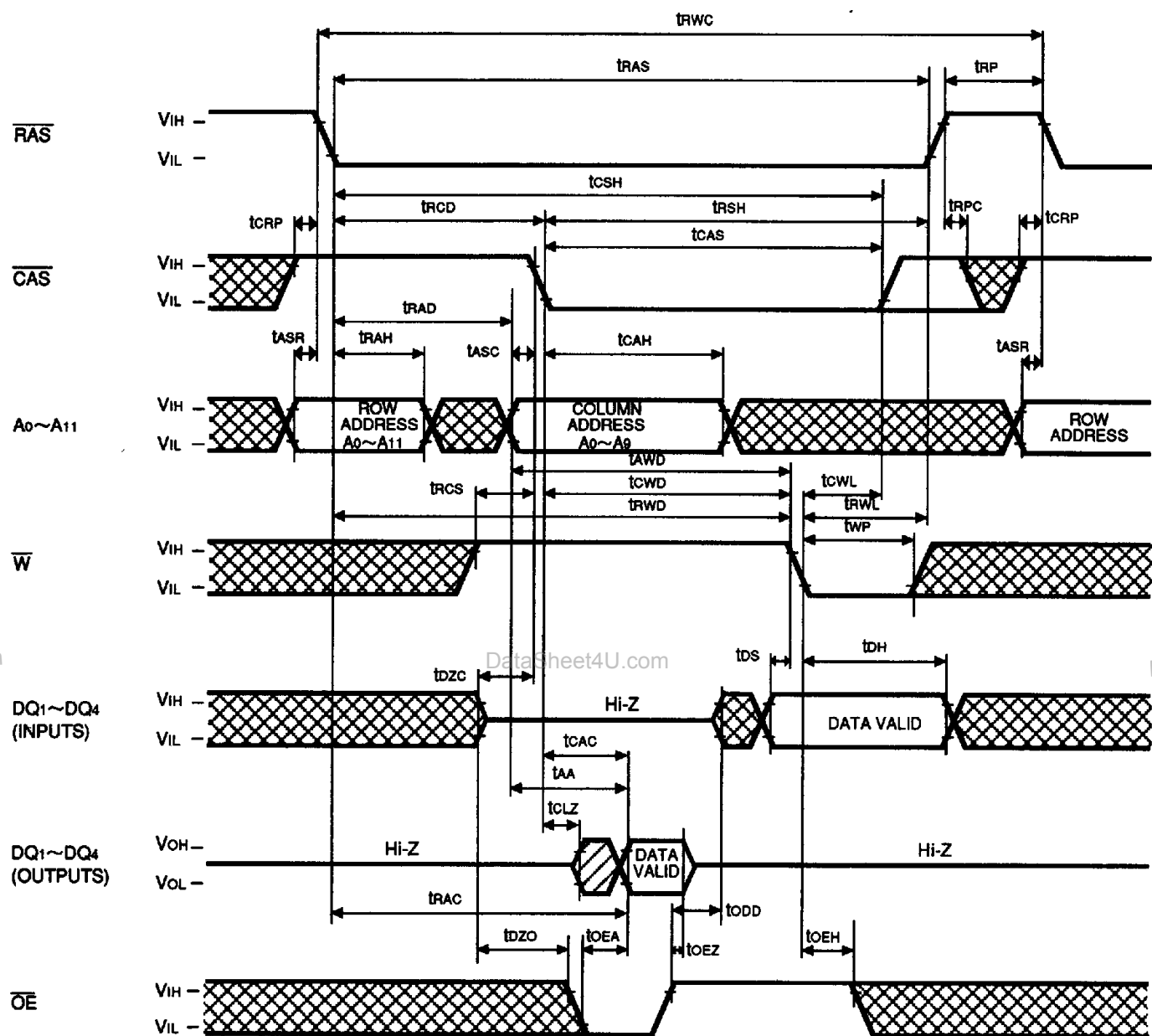
M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****Write Cycle (Early write)**

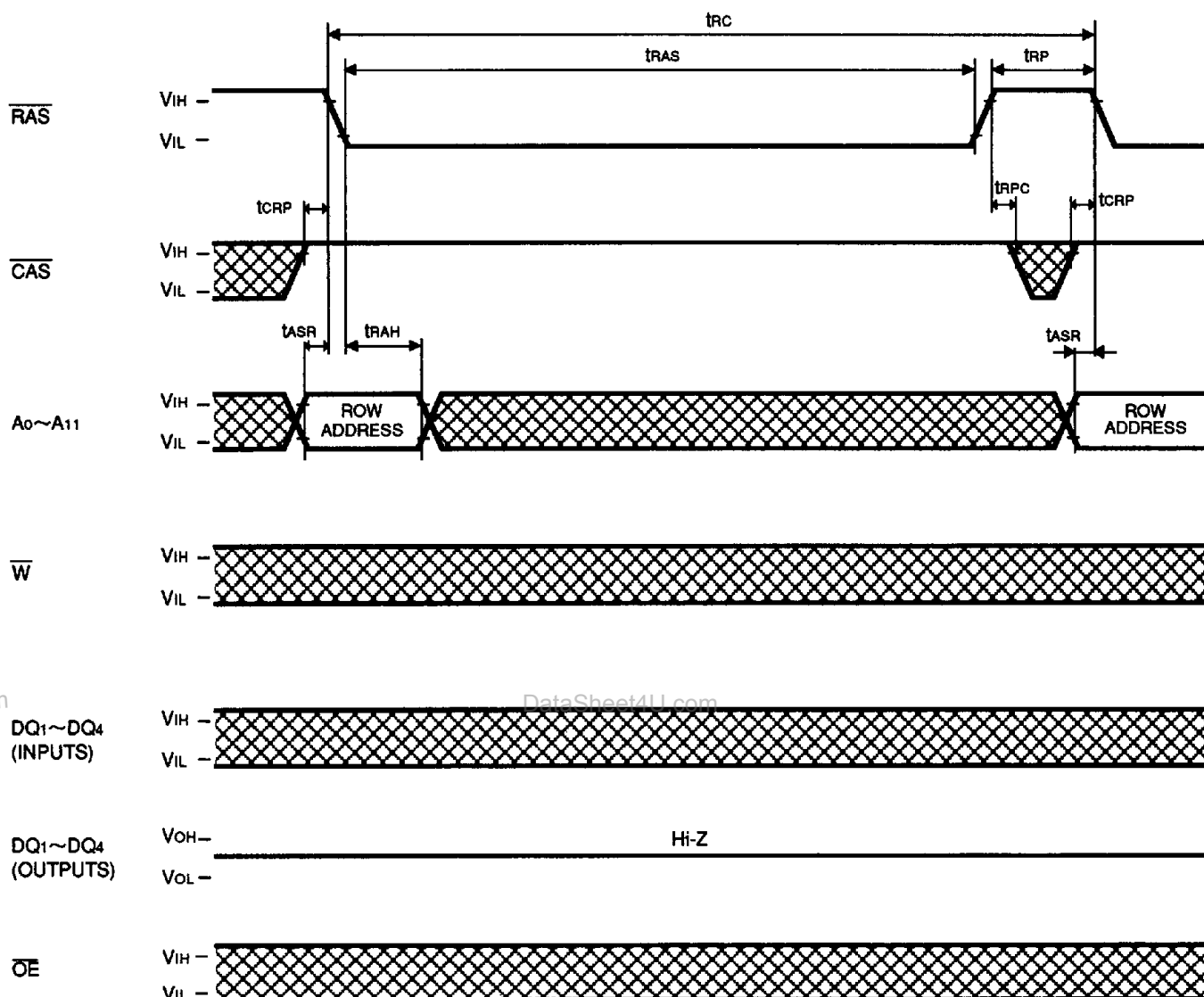
M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S

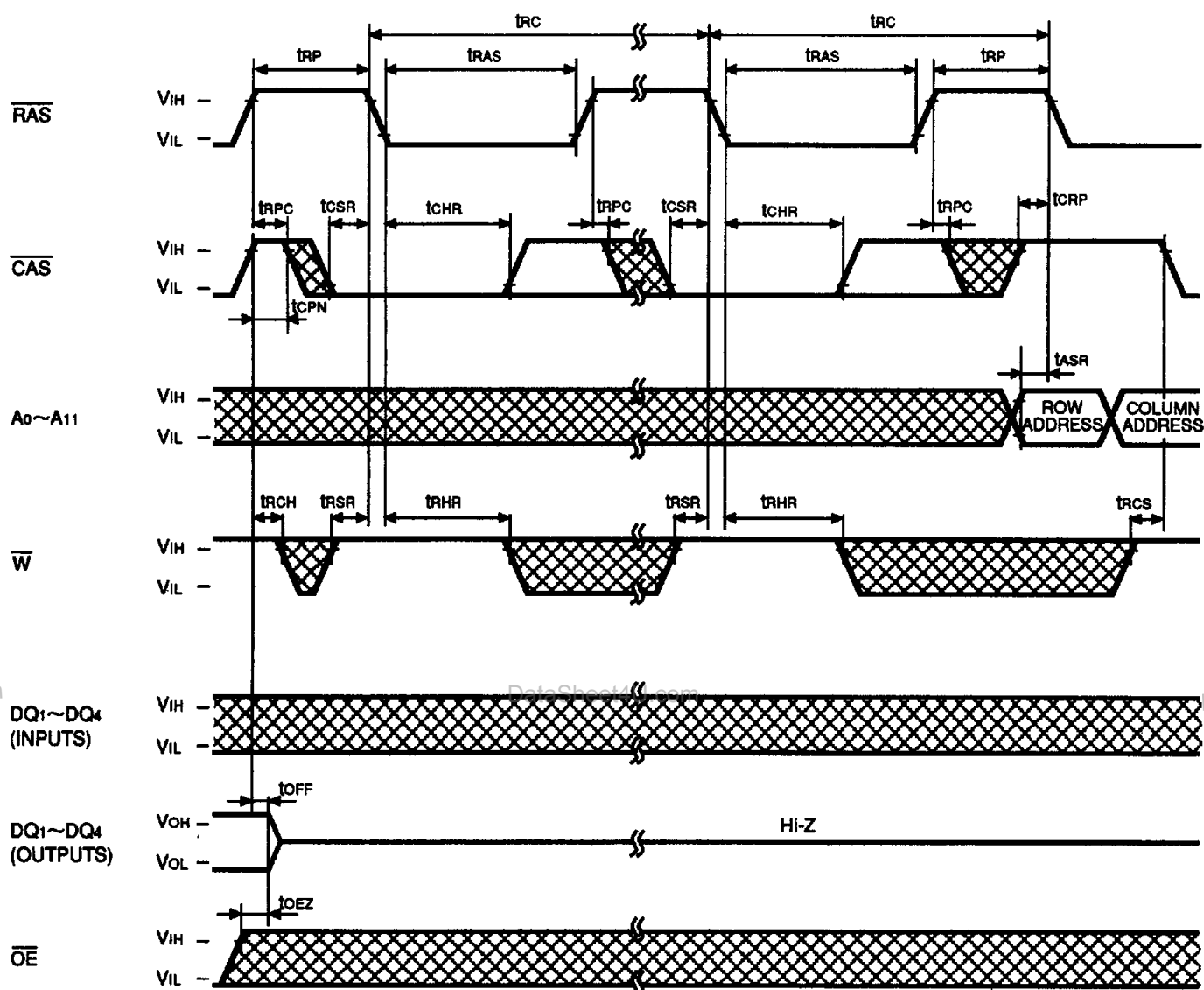
FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

Write Cycle (Delayed write)



M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****Read-Write, Read-Modify-Write Cycle**

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM** **$\overline{\text{RAS}}$ -only Refresh Cycle**

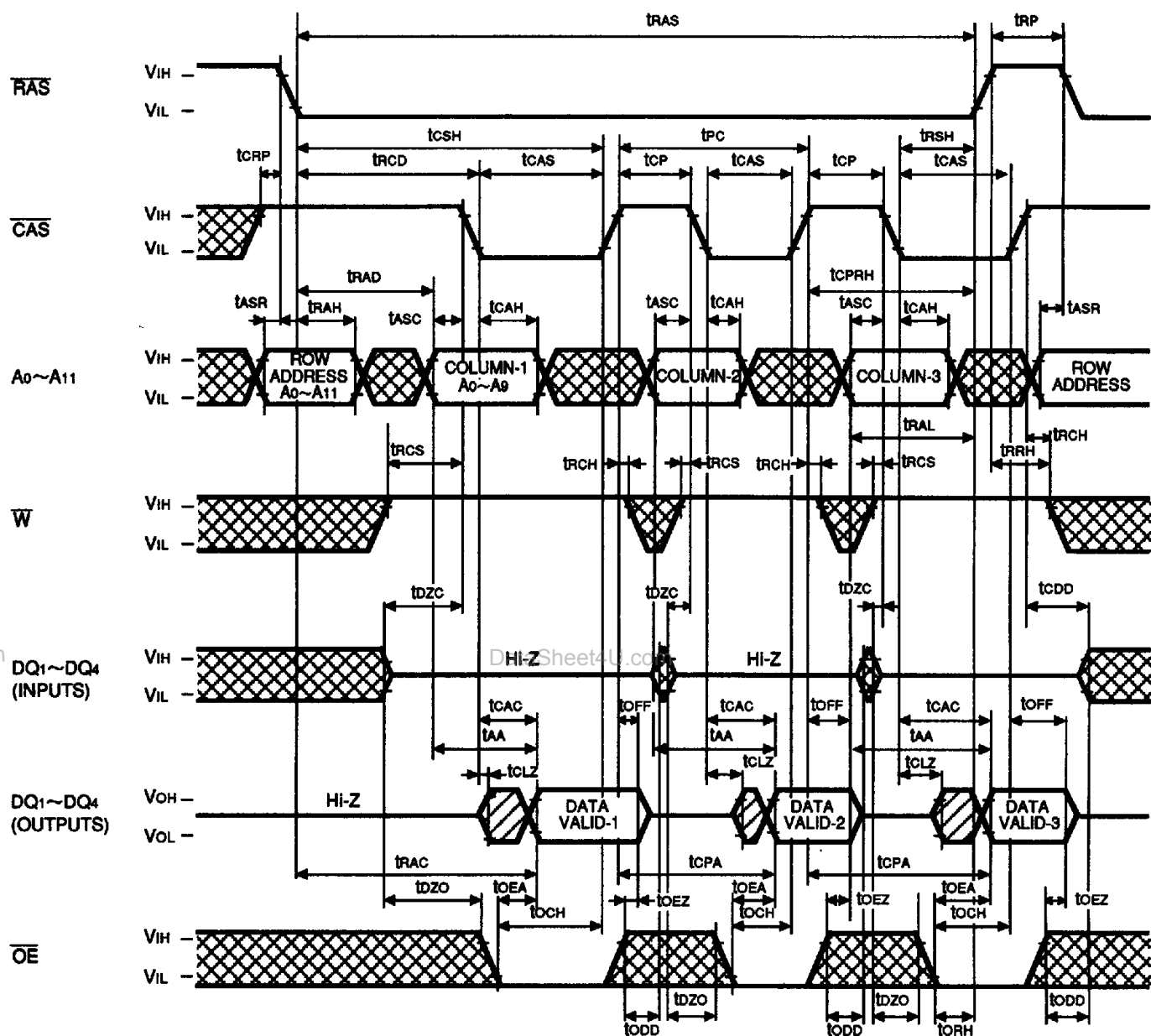
M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****CAS before RAS Refresh Cycle**

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

The diagram illustrates the timing relationships for the 64K1602 LCD module. It shows the signals RAS, CAS, A0~A11, W, DQ1~DQ4 (INPUTS), DQ1~DQ4 (OUTPUTS), and W. The timing parameters are defined as follows:

- RAS:** t_{RC} (Row Access Time), t_{RP} (Row Pulse Width), t_{CRP} (Row Setup Time), t_{CHD} (Row Hold Time).
- CAS:** t_{ASR} (Column Setup Time), t_{RAH} (Row Address Hold Time), t_{ASC} (Row Address Setup Time), t_{CAH} (Column Address Hold Time), t_{RCS} (Row Column Setup Time), t_{RAL} (Row Address Latency), t_{RRH} (Row Address Hold Time).
- A0~A11:** t_{RAD} (Row Address Delay), t_{RSH} (Row Setup Time), t_{RCH} (Row Hold Time), t_{RCS} (Row Column Setup Time), t_{RAL} (Row Address Latency), t_{RRH} (Row Address Hold Time).
- W:** t_{DZC} (Data Zero Setup Time), t_{CDD} (Data Delay Time), t_{DZC} (Data Zero Setup Time), t_{CDD} (Data Delay Time).
- DQ1~DQ4 (INPUTS):** t_{CAC} (Data Setup Time), t_{AA} (Data Address Setup Time), t_{CLZ} (Data Clear Time), t_{OFF} (Data Output Time), t_{DZC} (Data Zero Setup Time), t_{CDD} (Data Delay Time).
- DQ1~DQ4 (OUTPUTS):** t_{OEA} (Data Output Enable Time), t_{ORH} (Data Output Hold Time), t_{DZO} (Data Zero Output Time), t_{OEZ} (Data Output Enable Time), t_{ODD} (Data Output Delay Time).

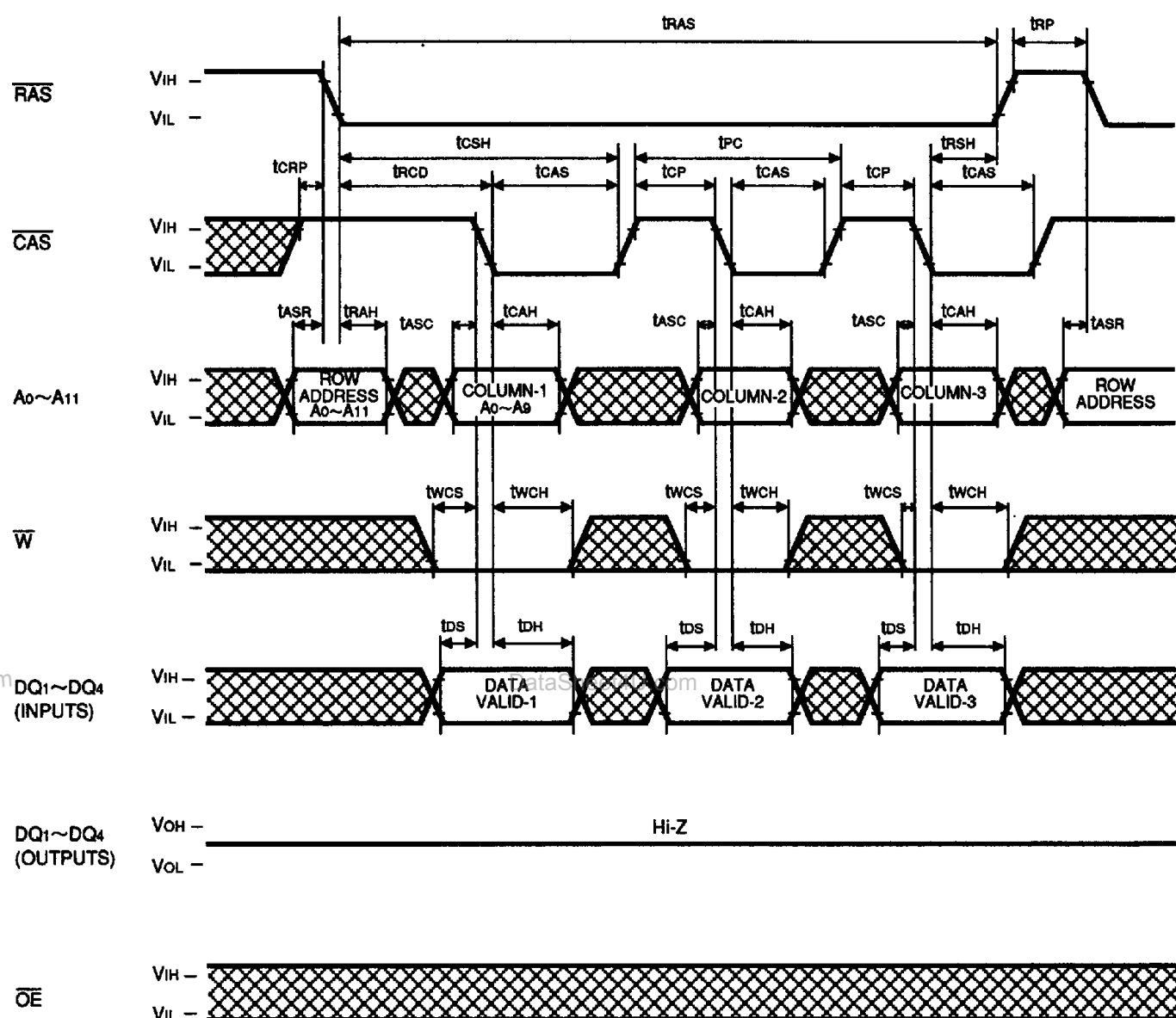
Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****Fast Page Mode Read Cycle**

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)



FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

[illegible]

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

The timing diagram illustrates the sequence of signals for the 64K1602 LCD module. The signals shown are:

- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- A0~A11**: Address bus, providing ROW ADDRESS, COLUMN-1, COLUMN-2, and ROW ADDRESS.
- W**: Write Enable, active low.
- DQ1~DQ4 (INPUTS)**: Data bus for inputs.
- DQ1~DQ4 (OUTPUTS)**: Data bus for outputs.
- OE**: Output Enable, active low.

Key timing parameters labeled in the diagram include:

- t_{RAS} : RAS pulse width.
- t_{RCD} : RAS to CAS delay.
- t_{CAH} : CAS high pulse width.
- t_{CP} : CAS to RAS delay.
- t_{PRWC} : Precharge to RAS delay.
- t_{TRP} : Precharge to RAS delay.
- t_{TRWL} : RAS to precharge delay.
- t_{RAD} : RAS to address delay.
- t_{TASR} : Address to RAS delay.
- t_{TRAH} : Address to RAS delay.
- t_{TASC} : Address to RAS delay.
- t_{TAWD} : Address to write delay.
- t_{TRCS} : RAS to column strobe delay.
- t_{TCWD} : Column strobe to write delay.
- t_{TCWL} : Column strobe to write delay.
- t_{TWP} : Write pulse width.
- t_{TRWD} : Write pulse width.
- t_{TCPWD} : Column strobe to precharge delay.
- t_{TDZC} : Data to column strobe delay.
- t_{TDS} : Data to column strobe delay.
- t_{TDH} : Data to column strobe delay.
- t_{TCAC} : Column strobe to address delay.
- t_{TAA} : Address to address delay.
- t_{TCLZ} : Column strobe to column strobe delay.
- t_{TRAC} : RAS to address delay.
- t_{TDZO} : Data to column strobe delay.
- t_{TOEA} : Data to column strobe delay.
- t_{TODD} : Data to column strobe delay.
- t_{TCPA} : Column strobe to precharge delay.
- t_{TOEZ} : Data to column strobe delay.
- t_{TOEH} : Data to column strobe delay.

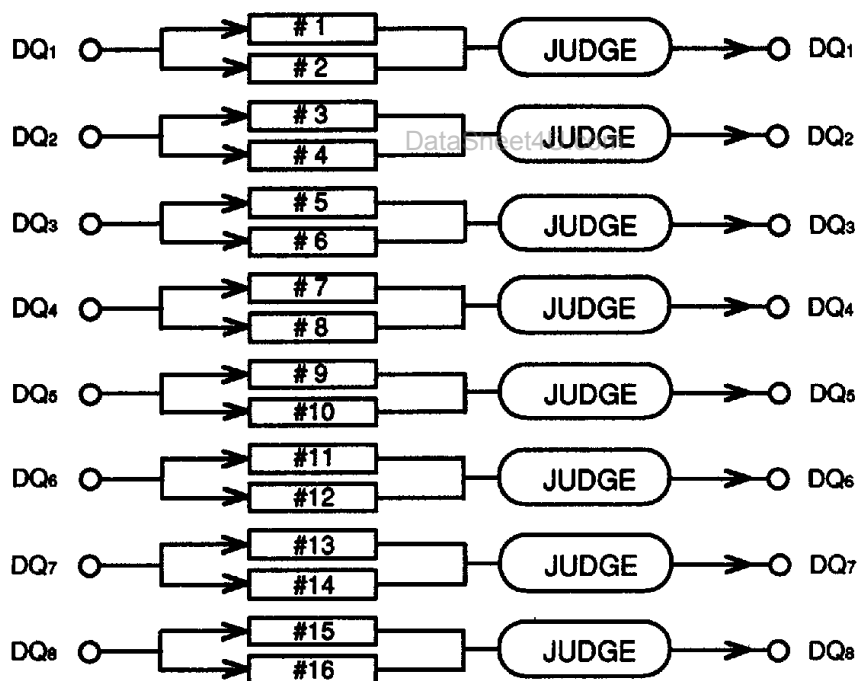
M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S

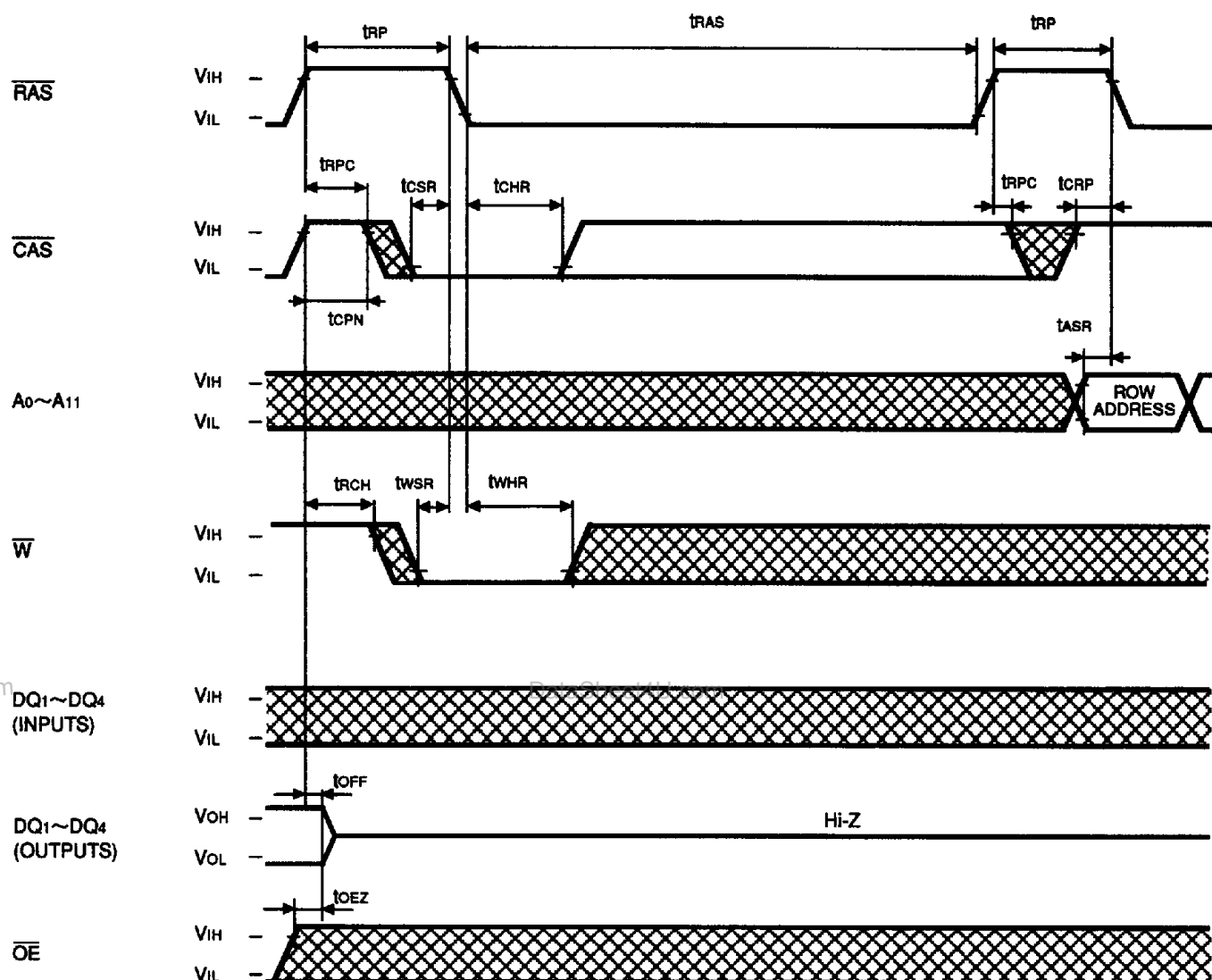
FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

TEST Mode SET Cycle

Symbol	Parameter	Limits						Unit
		M5M417800A-5,-5S		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t _{WSR}	W setup time before RAS low	10		10		10		ns
t _{WHR}	W hold time after RAS low	10		10		15		ns

Note 29 : The test mode function is initiated by a W and CAS before RAS cycle (WCBR cycle) as specified in timing diagram.
 The test mode function is terminated by either a CAS before RAS refresh cycle (CBR refresh cycle) or a RAS only refresh cycle.
 During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). No addressing of CA0, CA1 is required.
 During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
 During the test mode operation, WCBR cycle can be used to perform refresh.



M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 1677216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****TEST Mode SET Cycle**

M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S**FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM****SELF REFRESH SPECIFICATIONS**

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, $V_{ss} = 0V$, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CCS} (AV)	Average supply current from V_{cc} Self-Refresh cycle	M5M417800A (S) $\overline{RAS} = \overline{CAS} \leq 0.2V$			400	μA

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, $V_{ss} = 0V$, unless otherwise noted See notes 12,13)

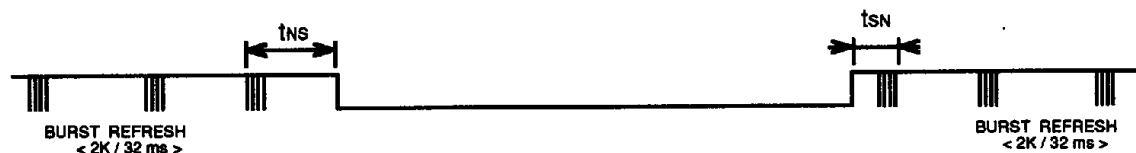
Symbol	Parameter	Limits						Unit
		M5M417800A-5S		M5M417800A-6S		M5M417800A-7S		
		Min	Max	Min	Max	Min	Max	
t _{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t _{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t _{CHS}	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns
t _{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t _{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS**(1) In case of distributed refresh**

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leq 32 \text{ ms}$ and $t_{SN} \leq 32 \text{ ms}$.

**(2) In case of burst refresh**

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leq 32 \text{ ms}$.



M5M417800AJ,TP,RT-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

Self Refresh Cycle

