

## N-Channel 100-V (D-S) MOSFET

### Key Features:

- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed
- Small Footprint DFN3x2-8L package

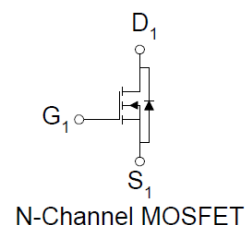
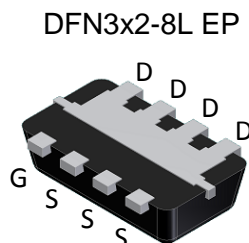
### Typical Applications:

- Telecom DC/DC converters
- White LED boost converters
- Industrial DC/DC conversion
- Automotive Entertainment and GPS DC/DC conversion

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
100	280 @ $V_{GS} = 10V$	2.1
	355 @ $V_{GS} = 4.5V$	1.9



RoHS  
COMPLIANT  
HALOGEN  
FREE



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	2.1
		$T_A = 70^\circ\text{C}$	1.7
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	$\pm 10$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	3	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 70^\circ\text{C}$	1.6
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	$t \leq 10$ sec	50
		Steady State	90

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

## Electrical Characteristics

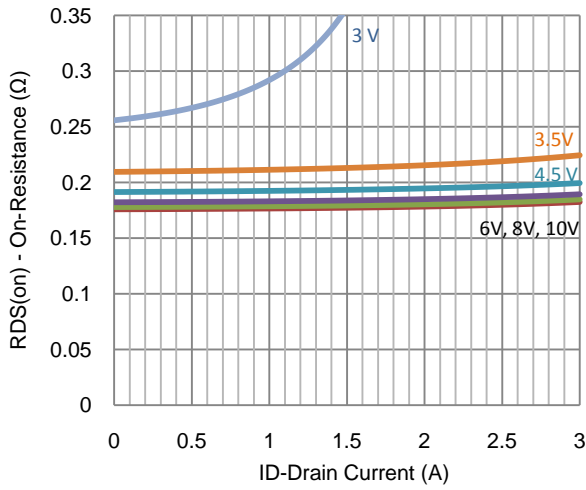
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		3.5	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	10			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 1.7 A$			280	m $\Omega$
		$V_{GS} = 4.5 V, I_D = 1.5 A$			355	
Forward Transconductance	$g_{fs}$	$V_{DS} = 15 V, I_D = 1.7 A$		5		S
Diode Forward Voltage	$V_{SD}$	$I_S = 1.5 A, V_{GS} = 0 V$		0.8		V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 1.7 A$		4.1		nC
Gate-Source Charge	$Q_{gs}$			1		
Gate-Drain Charge	$Q_{gd}$			1.9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50 V, R_L = 30 \Omega, I_D = 1.7 A,$ $V_{GEN} = 10 V, R_{GEN} = 6 \Omega$		3		ns
Rise Time	$t_r$			3		
Turn-Off Delay Time	$t_{d(off)}$			10		
Fall Time	$t_f$			3		
Input Capacitance	$C_{iss}$	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz$		420		pF
Output Capacitance	$C_{oss}$			50		
Reverse Transfer Capacitance	$C_{rss}$			30		

## Notes

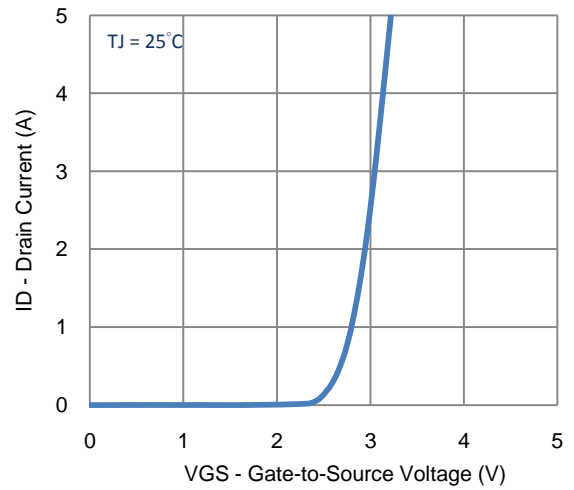
- Pulse test: PW  $\leq$  300us duty cycle  $\leq$  2%.
- Guaranteed by design, not subject to production testing.

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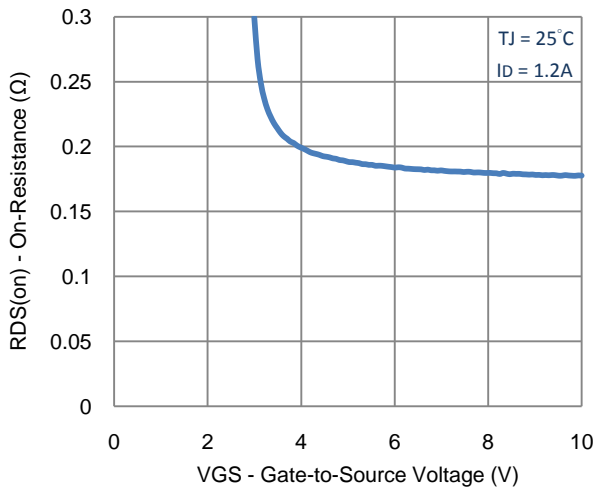
Typical Electrical Characteristics



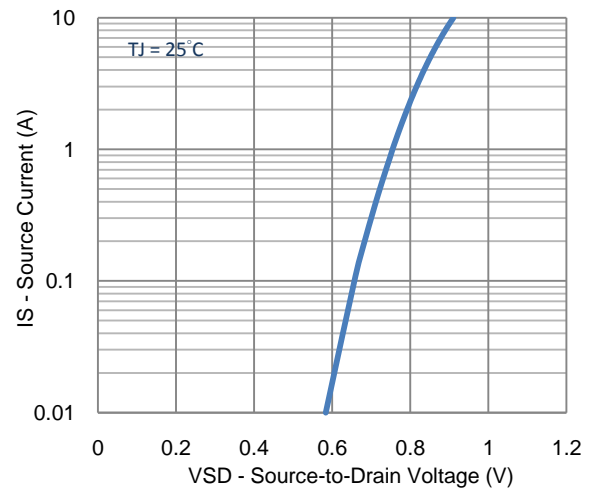
1. On-Resistance vs. Drain Current



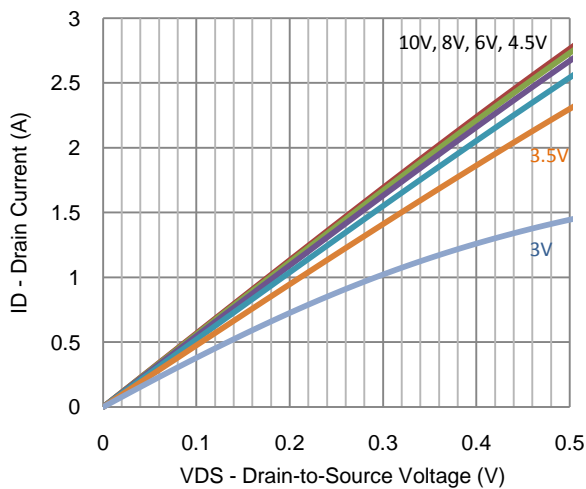
2. Transfer Characteristics



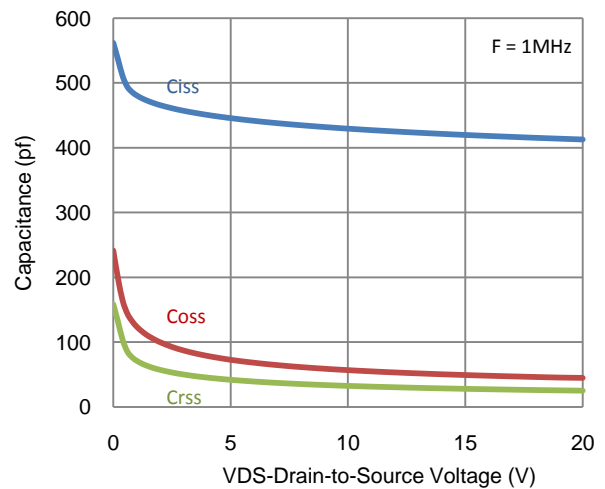
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

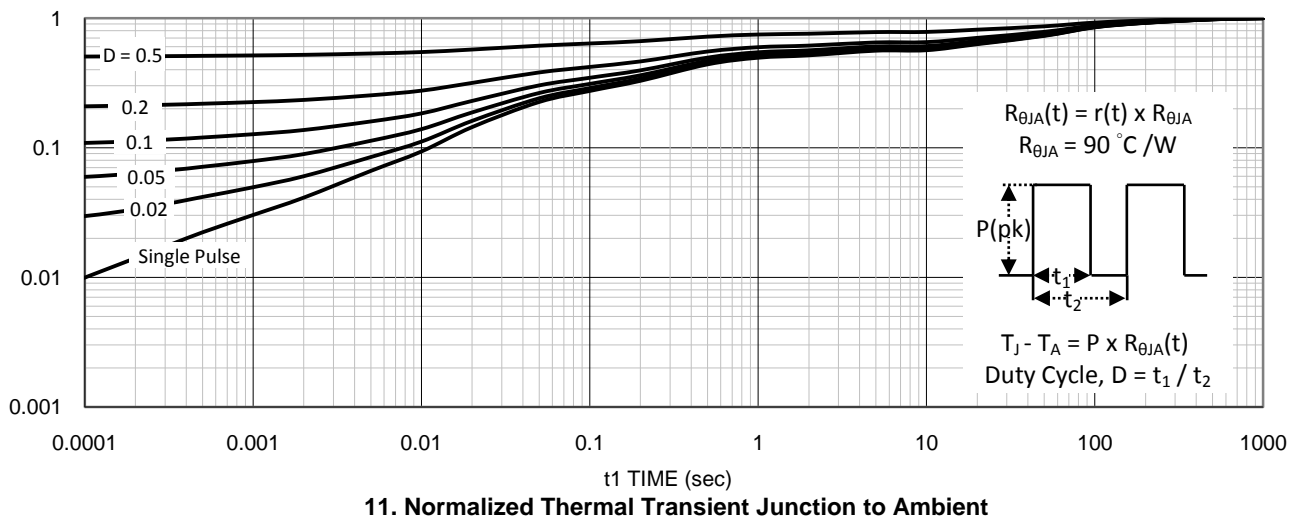
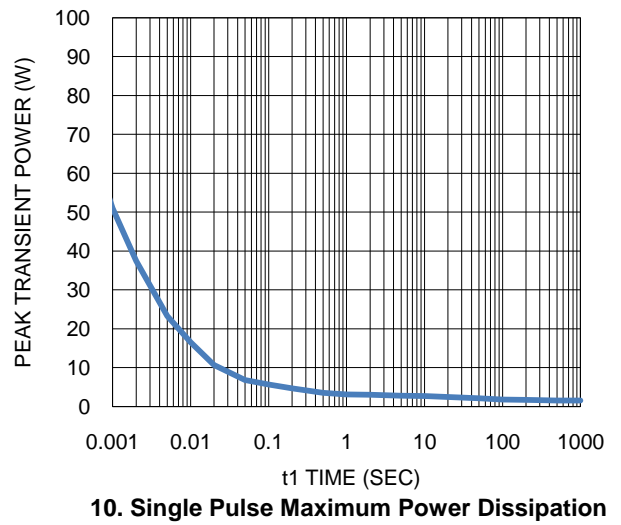
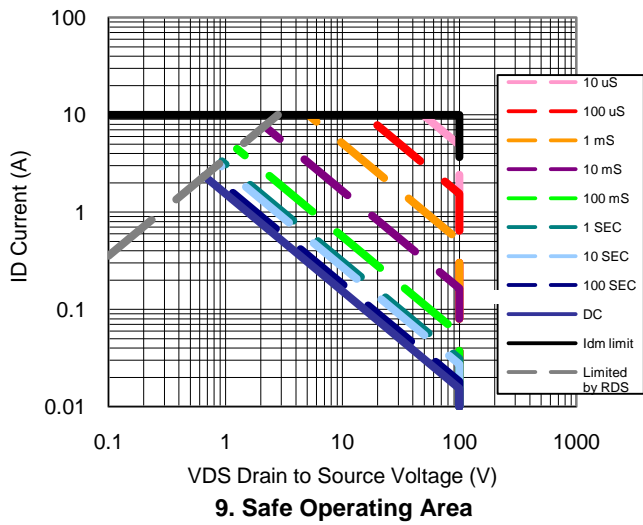
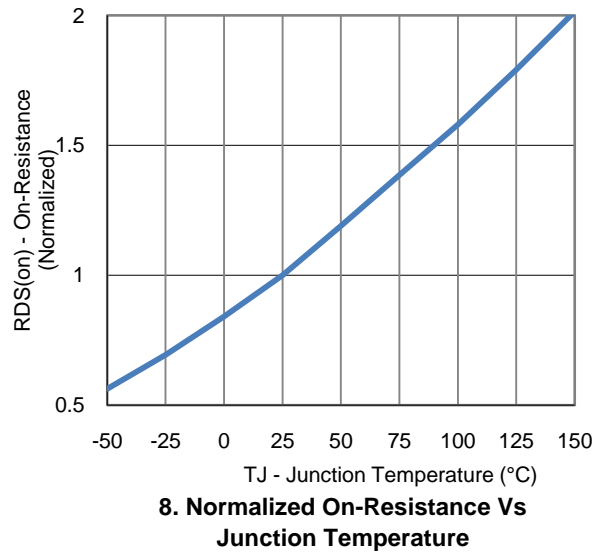
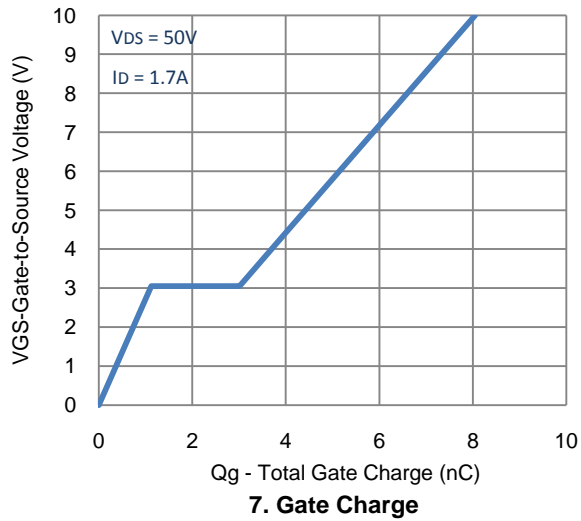


5. Output Characteristics

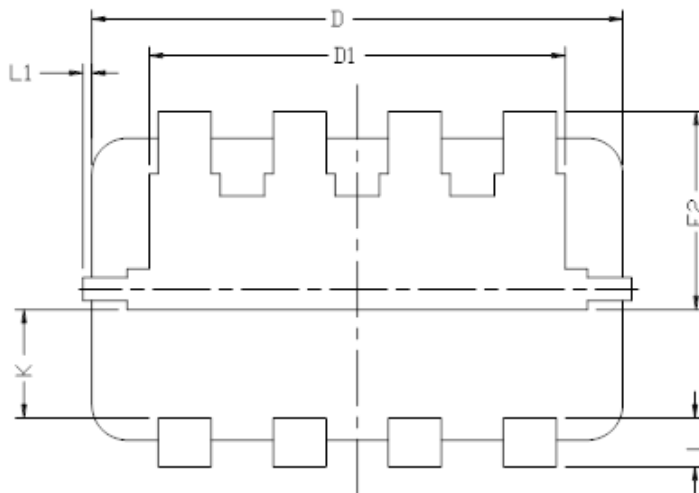
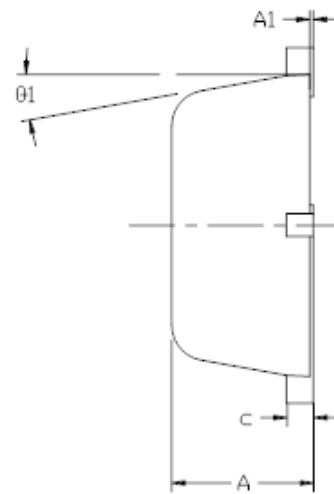
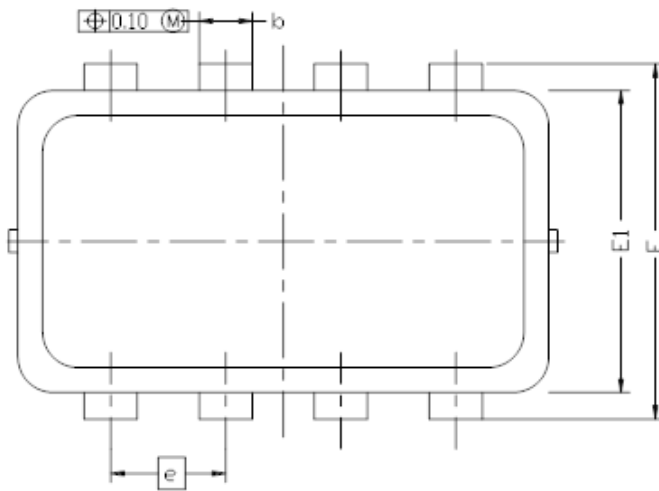


6. Capacitance

Typical Electrical Characteristics



Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.152	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.30	2.35	2.40	0.091	0.093	0.095
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
E2	1.065	1.115	1.165	0.042	0.044	0.046
e	0.65 BSC			0.026 BSC		
L	0.20	0.275	0.400	0.008	0.011	0.0157
K	0.56	0.61	0.66	0.022	0.024	0.026
L1	0	---	0.100	0	---	0.004
theta 1	0	10	12	0	10	12

Note:

1. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
2. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.